TECHNICAL MANUAL

ORGANIZATIONAL MAINTENANCE MANUAL
DISPLAY EQUIPMENT MAINTENANCE

EXPANDED TROUBLESHOOTING
(LOGIC DIAGRAM THEORY)

GUIDED MISSILE
AIR DEFENSE SYSTEM
AN/TSQ-73

This copy is a reprint which includes current pages from Change 1.

HEADQUARTERS, DEPARTMENT OF THE ARMY

25 JANUARY 1985

Change

No.1

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TM 9-1430-655-20-4-2, 21 January 1985, is changed as follows:

1. Remove old pages and insert new pages as indicated below. New or changed material is indicated by the applicable change number, i.e., Change 1, at the bottom of the page adjacent to the page number. Revised text will have a vertical bar in the margin next to the changed area. Revised illustrations will have suffix change letter added to the identification number.

Remove Pages	*Insert Pages*
A and B	A and B
i and ii	i and ii
5-7 and 5-8	5-7 and 5-8
5-55 and 5-56	5-55 and 5-56

2. File this change sheet in front of the publication for reference.

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WARNING

DANGEROUS VOLTAGE

is used in the operation of this equipment

DEATH ON CONTACT

may result if personnel fail to observe safety precautions

Never work on electronic equipment unless there is another person nearby who is familiar with the operation and hazards of the equipment and who is competent in administering first aid. When the technician is aided by operators, he must warn them about dangerous areas.

Whenever possible, the power supply to the equipment must be shut off before beginning work on the equipment. Take particular care to ground every capacitor likely to hold a dangerous potential. When working inside the equipment, after the power has been turned off, always ground every part before touching it.

Be careful not to contact high-voltage connections when installing or operating this equipment.

Whenever the nature of the operation permits, keep one hand away from the equipment to reduce the hazard of current flowing through vital organs of the body.

WARNING

Do not be misled by the term "low voltage." Potentials as low as 50 volts may cause death under adverse conditions.

EXTREMELY DANGEROUS POTENTIALS

greater than 500 volts exist in the following units:

Display console high voltage power supply

Display console CRT

WARNING

For emergencies requiring immediate shutdown of system power, press SYSTEM POWER OFF switch located on power cabinet power transfer unit. Observe that SYSTEM POWER ON indicator light goes off.

LIST OF EFFECTIVE PAGES

Insert latest change pages, dispose of superseded pages in accordance with applicable regulations.

NOTE: On a changed page, the portion of the text affected by the changes is indicated by a vertical line in the outer margins of the page.

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5-361	0	5-419	0	5-525	0
5-362 Blank	0	5-420 Blank	0	5-526 Blank	0
5-363 - 5-365	0	5-421	0	5-527	0
5-366 Blank	0	5-422 Blank	0	5-528 Blank	0
5-367	0	5-423	0	5-529 - 5-536	0
5-368 Blank	0	5-424 Blank	0		

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REPORTING OF ERRORS

You can help improve this publication. If you find any mistakes, or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms), or DA Form 2028-2 located in back of this manual direct to: Commander, U.S. Army Missile Command, ATTN: AMSMI-LC- ME-P, Redstone Arsenal, AL 35898-5238. A reply will be furnished to you.

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CHAPTER 5

DISPLAY CONSOLE EXPANDED TROUBLESHOOTING

Section I. INTRODUCTION

5-1. Scope. This manual is part two TM 9-1430-655-20-4, display console organizational maintenance for Guided Missile Air Defense System AN/TSQ-73, and provides supplemental expanded troubleshooting information. This manual is published for the use and guidance of advanced personnel responsible for repair of the display console beyond the scope of organizational maintenance covered in the basic TM 9-1430-655-20 series technical manuals.

5-2. Expanded Troubleshooting Concept. The expanded troubleshooting concept and troubleshooting criteria are described in the following subparagraphs.

a. *Expanded Troubleshooting.* Expanded troubleshooting is required when existing fault isolation procedures in the basic manuals fail to isolate and correct a malfunction. It is assumed that expanded troubleshooting will be performed by personnel fully trained and experienced in the AN/TSQ-73 system and its mission.

b. *Troubleshooting Criteria.* Expanded troubleshooting covered in this manual is based on use of existing on-site equipment (tapes, tools, test equipment, spare parts, and publications). Isolation of malfunctions is based on fault analysis of normal system operating conditions and using built-in M&D software programs.

5-3. Troubleshooting Aids. Reference material contained in this manual to aid in performing troubleshooting procedures are detailed below.

a. *Contents of Manual.* This manual contains functional logic diagrams to enhance troubleshooting and fault isolation capabilities. The functional logic diagrams and the associated circuit descriptions are intended to be self-contained and minimize requirements of additional troubleshooting aids. Also, power distribution diagrams, cabling diagrams, and front-panel schematic diagrams are supplied.

b. *Input/Output Tables.* Input and output tables are provided as applicable for each figure and sheet to enable easy access to signals referenced to other diagrams.

c. *Input and Output Symbology.* Symbols used on diagrams to indicate input and input signals include the following:

▲ Indicates input from another figure.

▲ Indicates input from same figure.

■ Indicates output to another figure.

□ Indicates output to same figure.

◪ Indicates output to same and another figure.

d. *Equipment Interface.* The troubleshooting diagrams may reference inputs and outputs interfacing between other equipments. When a notation that an external equipment is involved, it is assumed that the user will refer to the applicable troubleshooting information provided for that equipment.

e. *Logic Symbology.* Logic symbology depends on card types. For discrete circuit cards containing conventional integrated circuits, conventional logic symbols are used. These symbols are used independently with card locations and card pin numbers notated with the symbol. For analog circuits, circuit card details are provided only to a functional level.

5-4. Physical Description (fig. 5-1). The display console is a free-standing assembly consisting of a cabinet assembly and three slide-mounted chassis assemblies. Two display consoles (units IA5 and IA6) are normally installed in the AN/TSQ-73 system shelter (unit 1). Provisions are provided for installing either or both display consoles in a remoted position external to the system shelter. Refer to TM 9-1430-655-20-1 for cabling diagrams depicting the various display console installations. Refer to table 5-1 for a cross-reference of part numbers and drawing numbers for major system equipment in reference designator order; refer to table 5-2 for a detailed cross-reference of major display console assemblies and components.

a. *Cabinet Assembly.* The display console cabinet assembly is an electromechanical enclosure housing three slide-mounted electronic assemblies. Mechanically, the cabinet assembly contains a cooling system and provides mounting provisions for cables, power supplies, and mechanical components.

(1) Electronic assemblies. The electronic assemblies include the left (A1) and right hand (A3) assemblies and the center section (A2) which are mounted in the upper portion of the cabinet assembly. When installed, the front panels of the electronic assemblies provide an overall operating surface of approximately 24 by 29 inches; the operating surface is tilted 15 degrees from the vertical for operating convenience. A bullnose, or writing shelf, is externally mounted on the cabinet for use by the operator.

(2) *Cabinet cooling system*. Cooling air circulation within the display console is accomplished by an internally mounted blower (A4) which draws in ducted air for distribution to electronic components by an air plenum. Intake and exhaust air filters provide emi-isolation and dust filtering.

(3) *Cabinet cable set.* The cabinet cable set includes wiring harnesses and cable assemblies W251 thru W253, W255, W256, and W270 thru W272. The cable set provides electrical interconnection between internal electronic components and external interface. Tilted connector panels are mounted on both sides of the lower cabinet recess. The connector panel accommodates interconnecting cabling as well as providing facilities for two headsets and a footswitch used for voice communications.

(4) *Power supplies.* The power supplies are also mounted in the lower cabinet recess behind an access panel. The power supplies include three dc/dc converters (PS1 thru PS3) and a variable lamp power supply (PS4). A hinged door in the access panel permits MTS interface. The MTS interface card is normally installed in connector J15 (located behind the hinged door); the MTS umbilical card is installed in J15 when the MTS is used for in-system testing.

b. *Left Hand Assembly*. The left hand assembly consists primarily of the left hand front panel and the left hand card cage containing three bays. When the left hand assembly is extended for maintenance, circuit cards are readily accessible from the center of the console.

c. *Center Section*. The center section has a modular construction for ease of maintenance. Major assemblies include crt assembly (A2A1), center section card cage (A2A2), deflection amplifier (A2AR1), high voltage power supply (A2PS1), and deflection amplifier power supply (A2PS2). The crt assembly is modularized and contains the crt, deflection coils, and tube shield. The center section card cage is hinged for access from the top when the center section is extended for maintenance. The deflection amplifier, high voltage power supply, and deflection amplifier power supply are also modular and are readily accessible for maintenance.

d. *Right Hand Assembly.* The right hand assembly consists primarily of the right hand front panel (A3A1), the right hand card cage (A3A2) containing three bays, and the VCS (A3A3). When the right hand assembly is extended for maintenance, circuit cards are readily accessible from the center of the console. The VCS is a separate unit and is console mounted for front panel access by the operator.

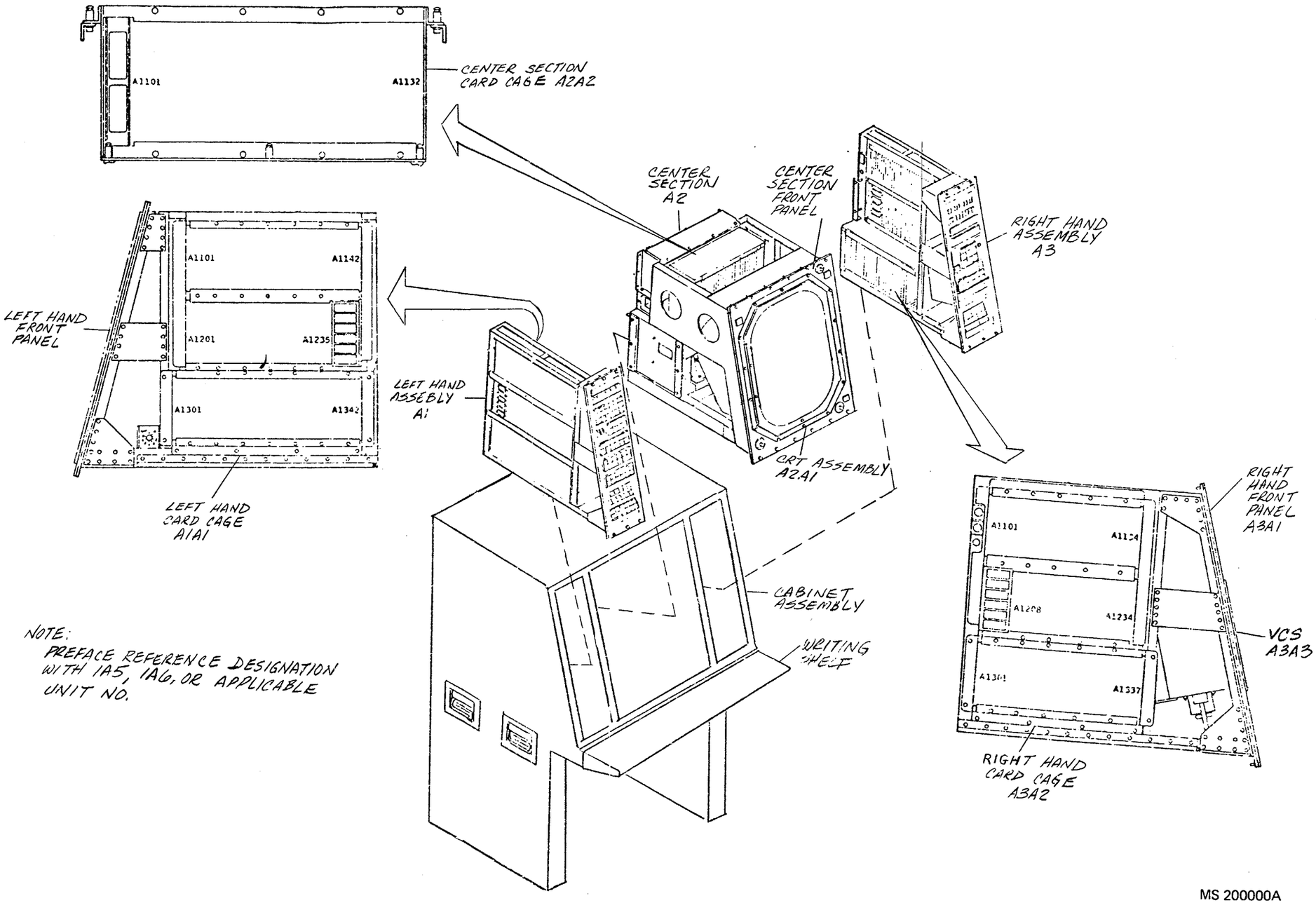


Figure 5-1. Display Console Major Units and Assemblies

Table 5-1. AN/TSQ-73 Major Equipment Cross-Reference

Ref des	Equipment	Part no.	Drawing
---	External Cable Set	10281356	10284717
1	Shelter	Multiple	---
	Intra-Shelter Cable Set	10282262	10284718
1A1	Equipment Rack	10284818	---
	Equipment Rack Cable Set	10284715	10284716
1A1A1	Rack 1 -	---	---
1A1A1A1	Radar Interface Equipment (RIE) II Panel	10282235	WL10282235
1A1A1A2	Radar Simulator Panel	10281406	WL10281406
1A1A1A3	Video Simulator Unit (VSU)	10281390	---
	VSU Wired Card Cage	10281348	WL10281348
1A1A1A4	Radar Integration Unit (RIU)	10281380	---
	RIU Bay 1 Wired Card Cage	10281387	WL10281387
	RIU Bay 2 Wired Card Cage	10281436	WL10281436
1A1A1A5	Video Processor Unit (VPU)	10281383	---
	VPU Bay 1 Wired Card Cage	10281388-13	WL10281388-2
	VPU Bay 2 Wired Card Cage	10281422	WL10281422
1A1A1A6	Radar/Simulator Unit (RSU)	10281614	---
	RSU Unit Wired Card Cage	10281615	WL10281615-2
1A1A1A7	1-Port 8K Core Memory	10281385	---
1A1A1A8	Wired Core Memory Assembly	10281386	WL10281386
1A1A2	Rack 2	---	---
1A1A2A1	Automatic Data Processor (ADP) Status and Control Panel	10284664	WL10284664
1A1A2A2	Data Comm Control Panel	10281439	WL10281439
1A1A2A3	4-Port 8K Core Memory	10281342	---
1A1A2A4	Wired Core Memory Assembly	10281397	WL10281397
1A1A2A5	Upper Modem (16/16)	10281616	---
	Upper Modem (10/16)	10284971	---
	Upper Modem Wired Card Cage	10281617-14	WL10281617-2
1A1A2A6	Data Comm Card Cage	10281619	---
	Data Comm Wired Card Cage	10281620	WL10281620
1A1A2A7	Lower Modem (4/16)	10281618	---
	Lower Modem (2/16)	10284830	---
	Lower Modem Wired Card Cage	10281650-14	WL10281650-2
1A1A2A8	4-Port 8K Core Memory	10281342	---
1A1A2A9	Wired Core Memory Assembly	10281397	WL10281397

Table 5-1. AN/TSQ-73 Major Equipment Cross-Reference
-Continued

Ref des	Equipment	Part no.	Drawing
1A1A3	Rack 3	---	---
1A1A3A1	Input/Output Unit (IOU)	10281344	
	IOU Wired Card Cage	10281394	WL10281394
1A1A3A2	Buffer Unit	10281437	---
	Buffer Unit Wired Card Cage	10281431	WL10281431
1A1A3A3	Central Processing Unit (CPU)	10281340	---
1A1A3A4	CPU Bay 1 Wired Card Cage	10281396	WL10281396
	CPU Bay 2 Wired Card Cage	10281430	WL10281430
1A1A3A5	4-Port 8K Core Memory	10281342	---
thru	Wired Core Memory Assembly	10281397	WL10281397
1A1A3			
1A1A4	RIE I Panel	10281406	WL10281409
1A1A5	ADP Interface Panel	10285182	WL10284551
1A1A6	Radar Interface Panel	10284817	WL10281445
1A2	Power Cabinet	10285434	WL10285257 10284916
1A3	Voice Communications Central (VCC)	10284822	---
1A3A1	RFI Filter Assembly	MIS-19560	---
thru			
1A3A39			
1A3A36	RFI Filter Assembly	MIS-19561	
thru			
1A3A39			
1A3A40	Communications Patching Panel	10281341	WL10281331
1A3A41	VCC Unit	10281355	WL10282276
1A3A41A1	VCC Control Panel	10281623	WL10281889
1A3A41A2	VCC Wired Card Cage	10281334-2	WL10281334-2
1A4	Maintenance Bench	10284823	---
1A5, 1A6	Display Console	10284960	10282130
1A7, 1A17	Data Display Group	10281361	10282122
1A8, 1A13	Magnetic Tape Unit (MTU)	10285127	---
	Wired MTU Assembly	10285128	WL10285128
	MTU Subassembly	10285138-2	WL10285138
1A9, 1A10	Voice Communications Station (VCS)	10281399-2	---
	Wired VCS Unit	10281625	WL10282287
	VCS Front Panel	10281630-2	WL10281630-2
	VCS Wired Card Cage	10282277	WL10282277

Table 5-1. AN/TSQ-73 Major Equipment Cross-Reference —Continued

Ref des	Equipment	Part no.	Drawing
1A11	Modular Collective Protection Equipment (MCPE) (when supplied)	10284806	
1A12	Keyboard Printer Unit (KPU)	10281464	
1A14	Module Test Set (MTS)	10281395	
	Wired MTS Assembly	10281449	WL10281449
	Test Set Probe Assembly	10285061	WL10281447
1A15	Environmental Control Panel (ECP)	10281477-2	WL10281477 10281565
2	Radar Junction Box (RJB)	10285092-1	WL10285092-3
3	Display Junction Box (DJB)	10284920	WL10284920
4	Motor Generator Set	10285058	
5	Diesel Engine Generator		

Table 5-2. Display Console Mayor Assembly Cross-Reference

Ref des	Equipment	Part no.	Drawing
1A5, 1A6	Display Console	10284960-7	10282130
	Cabinet Assembly	10284961-2	WL10284961-2
A1	Left-Hand Assembly	10284962-3	WL10281337
A1A1	Left Hand Card Cage	10281338-4	WL10281338-4
	Left Hand Front Panel	10281815-4	WL10281926
A2	Center Section	10284962	WL10281351
	Center Section Front-Panel/Chassis		WL10281351
A2A1	CRT Assembly	10281352	
A2A2	Center Section Card Cage	10281367-2	WL10281367-2
A2AR1	Deflection Amplifier	10281377-3	WL10281377-3
A2PS1	High Voltage Power Supply	10281379	WL10281379
A2PS2	Deflection Amplifier Power Supply	10281378	WL10281378
A3	Right Hand Assembly	10284964	WL10281389
A3A1	Right Hand Front Panel	10281813	WL10281927
A3A2	Right Hand Card Cage	10284595-4	WL10284595-4
A3A3	VCS	10281399	WL10281334-2
A4	Fan Assembly	10285005	
PS1, PS2	DC/DC Converter	126649-102	126649-300
PS3	DC/DC Converter	126650-103	126650-300
PS4	Variable Lamp Power Supply	10281467-3	10281469

Section II. OVERALL THEORY OF OPERATION

5-5. Overall Functional Description. (fig. 5-2). The display console provides display of tactical situation data consisting of radar returns and associated computer generated symbols, maps, lines, and alphanumeric characters. The display console allows operator participation in tactical data processing operations. In performing the functions stated, the display console interfaces externally with the RIE and the ADP through the display output unit (DOW) and the input/output exchange unit (IOX). The RIE supplies the radar video data, radar azimuth, radar range, and timing signals for the display console. The IOX interlinks the display console with the ADP using information and control lines. The DOU supplies the display console with synthetic data from the display refresh file in the ADP memory. The synthetic data consists of tracks, fire units, maps, etc. The DOU data transfer is monitored by fault and control lines. The display console consists of the following functional elements:

Alterable processor (AP)
Display controller (DC)
Display buffer (DB)
Video compressor (VC)
Display generator (DG)
Front panel logic
Computer buffer/C-BIT
Clocking circuit

The display console word formats plus a description of what is contained in the word formats is provided in section XV. Some word formats are included in the theory sections to emphasize and enhance functional descriptions.

a. *Alterable Processor*. The AP is a minicomputer which receives and processes all messages from the DOU The DOU messages (synthetic video) contains message type identification and data category codes. The messages are flagged by a new message bit which identifies the first word of the message and a parity signal which allows the message to be stored. The AP identifies the message type (track, fire unit. maps etc.) and category codes (hostile track. paired fire unit, etc.) and compares them with stored codes in the data file storage and address logic. The stored codes represent console operator category selections which are used to screen out messages not applicable to the particular console. The AP also deletes parts of messages which require generation of unselected features (e.g. track alphanumerics or velocity vectors). The data meeting all selection tests and falling within the selected console display area is transferred to the DB. If during message transfer the AP high speed input buffer reaches an almost full condition, the AP will send a buffer-almost-full signal to the computer buffer/C-BIT to temporarily inhibit the DOU from sending synthetic video. At the end of message transfer (EOF) the AP will receive, process, and transfer console status information to and from the front panel logic and the computer buffer/C-BIT.

b. *Display Controller.* The DC is also a minicomputer which reflects a similar command structure and arithmetic and logical operations as the AP. The DC synchronizes AP operation with the DG for display of synthetic video and also synchronizes the VC operation with the DG for display of radar video. The DC stored program accepts the various messages (ARO. fire unit. geographic map track, etc.) from the DB and examines the messages to extract required data. The data consists of an ASCII code for characters and special symbols along with positioning data which is made available to the DG. The DC also monitors the DG to determine when a function is complete. The VC is monitored periodically by the DC to determine if sweep information is ready to be transferred to the DG. When sweep information is available, the DC positions the DG to radar center and supplies sine and cosine information from the RIE. This process interleaves the radar sweeps with the synthetic data received through the DB.

c. *Display Buffer* The DB provides storage for AP synthetic data at the A P output rate and sends the data to the DC as required. The DB storage is large enough to continue receiving data from the AP while the DC is stopped for radar data display.

d. *Video Compressor.* The VC provides compression of radar video information from the RIE to the DG. Compressing the time required for radar video display allows the required quantity of synthetic data to be multiplexed on the crt without loss of radar video. The video compressor operates in an input and output mode and processes eight channels of radar video signals. The front panel logic selects which combination of radar video signals are to be processed and controls the brightness of each video signal. During the input mode, the video compressor converts the video from analog to digital form and clocks the selected video into a memory channel at a 1-MHz rate. When the memory channel has received all video for the specified range, the video compressor changes into the output mode. During the output mode, the video is clocked out of the memory channel at a 5-MHz rate to the DG.

e. *Display Generator.* The function of the DG is to paint lines, characters, and radar sweeps on the crt. The display generation process is controlled by the DC. The radar video and processed synthetic data is displayed on the upper portion of the crt while the lower portion of the crt displays detailed information on tracks and fire units. The DG accepts ASCII characters and special symbols

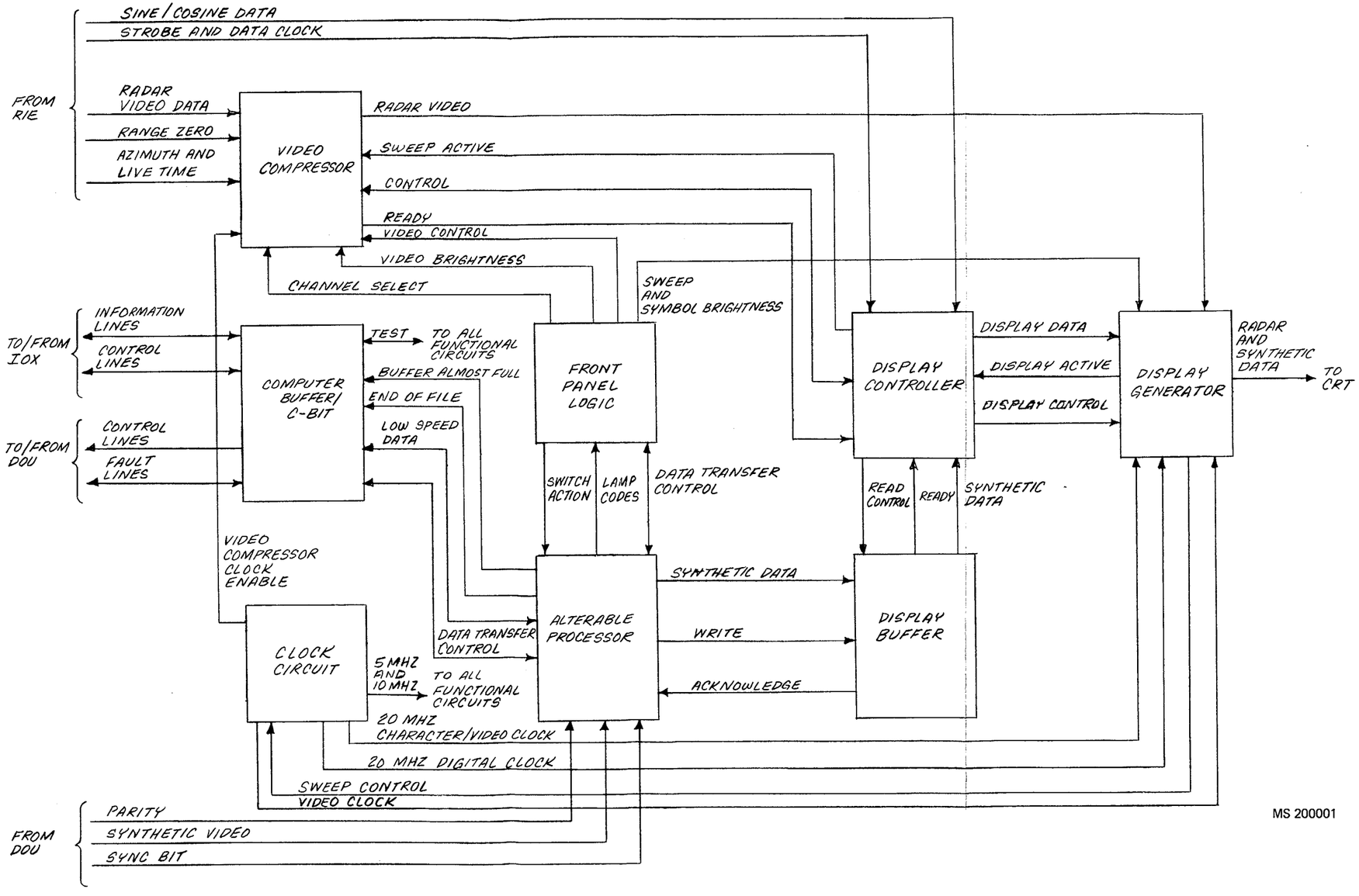


Figure 5-2. Display Console Overall Functional Block diagram

from the DC and converts the character/symbol codes into differential analog voltages for display on the crt. Line and sweep information supplied by the DC is also converted to differential analog voltages for display on the crt. Video is displayed using 10 video channels, of which 9 are used for synthetic data with individual intensity control supplied by the front panel logic. The other channel is used for radar video.

f. *Front Panel Logic.* The front panel logic detects operator switch actions and encodes and transfers the data to the AP. The front panel logic also receives lamp code information from the AP and lights the appropriate indicators. The front panel switch actions and force stick increments are binary coded (switch function code) and are read and processed by the AP using the switch function code. The AP will report to the ADP at the end of the display refresh cycle any switch action detected. Any time the AP is to send or receive data to or from the front panel logic, a command phase is initiated. The purpose of the command phase is to notify the front panel logic as to which type of data is to be transferred. The command phase sets up the data transfer control logic and enables the appropriate data paths. All data transfer within the front panel logic is serial. Lamp data is the only type of data that is transferred to the front panel logic from the AP. Lamp data transfer is performed using an input and output mode of operation. During the input mode, the lamp data lights or turns off the appropriate switch-associated indicators on the front panels, sends lamp status information to the AP, and updates range signals to the VC and DC. During the output mode, the new lamp data from the AP, consisting of a lamp group code contained in the command word, is serially loaded into the front panel logic.

g. *Computer Buffer/C-BIT.* The computer buffer/C-BIT provides timing and control signals for receiving and transferring data between both' the IOX and the DOU. This includes the interface control to the AP. The computer buffer/C-BIT also performs built-in testing of the display console sections during the maintenance mode.

(1) DOU interface. During the DOU interface, the computer buffer/C-BIT supplies the necessary control signals from the AP to the DOU to prepare (reset) the DOU for data refresh file transfer and initiate (request) the data refresh file transfer cycle. The computer buffer/C-BIT also monitors the AP and DOU for data transfer faults and completion of data transfer by the DOU. The faults consist of the following: inhibit, which indicates that the AP high speed buffer is almost full; memory time out (MTO), which indicates that the DOU is unable to access memory for the data refresh file; memory overrun (MO), which indicates that the AP was unable to receive the data refresh file in 50 ms; and data parity (DP) and control word parity check (CWP), which indicates an error in parity. The inhibit line is also used to indicate the EOF to the DOU.

(2) IOX interface. The IOX interface consists of nine information lines (including parity) and four control lines which consist of enable, command, indicator, and request. The feedback (console status) and test data is transferred over the information lines and is stored in the computer buffer/C-BIT as 32-bit words. The data is transferred in 8-bit bytes. The console status or feedback data from the AP consists of three 32-bit words and contains console number and front panel logic information. Test data is transferred to and from the computer buffer/C-BIT by ADP-generated output from register (OFR) and input to register (ITR) operations. The OFR (ADP requesting test) contains data, control codes, and identification of a BIT test point to be sampled. After the computer buffer/C-BIT samples the test point (at the unit specified by the control code), a 16-bit resultant is obtained. The ITR (ADP requesting test data back) contains the 16-bit test sample and 16 least significant bits (LSB)s of the last OFR. If the test is not completed, the computer buffer/C-BIT will not respond to the ITR operation.

(3) Control lines. The computer buffer/C-BIT control lines provide communication between the ADP and the display console for initialization (command/ indicator), mode of operation (command/indicator), and transfer of data (enable/request). The EOB (end of block) operation uses only the command line.

h. *Clocking Circuit.* The clocking circuit contains the functional elements required to provide all clock timing for the display console functional sections. The clocking circuit generates and supplies 5-MHz and 10-MHz clock trains to the display console functional sections. The 20-MHz clock is generated and supplied directly to the video subsystem as a video clock and to the line and character generators and deflection subsystem as a character/video clock. Upon receiving a video sweep control signal from the DG, a 20-MHz digital clock is supplied back to the DG. The VC receives a 5-MHz VC clock.

i. *Display Console Data and Control Timing Interfacing.* The following paragraphs describe the basic philosophy and the general implementation of the interface repertoire between the display console and the IOX and DOU. Refer to figure 5-3 for interfacing signal flow. The data and control communication between the display console primary functional assemblies (computer buffer/C-BIT, AP, and front panel logic), which is an adaptation of the console interface, is then described. The IOX data controls the display console mode of operation (normal operation, test mode, reset, etc.). During normal operation, the IOX places the display console under control of the DOU which provides direct access to computer memory in order to receive and process the high-speed synthetic data required to refresh the display. Additional lines are available between the console and the DOU to provide mutual status indications.

(1) IOX interface. The IOX/display console interface employs two pairs of control signals: the command/indicator signals and the request/enable signals. The command line is bussed to a maximum of eight consoles and is always accompanied by a console address byte. The particular command, which is defined by the second byte (referred to as the control byte), is a computer-programmed function and indicates the initiation or termination of a console operating mode. The indicator signal, which is bussed to a maximum of eight consoles, is a console acknowledgment that the command and accompanying data has been received. Refer to the detailed description of the computer buffer/C-BIT timing and control logic for context of the interface command data. The request line to the IOX is activated when the computer buffer/C-BIT output register contains data to be transmitted. The stored information may be either console status data or BIT sample data. The request is supplied over one of eight lines, manually selected at the particular console. The IOX responds to the request with an enable when the IOX is prepared to accept the data. In a similar manner for the command line, the enable is accompanied by an address byte to ensure that the requesting console will respond.

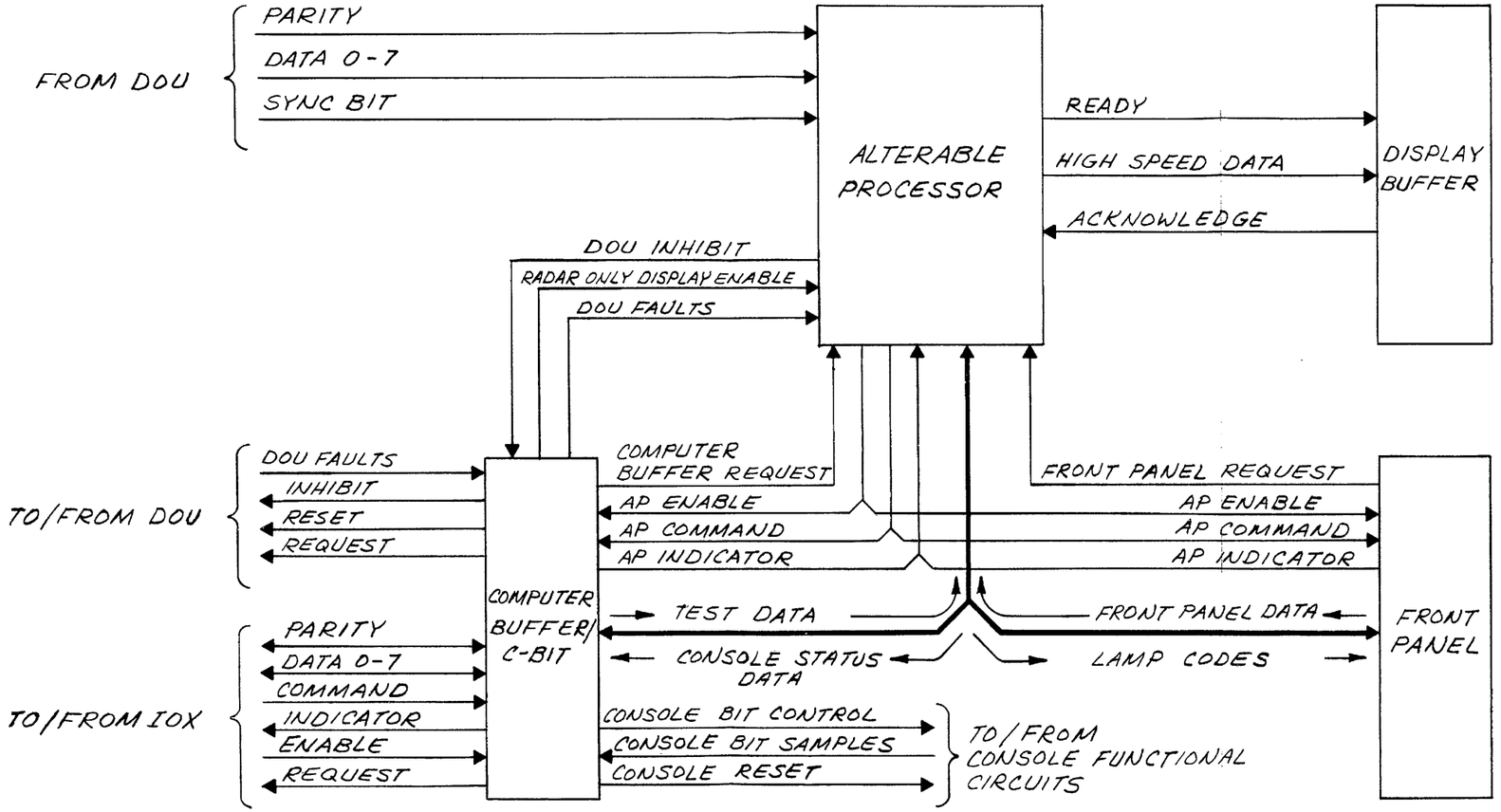
(2) DOU interface. During normal operation, the DOU supplies synthetic data to the AP for up to 47 ms of each 50 ms display refresh cycle. The data is provided as 7-bit bytes plus parity, with the initial byte of each new word identified by a sync bit. The DOU status is monitored by the DOU fault inputs. The reset signal is utilized to initialize the DOU whenever the console logic is reset. The inhibit signal halts DOU data transmission after the complete refresh file has been received or when the AP input buffer approaches its storage capacity. The request line is utilized to initiate each 50-ms display refresh cycle.

(3) Console internal interfacing. The console internal interfacing is an adaptation of the external interface, with the AP acting as the IOX and the computer buffer/C-BIT and front panel logic acting as the bussed devices. A 1 6-bit low speed bus is provided for control word and data communication. The AP command line is utilized in conjunction with the data lines to address the bussed device and indicate the direction of subsequent data transmission and the type of data to be transmitted. The computer buffer/C-BIT or the front panel logic acknowledges the AP command with the AP indicator signal. When the addressed device is prepared to respond to the command, a request is sent to the AP. The AP enable signal then initiates data transmission.

(4) Initialization. When power is applied to the console, the console logic is placed in a master reset condition and a reset signal is applied to the DOU. When the power-on time is completed, the master reset is removed, and the AP commences a programmed initialization routine. This routine clears the AP scratchpad memory. During this time, the DOU is idling and the console is in the radar only display mode.

(5) Display refresh cycle. When the IOX is prepared to commence normal system operation, a manual master reset will usually be generated to initialize the ADP and all associated devices. The master reset is indicated by simultaneously active signals on the CPU command and enable lines. The master reset initializes all pertinent console and DOU logic with the exception of the radar only display mode logic. At this time, the IOX may interrogate the console status by means of an OFR/ITR sequence to ensure that the console is prepared to accept and process display data. The ADP is programmed to supply a DEV-2 (reset) operation command. This terminates the console radar only display mode. The ADP then supplies a DEV-1 (normal) operation to one of the online consoles. The computer buffer/C-BIT then activates the request line to the DOU, initiating the 50-ms display refresh cycle to all online consoles. The DOU will commence to forward the series of synthetic data messages constituting the display refresh file. The AP will screen the input data for display ability, process the data as required, and forward the information to the display buffer. The DOU inhibit indicates either the detection of an EOF message or an input data parity error. For either of these events, the console activates the DOU inhibit line, terminating display data transmission, and enters the console status mode. The AP then initiates the required command/ indicator and request/enable dialogue to obtain front panel data in order to construct the console status word. The AP outputs control words and lamp addressing data to the front panel logic. The front panel logic returns switch, lamp, keyboard, force stick, variable range, and time-to-go data. The data is reformatted and supplied to the IOX through the computer buffer/C-BIT as the console status message. When this transmission is completed, the DOU inhibit signal is released. When all consoles have released the DOU inhibit, the DOU commences a new refresh cycle. The DOU inhibit is also activated when the AP memory approaches its maximum capacity. This memory is a first-in, first-out (FIFO) device and input data would overwrite stored data if the AP substantially lagged the input data rate. When the memory is sufficiently emptied, the DOU inhibit is released and normal display refresh data processing is permitted to proceed.

(6) Maintenance mode. The computer buffer/C-BIT is mechanized to exercise various portions of the console logic and supply BIT sample data to the IOX for fault isolation. A DEV-3 operation instruction places the console in the maintenance mode. An OFR instruction indicates the type of test, the portion of the console to be tested, and the data content to be used in the test. The BIT sample resultant of the test is returned and stored in the computer buffer/C-BIT output register. An ITR operation instruction then transfers the BIT sample to the IOX.



MS200002

Figure 5-3. Display Console Primary Data and Control Lines Block Diagram

5-6. Logic Theory Presentation. The following subparagraphs describe the philosophy and techniques utilized to illustrate and support the console logic theory. The detailed logic diagrams are located in volume 2. These are supplemented by functional block diagrams, timing diagrams, and tabular data which are integrated into the logic theory.

a. *Functional Logic Groups.* As previously described, the display console is divided into six primary functional and physical entities: the AP, DB, DC, DG, front panel, and computer buffer/C-BIT. Each prime functional entity is further divided into secondary functional logic groups. For purposes of convenient logic analysis, several of these secondary functional logic groups (the AP and DC timing and control and AP high speed input buffer) are further broken down into discrete logic groups which can be assigned unique logical identities. Each of these final levels of logic groups, referred to as primary functional subassemblies, is represented by a logic diagram which may comprise one or several sheets. Each primary functional subassembly is described under a prime heading and is supported by a functional block diagram. For those circuits that perform a sequential and predictable logic function (timing and control), detailed timing diagrams are provided. For those circuits whose functions significantly vary with the context of input data or control signals (instruction decoding), tabular information is included.

b. *Functional Block Diagrams.* The intent of the functional block diagrams is to provide simplified illustrative support for the theoretical prose, emphasizing functional flow and descriptive signal connotation as opposed to the logic diagrams which necessarily portray individual signal flow and unique mnemonic connotation. The block diagrams are therefore a tool for understanding the operation of the device and will facilitate application of the logic diagrams when isolating a fault. The block diagrams collect various related functional elements (gates, flip-flops, multiplexers (muxs), etc.) into functional blocks. These functional blocks are directly related to the broken-line enclosed areas reflected on the associated logic diagrams. In addition, the block diagrams contain the primary input and output mnemonics for each functional block. For the purpose of simplicity, both outputs (flip-flop J and K) are only shown when logically critical and bussed lines are used, where practical, to illustrate the flow signals. Clock inputs and initialization signals are not shown.

c. *Signal Names.* The descriptive signal names are usually a direct translation of the particular mnemonic. Due to the limitation of 7-bit mnemonically significant permutations, the mnemonics often have no obvious relationship with the descriptive connotation. The mnemonic can, however, facilitate evaluation of the nature of the signal. The first letter is indicative of the primary functional assembly from which the signal emanated, as follows:

A = Alterable processor
K = Display buffer or display controller
V = Video compressor
C = Display generator
R = Front panel
L = Computer buffer/C-BIT

The final two letters usually indicate the output element which then is indicative of the signal's logic significance, as follows:

Final mnemonic letter	Source element	Logic significance
J or JQ	Flip-flop J output	High when set
K or KQ	Flip-flop K output	High when reset
A	AND gate output	Low when enabled
O	OR gate output	High when enabled
OV	Inverted AND gate output	High when active
AV	Inverted K gate output	Low when active
0T-9T	Decoder outputs output	Low for active
1V-2V	Binary counter outputs	High when active
0E-3E	Shift register outputs	High when active

5-7. Circuit Card and Key Signal Lookup Tables. Circuit card and key signal Lookup tables provide figure references to functional logic diagrams. These Lookup tables permit rapid access for locating circuit areas corresponding to circuit card locations or when signal mnemonics are known.

a. *Circuit Card Lookup.* Tables 5-3 thru 5-5 are circuit card locations for the left hand, center section, and right hand card cages, respectively. The circuit card Lookup table provides figure and sheet references to logic diagrams when a circuit card at a particular location is suspect. Since a circuit card may be used for different functional applications, multiple references may be provided for a single circuit card. The circuit card Lookup

table also provides information on whether a circuit card is testable by the MTS.

b. *Key Signal Lookup.* Tables 5-6 thru 5-8 are key signal Lookup listings for the left hand, center section, and right hand assemblies, respectively. Key signals are interconnecting signals going between either a physical assembly or a functional circuit area covered by a troubleshooting diagram. Key signals are listed in alphabetical/numerical order (letters precede numbers). The columns under the distribution heading list connectors, pin numbers, test points, and foldout numbers with sheet numbers. They appear as follows:

Connector	Pin number	Test point	Foldout and sheet
*J1214	54	25A	FO1400

The * symbol indicates the source of the signal. The foldout and sheet number is in code form: FO refers to a Volume 3 foldout, the first two digits (14) represent the foldout number, and the last two digits (00) represent the sheet. When a foldout consists of only one sheet, the last two digits are 00. The connector designations are represented by a J.

Table 5-3. Left Hand Assembly Card Location Index

Card Slot	Fig	Sh	Module test set testable
A1104	FO-49		YES
	FO-1	2	
A1105	FO-51		YES
	FO-52	1	
	FO-52	4	
A1106	FO-54	2	NO
A1107	FO-49		YES
	FO-50		
A1108	FO-49		YES
	FO-50	2	
	FO-51		
A1109	FO-49		YES
	FO-51		
A1110	FO-9	2	YES
	FO-50	2	
	FO-51		
	FO-54	2	
A1111	FO-49		YES
	FO-50	2	
	FO-51		
A1112	FO-48	1	YES
	FO-49		
	FO-50	2	
A1115	FO-49		YES
	FO-50	2	
	FO-51		
	FO-52	1	
A1116	FO-47		YES
	FO-50	2	
	FO-50		
	FO-52	1	
	FO-53		
A1117	FO-5		YES
	FO-48	1	
	FO-50	1	
	FO-50	2	
	FO-51		
	FO-52	1	
	FO-53		
	FO-1	2	
A1118	FO-47		YES
	FO-49		
	FO-50	2	
	FO-51		
	FO-52	3	
	FO-53		
A1119	FO-5		YES
	FO-47		
	FO-49		
	FO-50	1	
	FO-50		
	FO-51		
	FO-52	1	
	FO-53		
	FO-54	2	
A1120	FO-47		YES
	FO-48	1	
	FO-49		
	FO-50	1	
	FO-50	2	
	FO-51		
	FO-52	1	
	FO-53		
A1122	FO-4	1	YES
	FO-6	2	
	FO-6	3	
	FO-49		
	FO-50	2	
	FO-51		

Table 5-3. Left Hand Assembly Card Location Index - Continued

Card Slot	Fig	Sh	Module test set testable
	FO-52	1	
	FO-52	2	
A1123	FO-47		YES
	FO-52		
A1124	FO-47		YES
	FO-48	1	
	FO-52	1	
A1125	FO-48	1	NO
	FO-48	2	
	FO-49		
	FO-50		
A1126	FO-49		YES
	FO-50	2	
	FO-51		
A1127	FO-48	1	YES
	FO-50	1	
	FO-50	2	
	FO-53		
A1128	FO-48	1	YES
	FO-50	1	
A1129	FO-48	1	YES
	FO-50	1	
A1130	FO-50	2	YES
	FO-51		
	FO-52	1	
A1131	FO-48	1	YES
	FO-49		
	FO-51		
A1132	FO-48	1	YES
	FO-49		
	FO-50	2	
	FO-51		
	FO-52	1	
A1133	FO-48	1	YES
	FO-49		
	FO-50	2	
A1134	FO-9	2	YES
	FO-41	3	
	FO-47		
	FO-48	1	
	FO-49		
	FO-50	2	
	FO-51		
	FO-52	1	
	FO-52	3	
A1135	FO-10		YES
	FO-48	1	
	FO-49		
	FO-50	2	
	FO-52		
A1136	FO-48	1	NO
	FO-48	2	
A1137	FO-48	1	NO
A1138	FO-48	1	NO
A1139	FO-48	1	NO
A1140	FO-48	1	NO
A1142	FO-48	1	NO
A1204	FO-41	2	YES
	FO-41	3	
	FO-44	2	
A1205	FO-41	3	YES
	FO-49		
	FO-51		
	FO-52	1	
	FO-1	2	
A1206	FO-5		YES

Table 5-3. Left Hand Assembly Card Location Index - Continued

Card Slot	Fig	Sh	Module test set testable
	FO-10		
	FO-11		
	FO-50	2	
	FO-52	3	
	FO-53		
A1207	FO-15		YES
	FO-41	4	
	FO-52	2	
A1208	FO-6	1	YES
	FO-44	2	
	FO-45	2	
	FO-52	2	
A1209	FO-44	2	YES
	FO-49		
	FO-51		
A1210	FO-1	2	YES
	FO-5		
	FO-48	2	
	FO-53		
A1211	FO-47		NO
	FO-50		
	FO-51		
A1212	FO-6	1	YES
	FO-6	3	
	FO-9	2	
	FO-10		
	FO-12		
	FO-14	1	
	FO-15		
	FO-44	2	
	FO-45	2	
	FO-50	2	
	FO-52	4	
A1213			YES
	FO-9	1	
	FO-9	2	
	FO-11		
	FO-14	2	
	FO-52	4	
A1214	FO-4	1	YES
	FO-5		
	FO-6	1	
	FO-9	1	
	FO-10		
	FO-12		
	FO-14	1	
	FO-14	2	
A1215	FO-4	1	YES
	FO-5		
	FO-6	1	
	FO-9	2	
	FO-11		
	FO-14	1	
	FO-14	2	
	FO-52	1	
A1216	FO-5		YES
	FO-6	1	
	FO-6	3	
	FO-9	1	
	FO-9	3	
	FO-11		
	FO-12		
	FO-14	1	
	FO-14	2	
	FO-41	4	
	FO-44	2	
A1217	FO-6	1	YES
	FO-6	3	

Table 5-3. Left Hand Assembly Card Location Index - Continued

Card Slot	Fig	Sh	Module test set testable
	FO-9	2	
	FO-10		
	FO-12		
	FO-14	1	
	FO-14	2	
	FO-41	4	
	FO-44	2	
A1218	FO-2		YES
	FO-3		
	FO-4	1	
	FO-4	2	
	FO-5		
	FO-6	1	
	FO-9	2	
	FO-11		
	FO-12		
	FO-13		
	FO-14	2	
	FO-15		
	FO-41	3	
	FO-44	2	
	FO-52	1	
	FO-53		
	FO-54	2	
A1219	FO-6	1	YES
	FO-9	2	
	FO-11		
	FO-12		
	FO-14	1	
	FO-14	2	
	FO-54	2	
A1220	FO-1	2	YES
	FO-5		
	FO-9	2	
	FO-10		
	FO-11		
	FO-12		
	FO-14	1	
	FO-14	2	
	FO-41	4	
A1221	FO-4	1	YES
	FO-12		
	FO-14	1	
	FO-14	2	
	FO-44	2	
A1222	FO-41	3	NO
	FO-41	4	
	FO-44	2	
	FO-45	2	
	FO-47		
	FO-48		
	FO-50	2	
	FO-51		
	FO-54	2	
A1223	FO-11	YES	
	FO-51		
A1224	FO-4	1	YES
	FO-4	2	
	FO-6	3	
	FO-12		
	FO-14	1	
	FO-14	2	
	Fo-49		
	FO-51		
A1225	FO-4	1	YES
	FO-5		
	FO-9	1	
A1226	FO-3		YES

Table 5-3. Left Hand Assembly Card Location Index - Continued

Card Slot	Fig	Sh	Module test set testable
	FO-9	1	
	FO-12		
	FO-14	1	
A1227	FO-9	1	YES
	FO-12		
	FO-14	1	
	FO-50		
	FO-52	1	
A1228	FO-5		
	FO-9	1	YES
	FO-14	1	
	FO-50	2	
A1229	FO-1	2	YES
	FO-4	1	
	FO-11		
A1230	FO-2		YES
	FO-3		
	FO-12		
	FO-52	2	
A1231	FO-2		YES
	FO-41	3	
A1232	FO-2		YES
A1233	FO-4	1	YES
	FO-4	2	
	FO-5		
	FO-10		
	FO-52	1	
	FO-54	2	
A1234	FO-4	1	YES
	FO-4	2	
	FO-5		
	FO-12		
	FO-51		
	FO-53		
A1235	FO-1	2	YES
	FO-5		
A1302	FO-41	3	NO
A1303	FO-41	2	NO
	FO-44	2	
A1304	FO-41	3	NO
	FO-44	2	
A1305	FO-41	3	NO
	FO-44	2	
A1306	FO-41	3	NO
	FO-44	2	
A1307	FO-41	4	NO
	FO-44	2	
A1308	FO-6	3	NO
	FO-8	1	
	FO-41	4	
	FO-44	2	
	FO-47		
	FO-49		
	FO-50		
	FO-51		
	FO-54	2	
A1311	FO-1	2	
	FO-10		
	FO-44		
A1312	FO-6	1	NO
	FO-6	3	
	FO-14	2	
	FO-15		
A1313	FO-6	3	NO
	FO-8	2	
	FO-14		
	FO-6	3	
A1314	FO-6	2	NO

Table 5-3. Left Hand Assembly Card Location Index - Continued

Card Slot	Fig	Sh	Module test set testable
	FO-8	2	
A1315	FO-6	2	NO
		1	
	FO-8	1	
A1316	FO-6	1	NO
	FO-8	1	
A1317	FO-7	2	NO
	FO-14	2	
A1318	FO-7	2	YES
	FO-11		
A1319	FO-7	2	YES
A1320	FO-7	2	NO
A1321	FO-7	2	NO
A1322	FO-7	2	No
A1323	FO-7	2	NO
A1324	FO-7	2	NO
A1325	FO-4	1	NO
	FO-7		
A1326	FO-9	1	NO
A1327	FO-52	2	YES
A1328	FO-9	2	YES
	FO-52	2	
A1329	FO-9	1	NO
A1330	FO-9	1	NO
A1331	FO-8	2	YES
	FO-52	1	
	FO-52	2	
A1332	FO-5		YES
	FO-9	1	
	FO-12		
A1333	FO-9	1	NO
A1334	FO-13		NO
A1335	FO-2		NO
A1335	FO-2		YES
	FO-3		
	FO-41	3	
A1338	FO-1	2	YES
	FO-3		
	FO-4		
	FO-4	2	
	FO-9	1	
		1	
	FO-54	2	
A1339	FO-1	2	Yes
	FO-3		
	FO-4	1	
	FO-4	2	
A1340	FO-1	2	YES
	FO-3		
	FO-4	1	
	FO-4	2	
	FO-54	2	
A1341	FO-1	2	YES
	FO-5		
	FO-52	2	
A1342	FO-1	2	YES
	FO-47		

Table 5-4. Center Assembly Card Location Index

Card Slot	Fig	Sh	Module test set testable
A1101	FO-37	1	NO
	FO-37	2	
	FO-38	2	
	FO-39	2	
	FO-40		
	FO-50		
	FO-54	1	
A1102	FO-1	1	YES
A1103	FO-1	1	YES
A1104	FO-1	1	YES
A1105	FO-1	1	YES
A1106	FO-1	1	YES
A1107	FO-50	2	YES
A1109	FO-45	1	NO
A1110	FO-37	2	NO
A1112	FO-37	1	NO
	FO-54	1	NO
A1113	FO-37	2	NO
A1114	FO-37	3	NO
	FO-52	3	
A1115	FO-37	4	NO
	FO-51	4	
	FO-52	4	
A1116	FO-37	4	NO
A1117	FO-37	4	NO
A1119	FO-40	2	NO
A1121	FO-40	2	NO
A1123	FO-40	1	NO
	FO-52	4	
A1124	FO-38	3	NO
A1125	FO-38	3	NO
A1126	FO-38	2	NO
	FO-52	3	
A1127	FO-37	1	NO
	FO-38	2	
A1129	FO-39	2	NO
A1132	FO-39	2	NO

Table 5-5. Right Hand Assembly Card Location Index

Card Slot	Fig	Sh	Module test set testable
A1101	FO-2	1	YES
	FO-34	1	
	FO-36	1	
	FO-45	1	
	A1102	FO-26	2	YES
	FO-34	2	
	FO-35		
	FO-36	2	
	FO-36	3	
	FO-45	2	
A1103	FO-26	1	YES
	FO-26	2	
	FO-32		
	FO-34	2	
	FO-35		
	FO-36	1	
	FO-36	2	
	FO-36	3	
A1104	FO-32		YES

Table 5-5. Right Hand Assembly Card Location Index - Continued

Card Slot	Fig	Sh	Module test set testable
	FO-34	2	
	FO-35		
	FO-36	1	
	FO-36	2	
	FO-36	3	
A1105	FO-32		YES
	FO-33	1	
	FO-34	2	
	FO-35		
	FO-36		
	FO-36	1	
	FO-36	2	
A1106	FO-32	3	YES
	FO-33		
	FO-33	1	
	FO-34	2	
	FO-35	2	
	FO-36		
	FO-36	1	
	FO-54	2	
A1107	FO-32	3	YES
	FO-34	3	
	FO-35		
	FO-36	2	
	FO-36		
	FO-36	1	
A1108	FO-35	3	YES
A1109	FO-		YES
	FO-	2	
	FO-		
	FO-	2	
	FO-	2	
	FO-	3	
A1110	FO-	2	YES
	FO-36	1	
	FO-36	2	
	FO-36	3	
A1111	FO-23		YES
	FO-26	1	
	FO-34	2	
	FO-35		
A1112	FO-32		YES
	FO-33	2	
	FO-34	2	
	FO-35		
	FO-36	1	
		2	
	FO-36		
	FO-36	3	
	FO-54	3	
A1113	FO-32		YES
	FO-33	2	
	FO-35		
	FO-36	1	
	FO-36	2	
	FO-36	3	
A1114	FO-32		YES
	FO-36	3	
	FO-41	1	
	FO-42		
	FO-44	1	
	FO-45	2	
A1115	FO-35		YES
	FO-36	1	
A1116	FO-21		YES
	FO-22		
	FO-29		
	FO-30	1	
	FO-32		

Table 5-5. Right Hand Assembly Card Location Index - Continued

Card Slot	Fig	Sh	Module test set testable
	FO-35		
	FO-36	1	
	FO-36	3	
	FO-45	2	
A1117	FO-43		NO
	FO-45	1	
A1118	FO-30	1	YES
	FO-35		
	FO-43		
	FO-52	3	
A1119	FO-30	1	
	FO-52	2	YES
A1120	FO-29		YES
	FO-30	1	
	FO-43		
	FO-45	2	
A1121	FO-29		YES
	FO-45	1	
	FO-45	2	
A1122	FO-21		YES
A1123	FO-21		YES
A1124	FO-22		YES
	FO-32		
	FO-43		
	FO-46		
A1125	FO-35		YES
	FO-45	2	
A1126	FO-45	2	YES
A1127	FO-26	1	YES
	FO-26	2	
	FO-34	2	
	FO-35		
	FO-41	1	
	FO-45	2	
A1128	FO-19	2	YES
	FO-24		
	FO-26	1	
	FO-26	2	
	FO-41	1	
	FO-42		
	FO-43		
	FO-44	1	
	FO-45	2	
	FO-52	2	
A1129	FO-16	2	YES
	FO-16	4	
	FO-23		
	FO-24		
	FO-28		
	FO-41	1	
	FO-42		
	FO-43		
	FO-45	2	
A1130	FO-22		YES
	FO-23		
	FO-36	1	
	FO-41	1	
	FO-44	1	
	FO-46		
A1131	FO-41	1	NO
	FO-42		
	FO-43		
	FO-44	1	
	FO-45	1	
	FO-45	2	
	FO-46		
	FO-54	3	
A1132	FO-22		YES

Table 5-5. Right Hand Assembly Card Location Index - Continued

Card Slot	Fig	Sh	Module test set testable
	FO-45	2	
	FO-46		
	FO-53		
A1133	FO-22		YES
	FO-36	1	
	FO-41	1	
	FO-42		
	FO-43		
	FO-44	1	
	FO-45	1	
	FO-45	2	
	FO-46		
A1134	FO-22		YES
	FO-28		
	FO-41	1	
	FO-42		
A1209	FO-19	2	YES
	FO-52	2	
A1210	FO-19	2	YES
	FO-52	2	
A1211	FO-24		YES
	FO-27		
	FO-52	2	
	FO-52	3	
A1212	FO-32		YES
	FO-34		
	FO-54	3	
A1213	FO-19	1	YES
	FO-29		
	FO-34	2	
	FO-35		
A1214	FO-19	1	YES
	FO-26	1	
	FO-29		
A1215	FO-24		YES
	FO-26	1	
	FO-29		
A1215	FO-19	1	YES
	FO-26	1	
	FO-29		
	FO-34	2	
A1217	FO-19	2	YES
	FO-25	1	
	FO-36	1	
A1218	FO-22		YES
	FO-24		
A1219	FO-21		YES
	FO-22		
	FO-28		
A1220	FO-22		YES
	FO-23		
	FO-28		
A1222	FO-32		NO
	FO-34	2	
	FO-36	1	
	FO-54	3	
A1223	FO-16	2	YES
	FO-22		
	FO-23		
	FO-25	1	
	FO-26	1	
	FO-26	2	
	FO-44	1	
A1224	FO-19	1	YES
	FO-19	2	
	FO-22		
	FO-24		
	FO-26	1	

Table 5-5. Right Hand Assembly Card Location Index - Continued

Card Slot	Fig	Sh	Module test set testable
	FO-26	2	
	FO-36	2	
	FO-42		
A1225	FO-16	2	YES
	FO-16	4	
	FO-19		
	FO-22		
	FO-23		
	FO-24		
	FO-26	1	
	FO-26	2	
	FO-54	3	
A1226	FO-16	2	YES
	FO-16	4	
	FO-19	2	
	FO-24		
	FO-25	1	
	FO-26	1	
	FO-26	2	
	FO-27		
	FO-28		
	FO-30	2	
A1227	FO-16	2	YES
	FO-16	4	
	FO-19	1	
	FO-19	2	
	FO-22		
	FO-24		
	FO-25	1	
	FO-26	1	
	FO-26	2	
A1228	FO-16	2	YES
	FO-19	2	
	FO-22		
	FO-24		
	FO-26	1	
	FO-26	2	
	FO-28		
A1229	FO-16	4	YES
	FO-19	1	
	FO-22		
	FO-23		
	FO-24		
	FO-26	1	
	FO-26	2	
	FO-28		
	FO-44	1	
A1230	FO-16	2	YES
	FO-16	4	
	FO-20		
	FO-21		
	FO-22		
	FO23-		
	FO-25	2	
	FO-26	1	YES
	FO-26	2	
	FO-28		
	FO-42		
	FO-52	2	
	FO-53		
	FO-54	3	
A1231	FO-32		NO
	FO-43		
	FO-45	1	
A1232	FO-20		YES
	FO-32		
	FO-45	1	
	FO-53		

Table 5-5. Right Hand Assembly Card Location Index - Continued

Card Slot	Fig	Sh	Module test set testable
A1233	FO-19	1	YES
	FO-19	2	
	FO-20		
	FO-23		
	FO-26	2	
A1234	FO-18	1	
	FO-19	2	YES
	FO-20		
	FO-22		
	FO-23		
	FO-24		
	FO-25		
	FO-26	1	
	FO-26	2	
	FO-30	2	
	FO-42		
	FO-44	1	
	FO-52	2	
A1302	FO-31		NO
	FO-34	2	
A1304	FO-31		NO
A1305	FO-33	1	NO
A1306	FO-33	2	NO
A1307	FO-32		NO
	FO-33	2	
A1308	FO-33	2	NO
A1309	FO-33	3	NO
A1310	FO-32		NO
	FO-33	3	
A1311	FO-30	2	NO
A1312	FO-30	2	NO
A1313	FO-25	2	NO
A1314	FO-22		YES
	FO-52	3	
A1315	FO-19	1	NO
A1316	FO-19	1	NO
	FO-19	2	
A1317	FO-16	1	NO
	FO-16	4	
	FO-27		
A1318	FO-17	1	NO
	FO-28		
A1319	FO-16	2	NO
	FO-18	1	
	FO-20		
A1320	FO-16	2	NO
	FO-18	2	
	FO-20		
A1321	FO-16	3	NO
	FO-18	2	
	FO-20		
	FO-22		
A1322	FO-16	4	NO
	FO-18	2	
	FO-20		
A1323	FO-36	1	NO
	FO-54	3	
A1324	FO-25	2	YES
A1327	FO-17		YES
	FO-26	2	
A1328	FO-17	2	NO
A1329	FO-17	2	NO
A1330	FO-17	2	NO
A1333	FO-44	1	NO
	FO-41	1	

Table 5-6. Left Hand Assembly Key Signal Lookup

Signal	Distribution								
ACCLD0	*J1220 15	07B	FO1402	J1313 06	11B	FO0603	J1314 06	13B	FO0602
	J1315 06		FO0602	J1313 06		FO0601			
AACRTC	*J1208 60	28A	FO0601	J1313 70		FO0603	J1313 70		FO0602
	J1315 70		FO0602	J1316 70		FO0601	J1327 29	13B	FO5202
AARCD	*J1208 63	31A	FO0601	J1312 20		FO0603	J1316 69		FO0601
	J1327 31	14B	FO5202						
AADUX0	J1219 07	03A	FO1200	*J1221 23	11B	FO1200			
AADVCA	J1213 56	26A	FO0901	J1216 17	08B	FO0500	J1216 55	29B	FO1200
	J1216 76	37A	FO1200	*J1219 09	04B	FO1200	J1220 05	03B	FO0500
	J1220 41	22B	FO0500						
AADVC0	J1100 76	37A	FO0902	*J1216 80	39A	FO1200	J1221 38	18A	FO0401
	J1224 40	19A	FO1100	J1225 14	06A	FO0902	J1225 26	13A	FO0902
	J1225 40	19A	FO0902	J1225 54	25A	FO0902	J1229 45	24B	FO1100
	J1229 54	25A	FO1100	J1229 59	30B	FO1100	J1229 66	32A	FO1100
	J1234 46	21A	FO1200	J1234 54	25A	FO1200			
AAFCI0	J1125 48		FO0601	J1208 54	26A	FO0601	J1312 05		FO0601
AAFC0A	J1208 62	29A	FO0601	J1312 03		FO0601			
AAFSMTA	*J1208 73	35B	FO0601	J1313 68		FO0603	J1314 68		FO0602
	J1315 68		FO0602	J1316 68		FO0601	J1327 25	12B	FO5202
AAFSMTB	*J1208 79	37B	FO0601	J1313 65		FO0603	J1314 65		FO0602
	J1315 65		FO0602	J316 65		FO0601	J1327 23	11B	FO5202
AAFSMTC	*J1208 74	36A	FO0602	J1313 66		FO0603	J1314 66		FO0602
	J1315 66		FO0602	J1313 66		FO0601	J1327 21	10B	FO5202
AAFSMTD	*J1208 80	38B	FO0601	J1313 56		FO0603	J1314 56		FO0602
	J1315 56		FO0602	J1316 56		FO0601	J1327 19	09B	FO5202
AAFS0A	J1125 54		FO0601	J1208 76	37A	FO0601	J1312 14		FO0601
AAFS1A	J1208 70	34A	FO0601	*J1313 04		FO0601			
AAFS2A	J1208 75	35B	FO0601	J1312 02		FO0601			
AAFS3A	J1208 69	32A	FO0601	*J1312 01		FO0601			
AAFT1A	*J1213 76	37A	FO1402	J1221 22	12A	FO1200			
AFF1C0	J1213 72	34A	FO1402	*J1221 57	30B	FO1401			
AAF1EA	J1221 55	29B	FO1401	*J1224 80	39A	FO1401			
AAF2UA	J1218 15	07B	FO1200	*J1200 38	18A	FO1200	J1221 25	12B	FO1200
AAF2U0V	*J1218 10	06B	FO1200	J1226 73	38B	FO1200	J1230 19	09B	FO1200
AALR101A	*J1316 01		FO0602						
AALR102A	*J1316 03		FO0602						

Table 5-6. Left Hand Assembly Key Signal Lookup - Continued

Signal	Distribution								
AALR103A	*J1316 17		FO0602						
AALR104A	J1315 02		FO0602	*J1316 20		FO0602			
AALR111A	J1210 54	25A	FO0500	J1215 27	13B	FO0500	J1228 45	23B	FO0901
	*J1316 21		FO0800	J1320 33		FO0702	J1321 33		FO0702
	J1322 33		FO0702	J1323 33		FO0702	J1325 56		FO0701
AALR112A	J1210 48	22A	FO0500	J1215 29	15B	FO0500	J1228 43	22B	FO0901
	*J1326 36		FO0800	J1320 34		FO0702	J1321 34		FO0702
	J1322 34		FO0702	J1323 34		FO0702	J1325 53		FO0701
AALR113A	J1210-41	22B	FO0500	J1215 33	17B	FO0500	J1228 41	19B	FO0901
	*J1316 45		FO0800	J1320 32		FO0702	J1321 32		FO0702
	J1322 32		FO0702	J1323 32		FO0702	J1325 64		FO0701
AALR114A	J1210 47	25B	FO0500	J1215 39	19B	FO0500	J1228 39	18B	FO0901
	*J1316 37		FO0800	J1320 25		FO0702	J1321 25		FO0702
	J1322 25		FO0702	J1323 25		FO0702	J1325 47		FO0701
AALR121A	*J1316 32		FO0602						
AALA122A	*J1316 31		FO0602						
AALR123A	*J1316 48		FO0602						
AALR124A	J1315 39		FO0602	*J1316 47		FO0602			
AALR131A	J03 03		FO1000	*J1316 40		FO1000			
AALR132A	J03 04		FO1000	*J1316 38		FO1000			
AALR133A	J03 05		FO1000	*J1316 22		FO1000			
AALR134A	J03 06		FO1000	*J1316 19		FO1000			
AALR141A	J1122-29	14B	FO0602	*J1316 55		FO0602			
AALR143AA	J1312 66		FO0603	*J1316 77		FO0602			
AALR144A	J1312 65		FO0603	*J1316 76		FO0602			
AALR145A	J1316 75		FO0602						
AALR146A	J1308 55		FO0602	J1312 55		FO0603	J1316 73		FO0602
AALR147A	J1217 10	07A	FO0603	*J1316 67		FO0602			
AALR201A	*J1315 01		FO0602						
AALR202A	*J1315 03		FO0602						
AALR203A	*J1315 17		FO0602						
AALR204A	J1314 02		FO0602	*J1315 20		FO0602			
AALR2111A	J1210 40	19A	FFO-5--	J1214 05	03B	FO0500	J1227 59	30B	FO0901
	*J1315 21		FO0801	J1320 43		FO0702	J1321 43		FO0702
	J1322 43		FO0702	J1323 43		FO0702	J1325 39		FO0701
AALR212A	J1210 34	16A	FO0500	J1215 09	05B	FO0500	J1227 57	29B	FO0901

Table 5-6. Left Hand Assembly Key Signal Lookup - Continued

Signal	Distribution								
	*J1315 36		FO0801	J1320 39		FO0702	J1321 39		FO0702
	J1322 39		FO0702	J1323 39		FO0702	J1325 62		FO0701
AALR213A	J1210 29	14B	FO0500	J1215 15	07B	FO0500	J1227 55	27B	FO0901
	*J1315 45		FO0801	J1320 42		FO0702	J1321 42		FO0702
	J1322 42		FO0702	J1323 42		FO0702	J1325 30		FO0701
AALR214A	J1210 35	17B	FO0500	J1215 21	11B	FO0500	J1227 53	26B	FO0901
	*J1315 37		FO0801	J1320 38		FO0702	J1321 38		FO0702
	J1322 38		FO0702	J1323 38		FO0702	J1325 29		FO0701
AALR221A	*J1315 32		FO0602						
AALR222A	*J1315 31		FO0602						
AALR223A	*J1315 48		FO0602						
AALR224A	J1314 39		FO0602	*J1315 47		FO0602			
AALR231A	J03 07		FO1000	*J1315 40		FO1000			
AALR232A	J03 08		FO1000	*J1315 38		FO1000			
AALR233A	J03 09		FO1000	*J1315 22		FO1000			
AALR234A	J03 10		FO1000	*J1315 19		FO1000			
AALR241A	J1122 31	15B	FO0602	*J1315 55		FO0602			
AALR243A	J1312 64		FO0603	*J1315 7		FO0602			
AALR244A	J1323 63		FO0603	*J1315 76		FO0602			
AALR245A	J1315 75		FO0602						
AALR246A	J1308 61		FO0602	J1312 59		FO0603	*J1315 73		FO0602
AALR247A	*J1315 67		FO0602	J1316 72		FO0601			
AALR301A	*J1314 01		FO0603						
AALR302A	*J1314 03		FO0603						
AALR303A	*J1314 17		FO0603						
AALR304A	J1313 02		FO0603	*J1314 20		FO0603			
AALR311A	J1210 24	13A	FO0500	J1228 77	36B	FO0901	*J1314 21		FO0802
	J1320 53		FO0702	J1321 53		FO0702	J1322 53		FO0702
	J1323 53		FO0702						
AALR313A	J1210 18	10A	FO0500	J1228 75	35B	FO901	*J1314 36		FO0802
	J1320 52		FO0702	J1321 52		FO0702	J1322 52		FO0702
	J1323 52		FO0702						
AALR313A	J1210 17	08B	FO0500	J1228 73	34B	FO0901	*J1314 45		FO0802
	J1320 51		FO0702	J1321 51		FO0702	J1322 51		FO0702
	J1323 51		FO0702						
AALR314A	J1210 23	11B	FO0500	J1228 71	33B	FO0901	*J1314 37		FO0802

Table 5-6. Left Hand Assembly Key Signal Lookup - Continued

Signal	Distribution											
	J1320	46		FO0702	J1321	46		FO0702	J1322	46		FO0702
	J1323	46		FO0702								
AALR321A	*J1314	32		FO0603								
AALR322A	*J1314	31		FO0603								
AALR323A	*J1314	48		FO0603								
AALR324A	J1313	39		FO0603	*J1314	47		FO0603				
AALR331A	J03	11		FO1000	*J1314	40		FO1000				
AALR332A	J03	12		FO1000	*J1314	38		FO1000				
AALR333A	J03	13		FO1000	*J1314	22		FO1000				
AALR334A	J03	14		FO1000	*J1314	19		FO1000				
AALR341A	J1122	35	17B	FO0603	*J1314	55		FO0603				
AALR343A	J1313	76		FO0603	*J1314	77		FO0603				
AALR344A	J1312	78		FO0603	*J1314	76		FO0603				
AALR345A	J1314	75		FO0603								
AALR346A	J1308	62		FO0603	J1312	60		FO0603	*J1314	73		FO0603
AALR347A	*J1314	67		FO0603	J1315	72		FO0602				
AALR401A	*J1313	01		FO0603								
AALR402A	*J1313	03		FO0603								
AALR403A	*J1313	17		FO0603								
AALR404A	J1217	47	25B	FO0603	J1219	05	03B	FO0601	*J1313	20		FO0603
AALR411A	J1210	08	06A	FO0500	J1313	21		FO0802	J1320	63		FO0702
	J1321	63		FO0702	J1322	63		FO0702	J1323	63		FO0702
AALR412A	J1210	04		FO0500	*J1313	36		FO0802	J1320	60		FO0702
	J1321	60		FO0702	J1322	60		FO0702	J1323	60		FO0702
AALR413A	J1210	03	02A	FO0500	*J1313	45		FO0802	J1320	61		FO0702
	J1321	61		FO0702	J1322	61		FO0702	J1323	61		FO0702
AAL414A	J1210	11	05B	FO0500	J1310	25			*J1313	37		FO0802
	J1320	55		FO0702	J1321	55		FO0702	J1322	55		FO0702
	J1323	55		FO0702								
AALR421A	*J1313	32		FO0603								
AALR422A	*J1313	31		FO0603								
AALR423A	*J1313	48		FO0603								
AALR424A	J1212	39	19B	FO0601	J1216	25	12B	FO0601	J1312	38		FO0602
	*J1313	47		FO0603								
AALR431A	*J1313	40		FO1000								
AALR432A	J03	16		FO1000	*J1313	38		FO1000				

Table 5-6. Left Hand Assembly Key Signal Lookup - Continued

Signal	Distribution											
AALR433A	J03	17		FO1000	*J1313	22		FO1000				
AALR434A	J03	15		FO1000	*J1313	19		FO1000				
AALR441A	J1122	37	18B	FO0603	*J1313	55		FO0603				
AALR442A	J1216	11	05B	FO0603	*J1313	64		FO0603				
AALR443A	J1312	68		FO0603	*J1313	77		FO0603				
AALR444A	J1312	67		FO0603	*J1313	76		FO0603				
AALR446A	J1308	56		FO0603	J1313	57		FO0603	*J1313	73		FO0603
AALR447A	*J1313	67		FO0603	J1314	72		FO0602				
AALSHA	*J1217	50	23A	FO0601	J1218	11	07A	FO0601				
AALSH0V	*J1218	13	06A	FO0601	J1313	04		FO0603	J1314	04		FO0602
	J1315	04		FO0602	J1316	04		FO0601				
AALSIA	J1218	06	05A	FO0601	J1214	78	38A	FO1402	*J1219	01	02B	FO0601
AALSI0V	*J1218	08	04A	FO0601	J1316	02		FO0601				
AAL1SA	*J1312	50		FO0603								
AAMAIA	*J1217	51	27B	FO0603	J1224	45	24B	FO0603				
AAMEIA	*J1217	04	04A	FO0603	J1224	47	25B	FO0603				
AAMMIA	*J1216	15	07B	FO0603	J1224	49	26B	FO0603				
AA0PC0	*J1219	14	09A	FO1401	J1221	68	32A	FO1401				
AAPRTA	*J1219	51	27B	FO1401	J1221	70	33A	FO1401				
AARSCA	*J1217	07	03A	FO0601	J1219	17	08B	FO0601				
AARSH0	*J1219	21	10B	FO0601	J1313	71		FO0603	J1314	71		FO0602
	J1315	71		FO0602	J1316	71		FO0601				
AARSI0	*J1224	51	27B	FO0603	J1313	72		FO0603				
AARSMA	J1219	19	09B	FO0601	*J1220	14	09A	FO1200				
AAT1LA	*J1219	39	19B	FO1402	J1220	11	05B	FO1402				
AAT2LA	J1220	13	06B	FO1402	*J1221	59	31B	FO1401				
AAU2CA	*J1312	70		FO0603	J1315	69		FO0602				
AAU3CA	*J1312	69		FO0603	J1314	69		FO0602				
AAU4CA	*J1312	72		FO0603	J1313	69		FO0603				
AAU5CA	J1312	48		FO0603								
ABIS0A	J1125	52		FO1500	J1207	78	38A	FO1500	*J1312	10		FO1500
ABIS1A	J1207	72	35A	FO1500	*J1312	06		FO1500				
ABIS2A	J1207	77	36B	FO1500	*J1312	11		FO1500				
ABLIPJQ	J1224	62	30A	FO04-1	*J1229	80	39A	FO0401				
ABLIPKQ	J1130	77	38B	FO5201	J1225	66	32A	FO0401	*J1229	79	39B	FO0401
ABLTC1E	J1221	14	09A	FO0401	J1224	57	30B	FO0401	J1224	75	37B	FO0401

Table 5-6. Left Hand Assembly Key Signal Lookup - Continued

Signal	Distribution								
	*J1225 65	33B	FO0401	J1340 54	25A	FO0401	J1340 61	32B	FO0401
ABLTC2E	J1210 71	36A	FO0102	*J1225 68	33A	FO0401	J1229 78	38A	FO0401
ABLT2D	*J1210 72	34A	FO0102						
ABM010	J1123 09	05B	FO5202	*J1325 71		FO0701			
ABM020	J1123 15	07B	FO5202	*J1313 77		FO0603			
ABM030	J1123 11	06B	FO5202	*J1313 80		FO0603			
ABSMXTB	*J1207 79	37B	FO1500	J1313 16		FO0802	J131416		FO0802
	J1315 16		FO0801	J1316 16		FO0801	J1327 18	09A	FO5202
ABSMXTC	*J1207 74	36A	FO1500	J1313 15		FO0802	J1314 15		FO0802
	J1315 15		FO0801	J1316 15		FO0801	J1327 15	07B	FO5202
ABSMXTD	*J1207 80	38B	FO1500	J1313 18		FO0802	J1314 18		FO0802
	J1315 18		FO0801	J1316 18		FO0801	J1327 11	06B	FO5202
ABS00VA	*J1215 42	18B	FO0500	J1235 09	05B	FO0500			
ABS01AV	*J1215 31	16B	FO0500	J1235 07	04B	FO0500			
AVS02AV	*J1215 30	14B	FO0500	J1235 05	03B	FO0500			
ABS03AV	*J1215 26	12B	FO0500	J1235 03	02B	FO0500			
ABS04AV	*J1215 19	10B	FO0500	J1235 08	04A	FO0500			
ABS05AV	*J1215 10	06B	FO0500	J1235 10	05A	FO0500			
ABS06AV	*J1215 07	04B	FO0500	J1235 14	06A	FO0500			
ABS07AV	*J1215 01	02B	FO0500	J1235 13	07A	FO0500			
ACAD104	*SID	C	FO4802	J1308 05		FO0801	J1316 57		FO0801
ACAD204	*SIE	C	FO4802	J1308 07		FO0801	J1316 43		FO0801
ACAD404	*SIF	C	FO4802	J1308 09		FO0801	J1316 43		FO0801
ACCBEA	*J1206 21	10B	FO1100	J1312 52		FO1500			
ACC10JQ	J1220 07	03A	FO1100	J1227 04	02A	FO1401	J1227 20	10A	FO1401
	J1228 04	02A	FO1401	J1228 20	10A	FO1401	*J1229 56	26A	FO1100
	J1314 26		FO0802	J1318 77	38B	FO1100	J1327 39	18B	FO5202
ACC10KQ	J1213 07	03A	FO1100	J1214 72	34A	FO1401	*J1229 51	27B	FO1100
ACC11JQ	J1214 71	36A	FO1401	J1220-03	02A	FO1100	J1227 06	03A	FO1401
	J1227 22	11A	FO1401	J1228 06	03A	FO1401			
	J1228 22	11A	FO1401	*J1229 68	33A	FO1100	J1314 11		FO0802
	J1318 75	37B	FO1100	J1327 41	19B	FO5202			
ACC11KQ	J1213 06	05A	FO1100	*J1229 65	33B	FO110			
ACD8D0T	J1207 66	32B	FO1500	J1216 47	25B	FO1401	J1222 30	15A	FO1401
	*J1226 08	04A	FO1401	J1228 05	03B	FO1401			
ACD8D1T	J1212 47	24A	FO1401	J1216 49	26B	FO1401	*J1226 10	05A	FO1401

Table 5-6. Left Hand Assembly Key Signal Lookup -Continued

Signal	Distribution								
	J1228 21	10B	FO1401						
ACD8D2T	J1212 50	22A	FO1401	J1219 18	10A	FO1401	*J1226 14	06A	FO1401
	J1227 05	03B	FO1401						
ACD8D3T	J1214 09	04B	FO1401	*J1226 13	07A	FO1401	J1227 21	10B	FO1401
ACD800T	J1212 27	13B	FO1401	*J1228 08	04A	FO1401			
ACD801T	J1212 74	35A	FO1401	*J1228 10	05A	FO1401			
ACD802T	J1214 23	11B	FO1402	J1218 22	14A	FO1401	J1219 25	12B	FO1402
	*J1228 14	06A	FO1401						
ACD803T	J1220 34	16A	FO1402	*J1223 13	07A	FO1401			
ACD804T	J1217 24	13A	FO1401	*J1228 17	08B	FO1401			
ACD805T	J1220 23	11B	FO1401	*J1228 07	04B	FO1401			
ACD806T	J1216 41	22B	FO1402	J1221 73	36B	FO1402	* J1228 09	05B	FO1401
ACD807T	J1216 36	17A	FO1300	J1220 24	13A	FO1401	* J1228 11	06B	FO1401
ACD811T	*J1228 26	13A	FO1401	J1312 09		FO1500			
ACD812T	J1217 25	12B	FO1402	J1219 36	17A	FO1402	* J1228 27	14A	FO1401
	J1312 17		FO1500						
ACD813T	J1220 29	14B	FO1401	*J1228 30	15A	FO1401	J1312 08		FO1500
ACD814T	J1217 26	14A	FO1401	*J1228 33	16A	FO1401	J1312 25		FO0601
ACD815T	J1220 25	12B	FO1401	*J1228 23	11B	FO1401			
ACD816T	J1216 43	23B	FO1402	J1221 74	35B	FO1402	J1221 78	38A	FO1402
	*J1228 25	12B	FO1401						
ACD817T	J1220 26	14A	FO1401	*J1228 29	13B	FO1401			
ACD820T	*J1227 08	04A	FO1401	J1312 07		FO0601			
ACD821T	*J1227 10	05A	FO1401	J1312 34		FO0601			
ACD822T	*J1227 14	06A	FO1401	J1312 19		FO0601			
ACD823T	J1221 61	32B	FO1401	*J1227 13	07A	FO1401	J1312 27		FO0601
	J1312 27		FO1402						
ACD824T	*J1227 17	08B	FO1401	J1312 49		FO0601			
ACD825T	*J1227 07	04B	FO1401	J1312 31		FO0601			
ACD826T	J1207 51	25B	FO1200	J1216 61	32B	FO0601	J1217 22	12A	FO1401
	J1218 20	10A	FO1402	J1221 71	36A	FO1402	*J1227 09	05B	FO1401
	J1312 56		FO1500	J1317 75	37B	FO1402			
ACD827T	J1215 04	02A	FO1401	J1221 34	16A	FO1401	J1221 72	34A	FO1402
	*J1227 11	06B	FO1401	J1312 32		FO0601	J1312 40		FO1500
ACD830T	J1214 70	33A	FO0901	*J1227 24	12A	FO1401	J1317 77	38B	FO1402
ACD831T	J1216 59	31B	FO0601	*J1227 26	13A	FO1401	J1312 33		FO0601

Table 5-6. Left Hand Assembly Key Signal Lookup
-Continued

Signal	Distribution								
ACD832T	J1215 36	16A	FO1401	J1219 20	11A	FO1401	J1221 50	23A	FO1402
	J1312 13		FO0603	*J1227 27	14A	FO1401	J1312 46		FO0601
	J1312 12		FO0603						
ACD833T	J1220 36	17A	FO1402	J1221 64	30A	FO1402	*J1227 30	15A	FO1401
	J1317 78	38A	FO1402						
ACD834T	*J1227 33	16A	FO1401	J1312 35		FO0601	J1312 35		FO1402
ACD835T	J1214 21	10B	FO1402	J1218 23	12A	FO1402	J1221 60	28A	FO1401
	*J1227 23	11B	FO1401						
ACD836T	J1214 66	31A	FO0901	J1221 36	17A	FO1401	*J1227 25	12B	FO1401
ACFGPA	*J1217 39	19B	FO0902	J1317 74	35B	FO1402			
ACIM1TA	J1225 48	22A	FO0902	*J1331 55	27B	FO0902			
ACIM1TB	J1225 46	21A	FO0902	*J1331 61	31B	FO0902			
ACIM1TC	J1225 41	22B	FO0902	*J1331 60	28A	FO0902			
ACIM1TD	J1225 43	23B	FO0902	*J1331 63	31A	FO0902			
ACIM2TA	J1225 34	16A	FO0902	*J1331 73	34B	FO0902			
ACIM2TB	J1225 30	15A	FO0902	*J1331 79	37B	FO0902			
ACIM2TC	J1225 29	14B	FO0902	*J1331 74	36A	FO0902			
ACIM2TD	J1225 31	15B	FO0902	*J1331 80	38B	FO0902			
ACIM3TA	J1216 62	29A	FO1100	J1225 20	10A	FO0902	J1229 61	31B	FO1100
	*J1328 55	27B	FO0902						
ACIM3TB	J1216 68	32A	FO1100	J1225 18	09A	FO0902	J1229 47	25B	FO1100
	*J1328 61	31B	FO0902						
ACIM3TC	J1225 15	08B	FO0902	*J1328 60	28A	FO0902			
ACIM3TD	J1225 17	09B	FO0902	*J1328 63	31A	FO0902			
ACIM4TA	J1225 06	03A	FO0902	*J1328 73	34B	FO0902			
ACIM4TB	J1223 30	15A	FO1100	J1225 04	02A	FO0902	*J1328 79	37B	FO0902
ACIM4TC	J1223 29	14B	FO1100	J1225 01	02B	FO0902	*J1328 74	36A	FO0902
ACIM4TD	J1223 31	15B	FO1100	J1225 03	03B	FO0902	*J1328 80	38B	FO0902
ACI10A	*J1216 66	31A	FO1100	J1229 52	24A	FO1100			
ACI11A	*J1216 60	28A	FO1100	J1229 64	31A	FO1100			
ACRQ10E	J1215 20	10A	FO0902	*J1225 47	25B	FO0902	J1316 54		FO0801
	J1325 74		FO0701	J1328 03	02B	FO5202			
ACRQ11E	J1218 36	16A	FO0902	*J1225 51	27B	FO0902	J1316 33		FO0801
	J1325 78		FO0701	J132805	03B	FO5202			
ACRQ12E	J1218 33	17B	FO0902	*J1225 56	26A	FO0902	J1316 26		FO0801
	J1325 76		FO0701	J1328 07	04B	FO5202			

Table 5-6. Left Hand Assembly Key Signal Lookup -Continued

Signal	Distribution								
ACRQ13E	J1218 50	22A	FO0902	*J1225 52	24A	FO0902	J1316 11		FO0801
	J1325 73		FO0701	J1328 09	05B	FO5202			
ACRQ20E	J1217 05	03B	FO0601	J1218 41	23B	FO0902	*J1225 35	17B	FO0902
	J1315 54		FO0801	J1325 70		FO0701	J1328 11	06B	FO5202
ACRQ21E	J1217 54	25A	FO0601	J1218 45	25B	FO0902	*J1225 39	19B	FO0902
	J1325 80		FO0701	J1328 15	07B	FO5202			
ACRQ22E	J1218 51	27B	FO0902	*J1225 42	20A	FO0902	J1315 26		FO0801
	J1325 79		FO0701	J1328 18	09A	FO5202			
ACRQ23E	J1213 18	10A	FO0902	J1220 48	22A	FO0902	*J1225 38 1	8A	FO0902
	J1325 77		FO0701	J1328 17	08B	FO5202			
ACRQ30E	J1213 19	09B	FO0902	J1213 38	18A	FO0902	J1219 62	29A	FO0902
	*J1225 21	11B	FO0902	J1314 54		FO0802	J1327 35	16B	FO5202
ACRQ31E	J1220 59	31B	FO0902	*J1225 27	13B	FO0902	J1314 33		FO0802
	J1325 26		FO0701	J1327 37	17B	FO5202			
ACRQ33E	J1206 19	09B	FO1100	*J1225 24	12A	FO0902			
ACRQ40E	J1213 05	03B	FO1100	J1217 33	16B	FO0902	J1219 53	28B	FO0902
	*J1225 07	05B	FO0902	J1227 03	02B	FO1401	J1227 19	09B	FO1401
	J1228 19	09B	FO1401	J1318 74	35B	FO1100			
ACRQ41E	J1217 35	17B	FO0902	J1219 59	31B	FO0902	*J1225 11	07B	FO0902
	J1226 04	02A	FO1401	J1313 33		FO0802	J1318 73	36B	FO1100
	J1327 45	23B	FO5202						
ACRQ42E	J1219 77	38B	FO0902	*J1225 13	07A	FO0902	J1226 06	03A	FO1401
	J1312 36		FO0601	J1313 26		FO0802	J1318 72	34A	FO1100
	J1327 47	23A	FO5202						
ACRQ43E	J1110 78	38A	FO0902	*J1225 10	05A	FO0902	J1313 11		FO0802
	J1327 50	24A	FO5202						
ACR00AV	J1207 64	30A	FO1200	*J1215 18	09A	FO0902	J1334 22		FO1300
ACR01AV	J1207 56	28B	FO1200	*J1218 34	15A	FO0902	J1334 56		FO1300
ACR02AV	J1207 59	30B	FO1200	*J1218 31	16B	FO0902	J1334 71		FO1300
ACR03AV	J1207 53	26B	FO1200	*J1218 48	21A	FO0902	J1334 62		FO1300
ACR04AV	*J1218 46	22B	FO0902	J1219 47	25B	FO1401	J1334 60		FO1300
ACR05AV	J1212 36	16A	FO0902	*J1218 43	24B	FO0902	J1312 26		FO0601
	J1334 34		FO1300						
ACR050V	*J1212 34	15A	FO0902	J1221 79	39B	FO1402	J1315 33		FO0801
ACR06AV	J1212 21	11B	FO0902	*J1218 53	26B	FO0902	J1334 35		FO1300
ACR060V	*J1212 19	10B	FO0902	J1214 40	19A	FO0601	J1217 23	11B	FO1402

Table 5-6. Left Hand Assembly Key Signal L00kup
-Continued

Signal	Distribution								
ACR07A	J1207 76	37A	FO1500	J1212 29	15B	FO0603	J1213 40	19A	FO0902
	J1216 23	11B	FO0601	J1217 08	06A	FO0603	J1219 04	04A	FO0601
	*J1220 46	21A	FO0902	J1334 24		FO1300			
ACR070V	*J1212 30	14B	FO0603	J1217 49	26B	FO0603	J1315 11		FO0801
ACR08A	J1207 70	34A	FO1500						
	J1334 25		FO1300						
ACR080V	*J1212 31	16B	FO1500	J1312 53		FO1500			
ACR09A	J1207 75	35B	FO1500	J1213 20	11A	FO0902	J1213 37	18B	FO0902
	J1219 11	05B	FO1100	*J1220 63	33B	FO0902	J1334 23		FO1300
ACR12A	J1216 18	10A	FO0902	J1217 29	14B	FO1401	*J1219 57	30B	FO0902
	J1220 76	37A	FO0702	J1312 15		FO1500			
ACR120	J1214 65	34B	FO1401	*J1220 80	39A	FO0902	J1228 03	02B	FO1401
	J1312 42		FO1500	J1313 54		FO0800	J1327 43	22B	FO5202
ACR13A	J1213 04	04A	FO1100	J1213 22	12A	FO0902	J1213 36	17A	FO0902
	*J1219 63	33B	FO0902						
ACR14A	J1213 01	02B	FO1100	J1213 24	13A	FO0902	J1213 34	16A	FO0902
	J1217 37	18B	FO0902	*J1219 75	37B	FO0902			
ACTRKA	*J1219 72	34A	FO5402	J1226 37	17B	FO1200	J1226 69	32A	FO1200
	J1227 51	25B	FO0901	J1227 69	32A	FO1200	J1228 37	17B	FO0901
	J1228 69	32A	FO0901	J1325 60		FO0701			
ACWDTJQ	J1220 49	26B	FO0102	*J1229 13	07A	FO0102			
ACWSJA	*J1216 30	15A	FO1300	J1218 52	26A	FO1300			
ACWSJ0V	*J1218 54	25A	FO1300	J1334 07		FO1300			
ACWSWJ	J1214 22	12A	FO1000	*J1334 05		FO1300			
ACXBA0	J1312 23		FO0601						
ADCCJ0	*J1220 75	37B	FO1000	J1233 40	19A	FO1000			
ADCCWK	J1220 08	06A	FO1000	*J1233 35	17B	FO1000			
ADC0BAV	J1207 52	25A	FO1200	*J1218 01	25B	FO0401	*J1218 01	25B	FO0901
	*J1218 01	25B	FO0902	*J1218 01	25B	FO1401	*J1218 01	02B	FO0500
	J1225 59	30B	FO0401	J1226 05	03B	FO1401	J1226 21	10B	FO0901
	J1328 52	25A	FO0901	J1328 52	25A	FO0902	J1328 68	33A	FO0901
	J1328 68	33A	FO0902	J1331 52	25A	FO0902	J1331 68	33A	FO0902
	J1332 52	25A	FO0901	J1341 13	07A	FO5201	J1341 71	33B	FO0500
ADC0CAV	J1204 47	23A	FO4402	J1207 68	33A	FO1500	J1208 52	25A	FO0601
	*J1218 60	28A	FO0601	*J1218 60	28A	FO0901	*J1218 60	28A	FO0401
	*J1218 60	28A	FO0500	*J1218 60	28A	FO1401	*J121860	28A	FO1500

Table 5-6. Left Hand Assembly Key Signal L00kup
-Continued

Signal	Distribution								
	J1225 53	28B	FO0401	J1225 74	36A	FO0500	J1226 03	02B	FO1401
	J1227 78	38A	FO1200	J1235 11	06B	FO0500	J1332 68	33A	FO0901
	J1342 48	22A	FO4700						
ADC0DAV	J1204 61	31B	FO4402	J1208 68	33A	FO0601	*J1218 56	28B	FO0500
	*J1218 56	28B	FO0601	*J1218 56	28B	FO1101	*J1218 56	28B	FO1200
	J1223 36	17A	FO0500	J1225 08	04A	FO0902	J1225 22	11A	FO0902
	J1225 78	38A	FO1200						
	J1227 79	37B	FO1200	J1327 52	25A	FO0901	J1332 13	07A	FO1200
	J1341 68	33A	FO0500	J1342 30	15A	FO4700			
ADC0EAV	*J1218 57	30B	FO0300	*J1218 57	30B	FO0401	*J1218 57	30B	FO0500
	*J1218 57	30B	FO0901	*J1218 57	30B	FO1200	J1225 57	28A	FO0401
	J1226 79	37B	FO1200	J1230 21	10B	FO1200	J1327 68	33A	FO0901
	J1332 30	15A	FO1200	J1332 48	22A	FO0500	J1336 68	33A	FO0300
	J1341 77	36B	FO0500	J1342 13	07A	FO4700			
ADC0FAV	*J1218 68	32B	FO0200	J1230 48	22A	FO0200	J1230 61	31B	FO0200
	J1231 47	23A	FO0200	J1231 64	30A	FO0200	J1231 79	37B	FO0200
	J1232 47	23A	FO0200	J1232 64	30A	FO0200	J1232 79	37B	FO0200
	J1336 52	25A	FO0200						
ADC0GAV	J1204 48	22A	FO4402	J1204 64	30A	FO4402	J1207 48	22A	FO5202
	J1208 48	22A	FO5202	*J1215 77	38A	FO5201	J1327 13	07A	FO5202
	J1327 30	15A	FO5202	J1327 48	22A	FO5202	J1328 13	07A	FO5202
	J1328 30	15A	FO5202	J1328 48	22A	FO5202	J1331 13	07A	FO5202
	J1331 30	15A	FO5201	J1331 48	22A	FO5202	J1341 30	15A	FO5202
	J1341 13		FO5202						
ADDBLA	J1339 54	25A	FO0401	*J1340 52	24A	FO0401			
ADDBL0	J1229 07	05B	FO0101	J1229 10	05A	FO0102	*J1339 52	24A	FO0401
ADDDT0	*J1118 15	07B	FO0102	J1229 73	36B	FO0401			
ADDFBR	J1221 20	11A	FO0401	J1229 08	04A	FO00102	J1338 73	36B	FO0102
	*J1339 72	34A	FO0102						
ADDFBS	J1224 61	32B	FO0401	J1229 09	06B	FO0102	*J1338 72	34A	FO0102
	J1339 73	36B	FO0102						
ADDLCB4	*J1210 72	34A	FO0102	J1211 61		FO0102	*J1311 09	04B	FO0102
	J1339 03	02A	FO0102	J1339 04	04A	FO0102	J1339 08	06A	FO0102
	J1339 11	05B	FO0102	J1339 17	08B	FO0102	J1339 18	10A	FO0102
	J1339 23	11B	FO0102	J1339 24	13A	FO0102	J1339 71	36A	FO0102
	J1339 77	38B	FO0102						

Table 5-6. Left Hand Assembly Key Signal L00kup
-Continued

Signal				Distribution					
ADDL1D	*J1311 09	04B	FO0102						
ADDLPR	J1118 09	04B	FO0102	J1338 10	07A	FO0102	*J1339 06	05A	FO0102
ADDLPS	J1235 79	38B	FO0102	*J1338 06	05A	FO0102	J1339 10	07A	FO0102
ADDL0R	J1206 34	16A	FO0102	J1230 59	30B	FO0200	J1231 59	30B	FO0200
	J1338 05	03B	FO0102	*J1339 01	02B	FO0102			
ADDL0S	J1229 05	04B	FO0102	J1235 71	34B	FO0102	*J1338 01	02B	FO0102
	J1339 05	03B	FO0102						
ADDL1R	J1206 36	17A	FO0102	J1230 57	29B	FO0200	J1231 57	29B	FO0200
	J1338 07	03A	FO0102	*J1339 09	04B	FO0102			
ADDL1S	J1235 73	35B	FO0102	*J1338 09	04B	FO0102	J1339 07	03A	FO0102
ADDL2R	J1206 30	15A	FO0102	J1230 55	27B	FO0200	J1231 55	27B	FO0200
	J1338 13	06B	FO0102	*J1339 15	07B	FO0102			
ADDL2S	J1235 75	36B	FO0102	*J1338 15	07B	FO0102	J1339 13	06B	FO0102
ADDL3R	J1206 31	15B	FO0102	J1230 53	26B	FO0200	J1231 53	26B	FO0200
	J1338 26	14A	FO0102	*J1339 22	12A	FO0102			
ADDL3S	J1235 77	37B	FO0102	*J1338 22	12A	FO0102	J1339 26	14A	FO0102
ADDL4R	J1206 50	23A	FO0102	J1230 45	23B	FO0200	J1336 53	26B	FO0200
	J1338 20	11A	FO0102	*J1339 14	09A	FO0102			
ADDL4S	J1235 72	36A	FO0102	*J1338 14	09A	FO0102	J1339 20	11A	FO0102
ADDL5R	J1206 43	23B	FO0102	J1230 43	22B	FO0200	J1336 59	30B	FO0200
	J1338 19	09B	FO0102	*J1339 21	10B	FO0102			
ADDL5S	J1235 70	35A	FO0102	*J1338 21	10B	FO0102	J1339 19	09B	FO102
ADDL6R	J1206 46	21A	FO0102	J1230 27	13B	FO0102			
ADDL6S	J1235 68	34A	FO0102	*J1338 27	13B	FO0102	J1339 25	12B	FO0102
ADDL7R	J1206 48	22A	FO0102	J1230 39	18B	FO0200	J1336 64	30A	FO0200
	J1338 79	39B	FO0102	*J1339 75	37B	FO0102			
ADDL7S	J1235 66	33A	FO0102	*J1338 75	37B	FO0102			
	J1339 79	39B	FO0102						
ADDM1TA	J1340 10	07A	FO0102	*J1342 55	27B	FO0102			
ADDM1TB	J1340 05	03B	FO0102	*J1342 61	31B	FO0102			
ADDM1TC	J1340 03	02A	FO0102	*J1340 60	28A	FO0102			
ADDM1TD	J1340 11	05B	FO0102	*J1342 63	31A	FO0102			
ADDM2TA	J1340 24	13A	FO0102	*J1342 73	34B	FO0102			
ADDM2TB	J1340 18	10A	FO0102	*J1342 79	37B	FO0102			
ADDM2TC	J1340 17	08B	FO0102	*J1342 74	36A	FO0102			
ADDM2TD	J1340 23	11B	FO0102	*J1342 80	38B	FO0102			

Table 5-6. Left Hand Assembly Key Signal L00kup
-Continued

Signal				Distribution					
ADDM3TB	J1340 77	38B	FO0102	*J1341 61	31B	FO0102			
ADDM3TD	J1340 71	36A	FO0102	*J1341 63	31A	FO0102			
ADDNPA	J1338 08	06A	FO0102	*J1340 06	05A	FO0102			
ADDNSA	J1338 71	36A	FO0102	*J1340 72	34A	FO0102			
ADDN0A	J1338 04	04A	FO0102	*J1340 01	02B	FO0102			
ADDN1A	J1338 03	02A	FO0102	*J1340 09	04B	FO0102			
ADDN2A	J1338 11	05B	FO0102	*J1340 15	07B	FO0102			
ADDN3A	J1338 24	13A	FO0102	*J1340 22	12A	FO0102			
ADDN4A	J1338 18	01A	FO0102	*J1340 14	09A	FO0102			
ADDN5A	J1338 17	08B	FO0102	*J1340 21	01B	FO0102			
ADDN6A	J1338 23	11B	FO0102	*J1340 27	13B	FO0102			
ADDN7A	J1338 77	38B	FO0102	*J1340 75	37B	FO0102			
ADD0BJ	J1221 19	09B	FO0401	*J1233 49	26B	FO0401			
ADD0BK	J1224 79	39B	FO0401	*J1233 47	25B	FO0401			
ADDPCPR	J1220 47	25B	FO0102	*J1235 76	38A	FO0102			
ADDWDJ	J1229 35	17B	FO0401	*J1234 78	38A	FO0401			
ADDWDK	J1130 78	38A	FO5201	J1221 18	10A	FO0401	J1224 59	31B	FO0401
	J1224 77	38B	FO0401	*J1234 76	37A	FO0401	J1340 56	26A	FO0401
ADD1LA	*J1224 63	33B	FO0401	J1339 48	22A	FO0401			
ADD3LA	*J1224 73	36B	FO0401	J1339 50	23A	FO0401			
ADD3RAV	*J1105 78	36A	FO0102	J1118 13	06B	FO0102			
ADD3R0	J1105 76	37A	FO0102	*J1206 33	16B	FO0102			
ADD8RAV	*J1105 72	34A	FO0102	J1118 11	05B	FO0102	J1105 74	35A	FO0102
	*J1206 45	24B	FO0102						
ADMTFA	*J1220 51	27B	FO0102	J1336 49	24B	FO0200			
AD1D6A	*J1214 74	35B	FO1401	J1224 78	38A	FO1401			
AD1G20	J1213 26	14A	FO0902	J1213 30	15A	FO0902	*J1216 14	09A	FO0902
AD7R3A	J1216 20	11A	FO0902	*J1220 09	04B	FO1100			
AD8D10V	*J1212 49	23A	FO1401	J1217 34	16A	FO1401	J1312 39		FO1500
AD8D20V	*J1212 48	21A	FO1401	J1312 43		FO1500			
AD8D30	*J1214 15	07B	FO1401	J1312 16		FO1500			
AD8L20	*J1216 51	27B	FO1401	J1224 76	37A	FO1401			
AESCPA	J1216 78	38A	FO1200	*J1219 22	12A	FO1200			
AFA000	J1320 74		FO0702	J1321 74		FO0702	J1322 74		FO0702
	J1323 74		FO0702	J1324 08		FO0701	J1324 38		FO0701
	J1324 60		FO0701	*J1325 57		FO0701			

Table 5-6. Left Hand Assembly Key Signal L00kup
-Continued

Signal			Distribution				
AFA010	J1320 73		FO0702	J1321 73	FO0702	J1322 73	FO0702
	J1323 73		FO0702	J1324 09	FO0701	J1324 35	FO0701
	J1324 61		FO0701	*J1325 55	FO0701		
AFA020	J1320 77		FO0702	J1321 77	FO0702	J1322 77	FO0702
	J1323 77		FO0702	J1324 10	FO0701	J1324 39	FO0701
	J1324 62		FO0701	*J1325 54	FO0701		
AFA030	J1320 72		FO0702	J1321 72	FO0702	J1322 72	FO0702
	J1323 72		FO0702	J1324 18	FO0701	J1324 36	FO0701
	J1324 64		FO0701	*J1325 75	FO0701		
AFA040	J1324 23		FO0701	J1324 40	FO0701	J1324 70	FO0701
	*J1325 49		FO0701				
AFA050	J1324 24		FO0701	J1324 37	FO0701	J1324 72	FO0701
	*J1325 52		FO0701				
AFBS0A	J1323 05		FO0702	*J1325 41	FO0701		
AFBS1A	J1323 80		FO0702	*J1325 45	FO0701		
AFBS2A	J1322 05		FO0702	*J1325 46	FO0701		
AFBS3A	J1322 80		FO0702	*J1325 48	FO0701		
AFBS4A	J1321 05		FO0702	*J1325 51	FO0701		
AFBS5A	J1321 80		FO0702	*J1325 40	FO0701		
AFBS6A	J1320 05		FO0702	*J1325 42	FO0701		
AFBS7A	J1320 80		FO0702	*J1325 43	FO0701		
AFCB00	J1324 27		FO0701	J1324 29	FO0701	*J1325 24	FO0701
AFCB10	J1324 31		FO0701	J1324 48	FO0701	*J1325 37	FO0701
AFCB20	J1324 63		FO0701	J1324 80	FO0701	*J1325 34	FO0701
AFCB30	J1324 17		FO0701	J1324 43	FO0701	*J1325 38	FO0701
AFCM100B	J1317 07	03A	FO0702	*J1324 59	FO0701		
AFCM101B	J1317 22	12A	FO0702	*J1324 57	FO0701		
AFCM102B	J1317 37	18B	FO0702	*J1324 56	FO0701		
AFCM103B	J1317 50	23A	FO0702	*J1324 55	FO0701		
AFCM104B	J1317 64	30A	FO0702	*J1324 65	FO0701		
AFCM105B	J1318 07	03A	FO0702	*J1324 66	FO0701		
AFCM106B	J1318 22	12A	FO0702	*J1324 68	FO0701		
AFCM107B	J1318 37	18B	FO0702	*J1324 69	FO0701		
AFCM140B	*J1324 13		FO0701				
AFCM141B	*J1324 11		FO0701				
AFCM142B	*J1324 15		FO0701				

Table 5-6. Left Hand Assembly Key Signal L00kup
-Continued

Signal			Distribution				
AFCM143B	*J1324 14		FO0701				
AFCM144B	*J1324 22		FO0701				
AFCM145B	*J1324 19		FO0701				
AFCM146B	*J1324 21		FO0701				
AFCM147B	*J1324 20		FO0701				
AFCM150B	*J1324 46		FO0701				
AFCM151B	*J1324 47		FO0701				
AFCM152B	*J1324 74		FO0701				
AFCM153B	*J1324 75		FO0701				
AFCM154B	*J1324 76		FO0701				
AFCM155B	*J1324 77		FO0701				
AFCM156B	*J1324 78		FO0701				
AFCM157B	*J1324 79		FO0701				
AFCM160B	*J1324 49		FO0701				
AFCM161B	*J1324 50		FO0701				
AFCM162B	*J1324 51		FO0701				
AFCM163B	*J1324 52		FO0701				
AFCM164B	*J1324 53		FO0701				
AFCM165B	*J1324 54		FO0701				
AFCM166B	*J1324 71		FO0701				
AFCM167B	*J1324 73		FO0701				
AFCM170B	*J1324 01		FO0701				
AFCM171B	*J1324 03		FO0701				
AFCM172B	*J1324 04		FO0701				
AFCM173B	*J1324 05		FO0701				
AFCM174B	*J1324 06		FO0701				
AFCM175B	*J1324 07		FO0701				
AFCM176B	*J1324 25		FO0701				
AFCM177B	*J1324 26		FO0701				
AFC08B	J1318 50	23A	FO0702	*J1324 01	FO0701	*J1324 13	FO0701
	*J1324 46		FO0701	*J1324 49	FO0701		
AFC09B	J1318 64	30A	FO0702	*J1324 03	FO0701	*J1324 11	FO0701
	*J1324 47		FO0701	*J1324 50	FO0701		
AFC10B	J1319 07	03A	FO0702	*J1324 04	FO0701	*J1324 15	FO0701
	*J1324 51		FO0701	*J1324 74	FO0701		
AFC11B	J1319 22	12A	FO0702	*J1324 05	FO0701	*J1324 14	FO0701

Table 5-6. Left Hand Assembly Key Signal L00kup
-Continued

Signal			Distribution						
	*J1324 52		FO0701	*J1324 75		FO0701			
AFC12B	J1319 37	18B	FO0702	*J1324 06		FO0701	*J1324 22		FO0701
	*J1324 53		FO0701	*J1324 76		FO0701			
AFC13B	J1319 50	23A	FO0702	*J1324 07		FO0701	*J1324 19		FO0701
	*J1324 54		FO0701	*J1324 77		FO0701			
AFC14B	J1319 64	30A	FO0702	*J1324 21		FO0701	*J1324 25		FO0701
	*J1324 71		FO0701	*J1324 78		FO0701			
AFC15B	J1319 75	37B	FO0702	*J1324 20		FO0701	*J1324 26		FO0701
	*J1324 73		FO0701	*J1324 79		FO0701			
AFD000	J1208 35	16B	FO5202	J1224 21	10B	FO1200	J1316 53		FO0601
	J1316 53		FO0801	*J1317 11	05B	FO0702	J1332 17	08B	FO1200
AFD010	J1208 37	17B	FO5202	J1316 35		FO0601	J1316 35		FO0801
	*J1317 23	11B	FO0702	J1332 03	02B	FO1200	J1332 33	16A	FO1200
AFD020	J1208 39	18B	FO5202	J1316 74		FO0601	J1316 74		FO0801
	*J1317 35	17B	FO0702	J1332 05	03B	FO1200	J1332 19	09B	FO1200
AFD030	J1208 41	19B	FO5202	J1316 09		FO0601	J1316 09		FO0801
	*J1317 47	25B	FO0702	J1332 07	04B	FO1200	J1332 21	10B	FO1200
AFD040	J1208 43	22B	FO5202	J1315 53		FO0602	J1315 53		FO0801
	*J1317 59	31B	FO0702	J1332 09	05B	FO1200	J1332 23	11B	FO1200
AFD050	J1208 45	23B	FO5202	J1315 35		FO0602	J1315 35		FO0801
	*J1318 11	05B	FO0702	J1332 11	06B	FO1200	J1332 25	12B	FO1200
AFD060	J1208 47	23A	FO5202	J1315 74		FO0602	J1315 74		FO0801
	*J1318 23	11B	FO0702	J1332 15	07B	FO1200	J1332 29	13B	FO1200
AFD070	J1208 50	24A	FO5202	J1315 09		FO0602	J1315 09		FO0801
	*J1318 35	17B	FO0702	J1332 18	09A	FO1200	J1332 31	14B	FO1200
AFD080	J1207 35	16B	FO5202	J1314 53		FO0602	J1314 53		FO0802
	*J1318 47	25B	FO0702	J1332 34	15B	FO1200			
AFD090	J1207 37	17B	FO5201	J1314 35		FO0602	J1314 35		FO0802
	*J1318 59	31B	FO0702						
AFD100	J1207 39	18B	FO5202	J1314 74		FO0602	J1314 25		FO0802
	*J1319 11	05B	FO0702						
AFD110	J1207 41	19B	FO5202	J1314 09		FO0602	J1314 09		FO0802
	*J1319 23	11B	FO0702						
AFD120	J1207 43	22B	FO5202	J1313 53		FO0603	J1313 53		FO0802
	*J1319 35	17B	FO0702						
AFD130	J1207 45	23B	FO5202	J1313 35		FO0603	J1313 35		FO0802

Table 5-6. Left Hand Assembly Key Signal L00kup
-Continued

Signal				Distribution				
	*J1319 47	25B	FO0702					
AFD140	J1207 47	23A	FO5202	J1313 74		FO0603	J1313 74	FO0802
	*J1319 59	31B	FO0702					
AFD150	J1207 50	24A	FO5202	J1313 09		FO0603	J1313 09	FO0802
	*J1319 76	37A	FO0702					
AFRW100C	J1317 06	05A	FO0702	*J1323 27		FO0702		
AFRW101C	J1317 20	11A	FO0702	*J1323 31		FO0702		
AFRW102C	J1317 36	17A	FO0702	*J1323 36		FO0702		
AFRW103C	J1317 49	26B	FO0702	*J1323 35		FO0702		
AFRW104C	J1317 62	29A	FO0702	*J1323 37		FO0702		
AFRW105C	J1318 06	05A	FO0702	*J1323 40		FO0702		
AFRW106C	J1318 20	11A	FO0702	*J1323 41		FO0702		
AFRW107C	J1318 36	17A	FO0702	*J1323 45		FO0702		
AFRW108C	J1318 49	26B	FO0702	*J1323 49		FO0702		
AFRW109C	J1318 62	29A	FO0702	*J1323 50		FO0702		
AFRW110C	J1319 06	05A	FO0702	*J1323 54		FO0702		
AFRW111C	J1319 20	11A	FO0702	*J1323 56		FO0702		
AFRW112C	J1319 36	17A	FO0702	*J1323 57		FO0702		
AFRW113C	J1319 49	26B	FO0702	*J1323 59		FO0702		
AFRW114C	J1319 62	29A	FO0702	*J1323 62		FO0702		
AFRW115C	J1319 74	35B	FO0702	*J1323 65		FO0702		
AFRW200C	J1317 05	03B	FO0702	*J1322 27		FO0702		
AFRW201C	J1317 19	09B	FO0702	*J1322 31		FO0702		
AFRW202C	J1317 34	16A	FO0702	*J1322 36		FO0702		
AFRW203C	J1317 48	22A	FO0702	*J1322 35		FO0702		
AFRW204C	J1317 61	32B	FO0702	*J1322 37		FO0702		
AFRW205C	J1318 05	03B	FO0702	*J1322 40		FO0702		
AFRW206C	J1318 19	09B	FO0702	*J1322 41		FO0702		
AFRW207C	J1318 34	16A	FO0702	*J1322 45		FO0702		
AFRW208C	J1318 48	22A	FO0702	*J1322 49		FO0702		
AFRW209C	J1318 61	32B	FO0702	*J1322 50		FO0702		
AFRW210C	J1319 05	03B	FO0702	*J1322 54		FO0702		
AFRW211C	J1319 19	09B	FO0702	*J1322 56		FO0702		
AFRW212C	J1319 34	16A	FO0702	*J1322 57		FO0702		
AFRW213C	J1319 48	22A	FO0702	*J1322 59		FO0702		
AFRW214C	J1319 61	32B	FO0702	*J1322 62		FO0702		

Table 5-6. Left Hand Assembly Key Signal L00kup
-Continued

Signal				Distribution				
AFRW215C	J1319 73	36B	FO0702	*J1322 65		FO0702		
AFRW300C	J1317 04	04A	FO0702	*J1321 27		FO0702		
AFRW301C	J1317 18	10A	FO0702	*J1321 31		FO0702		
AFRW302C	J1317 31	15B	FO0702	*J1321 36		FO0702		
AFRW303C	J1317 46	21A	FO0702	*J1321 35		FO0702		
AFRW304C	J1317 60	28A	FO0702	*J1321 37		FO0702		
AFRW305C	J1318 04	04A	FO0702	*J1321 40		FO0702		
AFRW306C	J1318 18	01A	FO0702	*J1321 41		FO0702		
AFRW307C	J1318 31	15B	FO0702	*J1321 45		FO0702		
AFRW308C	J1318 46	21A	FO0702	*J1321 49		FO0702		
AFRW309C	J1318 60	28A	FO0702	*J1321 50		FO0702		
AFRW310C	J1319 04	04A	FO0702	*J1321 54		FO0702		
AFRW311C	J1319 18	10A	FO0702	*J1321 56		FO0702		
AFRW312C	J1319 31	15B	FO0702	*J1321 57		FO0702		
AFRW313C	J1319 46	21A	FO0702	*J1321 59		FO0702		
AFRW314C	J1319 60	28A	FO0702	*J1321 62		FO0702		
AFRW315C	J1319 72	34A	FO0702	*J1321 65		FO0702		
AFRW400C	J1317 01	02B	FO0702	*J1320 27		FO0702		
AFRW401C	J1317 14	09A	FO0702	*J1320 31		FO0702		
AFRW402C	J1317 30	15A	FO0702	*J1320 36		FO0702		
AFRW403C	J1317 43	23B	FO0702	*J1320 35		FO0702		
AFRW404C	J1317 55	29B	FO0702	*J1320 37		FO0702		
AFRW405C	J1318 01	02B	FO0702	*J1320 40		FO0702		
AFRW406C	J1318 14	09A	FO0702	*J1320 41		FO0702		
AFRW407C	J1318 30	15A	FO0702	*J1320 45		FO0702		
AFRW408C	J1318 43	23B	FO0702	*J1320 49		FO0702		
AFRW409C	J1318 55	29B	FO0702	*J1320 50		FO0702		
AFRW410C	J1319 01	02B	FO0702	*J1320 54		FO0702		
AFRW411C	J1319 14	09A	FO0702	*J1320 56		FO0702		
AFRW412C	J1319 30	15A	FO0702	*J1320 57		FO0702		
AFRW413C	J1319 43	23B	FO0702	*J1320 59		FO0702		
AFRW414C	J1319 55	29B	FO0702	*J1320 62		FO0702		
AFRW415C	J1319 71	36A	FO0702	*J1320 65		FO0702		
AFWBSA	J1214 54	25A	FO1401	*J1216 33	16B	FO1401		
AFWDRA	J1214 56	26A	FO1401	*J1216 39	19B	FO1401		
AFWEN0	*J1214 50	23A	FO1401	J1320 03		FO0702	J1321 03	FO0702

Table 5-6. Left Hand Assembly Key Signal L00kup
-Continued

Signal	Distribution									
	J1322 03		FO0702	J1323 03		FO0702				
AFWSCA	J1214 52	24A	FO1401	*J1217 31	15B	FO1401	J1221 31	15B	FO1401
AGRSWA	*J1220 69	35A	FO1401	J1334 42		FO1300			
AGSSWA	*J1220 39	19B	FO1401	J1334 70		FO1300			
AHACK0V	*J1212 40	19A	FO1000	J1233 30	15A	FO1000	J1233 42	20A	FO1000
AH0DXA	*J1214 07	03A	FO1000	J1220 77	38B	FO1000			
AH0PDA	*J1214 20	11A	FO1000	J1220 79	39B	FO1000			
AH0RDA	J03 01		FO1000	*J1214 51	27B	FO1000			
AH0150	J03 18		FO1000	*J1220 06	05A	FO1000			
AHRLDA	J1135 76	37A	FO1000	*J1206 59	31B	FO1000	J1215 06	05A	FO1000
	J1334 03		FO1300						
AHRLD0V	J1214 05	03B	FO1000	J1214 26	14A	FO1000	*J1215 08	04A	FO1000
	J1313 80		FO1000	J1314 80		FO1000			
	J1315 80		FO1000	J1316 80		FO1000			
AHRLIA	J1214 77	38B	FO1402	*J1217 19	09B	FO1000	J1221 07	03A	FO1402
AHRRDJ	J1214 45	24B	FO1000	J1217 17	08B	FO1000	*J1233 31	15B	FO1000
AHRRJ0	*J1135 80	39A	FO1000	J1233 34	16A	FO1000			
AIBADJ	*J1233 43	23B	FO1401	J1234 71	36A	FO0402	1338 64	30A	FO0402
	J1340 64	30A	FO0402						
AIBADK	J1229 37	18B	FO0401	*J1233 45	24B	FO0401			
AIBAFAV	*J1218 70	34B	FO0401	J1233 60	28A	FO0401			
AIBAF0	J1218 69	35B	FO0401	J1233 62	29A	FO0401	*J1325 06		FO0401
AIBAMTA	J1335 72		FO0200	*J1336 73	34B	FO0300			
AIBAMTB	J1335 77		FO0200	*J1336 79	37B	FO0300			
AIBAMTC	J1335 73		FO0200	*J1336 74	36A	FO0300			
AIBAMTD	J1335 74		FO0200	*J1336 80	38B	FO0300			
AIBASR	J1224 62	29A	FO0402	J1336 66	32B	FO0300	*J1338 60	28A	FO0402
	J1339 62	29A	FO0300	J1339 70	33A	FO0402			
AIBASS	J1224 70	33A	FO0402	J1325 09		FO0401	J1325 15		FO0401
	J1338 53	28B	FO0300	J1338 62	29A	FO0402	*J1339 66	31A	FO0402
AIBAVJ	J1224 60	28A	FO0402	J1224 68	32A	FO0402	J1233 46	21A	FO0401
	*J1234 74	35B	FO0402						
AIBA4AV	*J1218 72	34A	FO0200	J1335 80		FO0200			
AIBA40	J1218 74	35A	FO0200	J1335 05		FO0200	*J1340 57	30B	FO0300
AIBCAK	J1119 31	15B	FO5002	*J1233 57	30B	FO0401			
AIBCC0	J1325 50		FO0401	*J1338 69	35A	FO0401			

Table 5-6. Left Hand Assembly Key Signal L00kup
-Continued

Signal	Distribution								
AIBC40	J1325 17		FO0401	J1325 18		FO0401	*J1325 25		FO0401
AIBELA	J1214 14	09A	FO0401	*J1221 21	10B	FO0401	J1231 50	24A	FO0200
	J1231 63	31A	FO0200	J1339 41	22B	FO0401			
AIBEL0	J1233 56	26A	FO0401	J1234 77	38B	FO0401	*J1339 45	24B	FO0401
AIBEMA	J1325 13		FO0401	J1339 65	34B	FO0401			
AIBEM0	J1338 68	32A	FO0401	*J1339 69	35A	FO0401			
AIBG00	J1233 48	22A	FO0401	*J1340 66	31A	FO0401			
AIBH11U	*J1231 38	18A	FO0200	J1335 25		FO0200	J1341 03	02B	FO5202
AIBH12U	*J1231 40	19A	FO0200	J1335 32		FO0200	J1341 05	03B	FO5202
AIBH13U	*J1231 42	20A	FO0200	J1335 34		FO0200	J1341 07	04B	FO5202
AIBH14U	*J1231 46	21A	FO0200	J1335 33		FO0200	J1341 09	05B	FO5202
AIBH21U	*J1231 54	26A	FO0200	J1335 38		FO0200	J1341 11	06B	FO5202
AIBH22U	*J1231 56	28B	FO0200	J1335 42		FO0200	J1341 15	07B	FO5202
AIBH23U	*J1231 60	28A	FO0200	J1335 39		FO0200	J1341 18	09A	FO5202
AIBH24U	*J1231 62	29A	FO0200	J1335 43		FO0200	J1341 17	08B	FO5202
AIBH31U	*J1230 38	18A	FO0200	J1331 03	02B	FO5202	J1335 46		FO0200
AIBH32U	*J1230 40	19A	FO0200	J1331 05	03B	FO5202	J1335 51		FO0200
AIBH33U	*J1230 42	20A	FO0200	J1331 07	04B	FO5202	J1335 52		FO0200
AIBH34U	*J1230 46	21A	FO0200	J1331 09	05B	FO5202	J1335 53		FO0200
AIBH41U	*J1230 54	26A	FO0200	J1331 11	06B	FO5202	J1335 55		FO0200
AIBH42U	*J1230 56	28B	FO0200	J1331 15	07B	FO5202	J1335 61		FO0200
AIBH43U	*J1230 60	28A	FO0200	J1331 18	09A	FO5202	J1335 60		FO0200
AIBH44U	*J1230 62	29A	FO0200	J1331 17	08B	FO5202	J1335 63		FO0200
AIBIMTA	J1231 45	23B	FO0200	*J1336 55	27B	FO0300			
AIBIMTB	J1231 43	22B	FO0200	*J1336 61	31B	FO0300			
AIBIMTC	J1231 41	19B	FO0200	*J1336 60	28A	FO0300			
AIBIMTD	J1231 39	18B	FO0200	*J1336 63	31A	FO0300			
AIBM100C	J1232 39	18B	FO0200	J1331 19	09B	FO5201	*J1335 27		FO0200
AIBM101C	J1232 41	19B	FO0200	J1331 21	10B	FO5201	*J1335 31		FO0200
AIBM102C	J1232 43	22B	FO0200	J1331 23	11B	FO5201	*J1335 36		FO0200
AIBM103C	J1232 45	23B	FO0200	J1331 25	12B	FO5201	*J1335 35		FO0200
AIBM104C	J1232 53	26B	FO0200	J1331 29	13B	FO5201	*J1335 37		FO0200
AIBM105C	J1232 55	27B	FO0200	J1331 31	14B	FO5201	*J1335 40		FO0200
AIBM106C	J1232 57	29B	FO0200	J1331 34	15B	FO5201	*J1335 41		FO0200
AIBM107C	J1232 59	30B	FO0200	J1331 33	16A	FO5201	*J1335 45		FO0200
AIBM108C	J1232 71	33B	FO0200	J1331 35	16B	FO5202	*J1335 49		FO0200

Table 5-6. Left Hand Assembly Key Signal L00kup
-Continued

Signal	Distribution								
AIBM109C	J1232 73	34B	FO0200	J1331 37	17B	FO5202	*J1335 50		FO0200
AIBM010C	J1232 75	35B	FO0200	J1331 39	18B	FO5202	*J1335 54		FO0200
AIBM111C	J1232 77	36B	FO0200	J1331 41	19B	FO5202	*J1335 56		FO0200
AIBM112C	J1231 71	33B	FO0200	J1331 43	22B	FO5202	*J1335 57		FO0200
AIBM113C	J1231 73	34B	FO0200	J1331 45	23B	FO5202	*J1335 59		FO0200
AIBM114C	J1231 75	35B	FO0200	J1331 47	23A	FO5202	*J1335 62		FO0200
AIBM115C	J1231 77	36B	FO0200	J1331 50	24A	FO5202	*J1335 65		FO0200
AIBNR0	*J1122 66	31A	FO0401	J1130 79	39B	FO5201			
AIB0LA	J1230 50	24A	FO0200	J1230 63	31A	FO0200	*J1340 63	33B	FO0401
AIB0L0	J1233 54	25A	FO0401	*J1339 46	21A	FO0401	J1340 59	31B	FO0400
AIB011U	*J1232 38	18A	FO0200	J1316 52		FO0801			
AIB012U	*J1232 40	19A	FO0200	J1316 29		FO0801			
AIB013U	*J1232 42	20A	FO0200	J1316 25		FO0801			
AIB014U	*J1232 46	21A	FO0200	J1316 10		FO0801			
AIB021U	*J1232 54	26A	FO0200	J1315 52		FO0801			
AIB022U	*J1232 56	28B	FO0200	J1315 29		FO0801			
AIB023U	*J1232 60	28A	FO0200	J1315 25		FO0801			
AIB024U	*J1232 62	29A	FO0200	J1315 10		FO0801			
AIB031U	*J1232 70	34A	FO0200	J1314 52		FO0802			
AIB032U	*J1232 72	35A	FO0200	J1314 29		FO0802			
AIB033U	*J1232 74	36A	FO0200	J1314 25		FO0802			
AIB034U	*J1232 76	37A	FO0200	J1314 10		FO0802			
AIB041U	*J1231 70	34A	FO0200	J1313 52		FO0802			
AIB042U	*J1231 72	35A	FO0200	J1313 29		FO0802			
AIB043U	*J1231 74	36A	FO0200	J1313 10		FO0802	J1313 25		FO0802
AIB044U	J1214 01	02B	FO1000	J1216 34	16A	FO1300	*J1231 76	37A	FO0200
AIBRC1U	*J1226 54	26A	FO0300	J1336 72	35A	FO0300			
AIBRC2U	*J1226 56	28B	FO0300	J1336 77	36B	FO0300			
AIBRC3U	*J1226 60	28A	FO0300	J1336 71	33B	FO0300			
AIBRC4U	*J1226 62	29A	FO0300	J1339 64	30A	FO0300			
AIBRDJQ	*J1229 25	14A	FO0401	J1234 40	19A	FO0401	J1340 68	32A	FO0401
AIBRDKQ	J1122 70	33A	FO0401	*J1229 27	13B	FO0401			
AIBREA	J1214 17	08B	FO0401	J1218 73	37B	FO0402	*J1224 55	29B	FO0402
	J1231 80	38B	FO0200	J1232 50	24A	FO0200	J1232 63	31A	FO0200
	J1232 80	38B	FO0200	J1338 65	34B	FO0401			
AIBRE0V	*J1218 71	36B	FO0402	J1226 61	31B	FO0300	J1229 23	12B	FO0402

Table 5-6. Left Hand Assembly Key Signal L00kup
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Signal	Distribution								
	J1233 71	36A	FO0402	J1233 72	34A	FO0402			
AIBRSD4	*J121075	37B	FO5300	J1211 75		FO5300	J122471	36A	FO0401
	J1226 49	24B	FO0300	J1229 03	03B	FO0102	J1229 17	09B	FO0401
	J1229 71	35B	FO0401	J1230 66	32B	FO0300	J1233 50	23A	FO0401
	J1233 73	36B	FO0402	J1234 20	11A	FO5100	J1234 36	17A	FO0401
	J1234 73	36B	FO0401	J1325 33		FO0401	J1234 36		FO1200
AIBRV0	Jl122 68	32A	FO0401	J1224 53	28B	FO0402	*J1338 66	31A	FO0401
AIBR0J	J1226 64	30A	FO0300	*J1233 74	35B	FO0402	J1336 78	38A	FO0300
AIBT10	J1325 16		FO0401	*J1325 19		FO0401			
AIBUB0V	*J1218 26	12B	FO0401	J1229 33	16B	FO0401			
AIBWAA	J1339 68	32A	FO0402	*J1340 60	28A	FO0402			
AIBWBR	*J1214 19	09B	FO0401	J1224 72	34A	FO0401	J1229 31	15B	FO0401
AIBWBS	J1214 18	10A	FO0401	J1218 27	13B	FO0401	*J1224 74	35B	FO0401
AIBWC1U	*J1230 70	34A	FO0300	J1336 70	34A	FO0300			
AIBWC2U	*J1230 72	35A	FO0300	J1336 75	35B	FO0300			
AIBWC3U	*J1230 74	36A	FO0300	J1336 69	32A	FO0300			
AIBWC4U	*J1230 76	37A	FO0300	J1338 55	29B	FO0300			
AIBWEA	J1218 79	39B	FO0402	*J1224 64	30A	FO0402	J1338 74	35B	FO0401
AIBWE0V	*J1218 80	38B	FO0401	J1229 36	17A	FO0401	J1230 79	37B	FO0300
	J1233 77	38B	FO0402	J1233 79	39B	FO0402	J1234 79	39B	FO0401
	J1335 03		FO0200						
AIBWRJQ	*J1229 42	20A	FO0401	J1340 62	29A	FO0402			
AIBWRKQ	*J1229 39	19B	FO0401	J1340 70	33A	FO0401			
AIBW0J	J1230 78	38A	FO0300	*J1233 78	38A	FO0402	J1336 76	7A	FO0300
AIB4RA	*J1339 60	28A	FO0300	J1340 55	29B	FO0300			
AIB4WA	*J1338 57	30B	FO0300	J1340 53	28B	FO0300			
AICENA	J1215 11	07A	FO1402	*J121606	05A	FO1402			
AICEN0V	*J1215 13	06A	FO1402	J1325 59		FO0701			
AICLDA	*J1216 09	04B	FO1402	J1325 61		FO0701			
AICTCA	J1212 06	05A	FO1402	*J1325 27		FO0701			
AICTC0V	*J1212 08	04A	FO1402	J1214 35	17B	FO1402			
AIRSYK	J1224 14	09A	FO1402	*J1234 35	17B	FO0401			
AI0WTA	J1206 62	29A	FO1402	J1213 75	37B	FO1402	J1214 48	22A	FO1402
	*J1216 38	18A	FO1402						
AI0WT0	*J1214 73	36B	FO1402	J1216 40	19A	FO1402			
ALACKA	*J1206 69	35A	FO0500	J1213 52	24A	FO0901	J1221 48	22A	FO1402.

Table 5-6. Left Hand Assembly Key Signal L00kup
-Continued

Signal				Distribution					
ALB000V	J1119 11	05B	FO0500	*J1215 78	36A	FO0500	J1316 49		FO0801
ALB010V	*J1215 72	34A	FO0500	J1316 50		FO0801			
ALB020V	*J1215 70	34B	FO0500	J1316 27		FO0801			
ALB030V	*J1215 71	36B	FO0500	J1316 07		FO0801			
ALB040V	*J1215 80	38B	FO0500	J1315 49		FO0801			
ALB050V	*J1215 68	32B	FO0500	J1315 50		FO0801			
ALB060V	*J1215 57	30B	FO0500	J1315 27		FO0801			
ALB070V	*J1215 56	28B	FO0500	J1315 07		FO0801			
ALB080V	J1119 61	32B	FO0500	*J1215 60	28A	FO0500	J1314 49		FO0802
ALB090V	*J1215 66	32A	FO0500	J1314 50		FO0802			
ALB100V	*J1215 53	26B	FO0500	J1314 27		FO0802			
ALB110V	*J1215 43	24B	FO0500	J1314 07		FO0802			
ALB120V	*J1215 46	22B	FO0500	J1313 49		FO0802			
ALB130V	*J1215 48	21A	FO0500	J1313 50		FO0802			
ALB140V	*J1215 49	23A	FO0500	J1313 27		FO0802			
ALB150V	*J1215 54	25A	FO0500	J1313 07		FO0802			
ALCAMIX	J1216 19	09B	FO0500	*J1332 36	17A	FO0500			
ALCFJA	J1207 54	26A	FO1200	J1214 53	28B	FO0500	J1215 61	31A	FO0500
	*J1221 76	37A	FO1402						
ALCFJ0V	*J1215 63	30A	FO0500	J1225 78	38A	FO0500	J1234 62	29A	FO0500
ALCFK0	*J1216 21	10B	FO0500	J1234 60	28A	FO0500			
ALCMDD	J03 19		FO0500	J1110 53	28B	FO5000	*J1210 60	28A	FO0500
ALCMFJ	J1119 13	06B	FO0500	J1210 62	29A	FO0500	*J1234 55	29B	FO0500
ALCMFK	J1206 73	36B	FO0500	*J1234 57	30B	FO0500			
ALCNCNA	J1225 70	34A	FO0500	*J1235 17	08B	FO0500			
ALCNCNB	J1225 69	34B	FO0500	*J1235 18	09A	FO0500			
ALCNCNC	J1225 71	35B	FO0500	*J1235 15	07B	FO0500			
ALCNR0E	*J1225 75	37B	FO0500	J1332 40	19A	FO0500			
ALCNR1E	*J1225 79	39B	FO0500	J1332 42	20A	FO0500			
ALCNR2E	*J1225 80	39A	FO0500	J1332 46	21A	FO0500			
ALEFJ0	*J1216 75	37B	FO0500	J1234 68	32A	FO0500			
ALEFK0	*J1220 01	02B	FO0500	J1234 70	33A	FO0500			
ALENAD	J03 21		FO0500	*J1210 66	31A	FO0500			
ALENFJ	J1112 70	33A	FO5002	J1116 14	09A	FO5002	J111670	33A	FO5002
	J1206 06	05A	FO5002	J1210 68	32A	FO0500	*J1234 61	32B	FO0500
ALENFK	J1206 72	34A	FO0500	*J1234 59	31B	FO0500			

Table 5-6. Left Hand Assembly Key Signal L00kup
-Continued

Signal	Distribution								
ALIAJA	*J1214 63	33B	FO0500	J1216 79	39B	FO0500			
ALINDB4	J03 43		FO4200	*J1112 66	31A	FO5002	*J1127 06	05A	FO5002
	J1220 04	04A	FO0500	J1222 65		FO5002			
ALI00B	J03 23		FO0500	J1124 03	02B	FO5201	*J1127 01	02B	FO5002
	J1128 72	35A	FO5001	*J1210 51	27B	FO0500	J1211 23		FO0500
	J1341 76	37A	FO0500						
ALI01B	J03 24		FO0500	J1124 05	03B	FO5201	*J1127 09	04B	FO5002
	J1128 70	34A	FO5001	*J1210 45	24B	FO0500	J1211 25		FO0500
	J1341 70	34A	FO0500						
ALI02B	J03 25		FO0500	J1124 07	04B	FO5201	*J1127 15	07B	FO5002
	J1128 69	34B	FO5001	*J1210 46	21A	FO0500	J1211 29		FO0500
	J1341 75	35B	FO0500						
ALI03B	J03 26		FO0500	J1124 09	05B	FO5201	*J1127 22	12A	FO5002
	J112871	35B	FO5001	*J1210 52	24A	FO0500	J1211 42		FO0500
	J1341 69	32A	FO0500						
ALI04B	J03 27		FO0500	J1124 11	06B	FO5201	*J1127 14	09A	FO5002
	J112972	35A	FO5001	*J1210 39	19B	FO0500	J1211 46		FO0500
	J1215 79	39B	FO0500						
ALI05B	J03 28		FO0500	J1124 15	07B	FO5201	*J1127 21	10B	FO5002
	J1129 70	34A	FO5001	*J1210 33	16B	FO0500	J1211 35		FO0500
	J1215 65	33B	FO0500						
ALI06B	J03 29		FO0500	J1124 18	09A	FO5201	*J1127 27	13B	FO5002
	J1129 69	34B	FO5001	*J1210 30	15A	FO0500	J1211 37		FO0500
	J1215 59	31B	FO0500						
ALI07B	J03 30		FO0500	J1124 17	08B	FO5201	*J1127 38	18A	FO5002
	J1129 71	35B	FO5001	*J121038	18A	FO0500	J1211 39		FO0500
	J1215 55	29B	FO0500						
ALI08B	J03 31		FO0500	J1118 23	00B	FO5002	J1124 19	09B	FO5201
	*J1127 30	15A	FO5002	J1128 60	29A	FO5001	*J1210 27	13B	FO0500
	J1211 52		FO0500	J1215 62	29A	FO0500			
ALI09B	J03 32		FO0500	J1124 21	10B	FO5201	*J1127 33	16B	FO5002
	J1128 57	28A	FO5001	*J1210 21	10B	FO0500	J1211 48		FO0500
	J1215 64	33A	FO0500						
ALI10B	J03 33		FO0500	J1124 23	11B	FO5201	*J1127 39	19B	FO5002
	J1128 53	28B	FO5001	*J1210 14	09A	FO0500	J1211 47		FO0500
	J1215 51	27B	FO0500						

Table 5-6. Left Hand Assembly Key Signal L00kup
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Signal	Distribution									
ALI11B	J03	34		FO0500	J1124	25	12B	FO5201	*J1127 52	24A	FO5002
	J1128	55	29B	FO5001	*J1210	22	12A	FO0500	J1211 45		FO0500
	J1215	45	25B	FO0500							
ALI12B	J03	35		FO0500	*J1124	29	13B	FO5201	*J1127 46	21A	FO5002
	J1129	60	29A	FO5001	*J1210	15	07B	FO0500	J1211 41		FO0500
	J1215	41	23B	FO0500							
ALI13B	J03	36		FO0500	J1124	31	14B	FO5201	*J1127 45	24B	FO5002
	J1129	57	28A	FO5001	*J1210	09	04B	FO0500	J1211 62		FO0500
	J1215	50	22A	FO0500							
ALI14B	J03	37		FO0500	J1124	34	15B	FO5201	*J1127 51	27B	FO5002
	J1129	53	28B	FO5001	*J1210	01	02B	FO0500	J1211 56		FO0500
	J1215	47	24A	FO0500							
ALI15B	J03	38		FO0500	J1124	33	16A	FO5201	*J1127 66	31A	FO5002
	J1129	55	29B	FO5001	*J1210	06	05A	FO0500	J1211 55		FO0500
	J1215	52	26A	FO0500							
ALRM1TA	J1215	73	37B	FO0500	*J1341	73	34B	FO0500			
ALRM1TB	J1215	69	35B	FO0500	*J1341	79	37B	FO0500			
ALRM1TC	J1215	74	35A	FO0500	*J1341	74	36A	FO0500			
ALRM1TD	J1215	76	37A	FO0500	*J1341	80	38B	FO0500			
ALRQRA	J1214	61	32B	FO0500	*J1217	27	13B	FO1402	J1218 21	11B	FO0500
ALRQR0V	*J1218	19	10B	FO0500	J1341	66	32B	FO0500			
AL0EBJ	J1210	05	03B	FO0500	J1210	07	03A	FO0500	J1210 10	07A	FO0500
	J1210	13	06B	FO0500	J1210	19	09B	FO0500	J1210 20	11A	FO0500
	J1210	25	12B	FO0500	J1210	26	14A	FO0500	*J1233 07	03A	FO0500
AL0ECJ	J1210	31	15B	FO0500	J1210	36	17A	FO0500	J1210 37	18B	FO0500
	J1210	42	20A	FO0500	J1210	43	23B	FO0500	J1210 49	26B	FO0500
	J1210	50	23A	FO0500	J1210	56	26A	FO0500	*J1233 13	06B	FO0500
AL0ED0	J1206	71	36A	FO0500	J1210	64	30A	FO0500	J1214 60	28A	FO0500
	*J1216	45	24B	FO1402	J1221	75	37B	FO1402	J1233 05	03B	FO0500
	J1233	08	06A	FO0500							
AL0EEA	*J1220	45	24B	FO0500	J1233	01	02B	FO0500	J1233 10	07A	FO0500
AL0EJA	*J1214	55	29B	FO0500	J1216	77	38B	FO0500			
AL000D	*J1210	51	27B	FO0500							
AL001D	*J1210	45	24B	FO0500							
AL002D	*J1210	46	21A	FO0500							
AL003D	*J1210	52	24A	FO0500							

Table 5-6. Left Hand Assembly Key Signal Lookup
-Continued

Signal				Distribution					
AL004D	*J1210 39	19B	FO0500						
AL005D	*J1210 33	16B	FO0500						
AL006D	*J1210 30	15A	FO0500						
AL007D	*J1210 38	18A	FO0500						
AL008D	*J1210 27	13B	FO0500						
AL009D	*J1210 21	10B	FO0500						
AL010D	*J1210 14	09A	FO0500						
AL011D	*J1210 22	12A	FO0500						
AL012D	*J1210 15	07B	FO0500						
AL013D	*J1210 09	04B	FO0500						
AL014D	*J1210 01	02B	FO0500						
AL015D	*J1210 06	05A	FO0500						
AMCCR1U	J1208 64	30A	FO0601	*J1226 70	34A	FO1200			
AMCCR2U	J1208 56	28B	FO0601	*J1226 72	35A	FO1200			
AMCD1A	J1218 35	18A	FO1200	*J1224 31	15B	FO1200			
AMCD10V	*J1218 37	17A	FO1200	J1230 20	10A	FO1200			
AMCD20	*J1219 46	21A	FO1200	J123022	11A	FO1200			
AMCM11X	J1224 29	14B	FO1200	*J1332 04	02A	FO1200			
AMCM21X	J1224 33	16B	FO1200	*J1332 20	I0A	FO1200			
AMCRLA	*J1217 36	17A	FO1402	J1226 80	38B	FO1200	J1227 80	38B	FO1200
AMC0BA	J1219 50	23A	FO1200	*J1224 27	13B	FO1200			
AMC2GA	J1219 48	22A	FO1200	*J1224 39	19B	FO1200			
AMFSD0T	J1224 46	21A	FO1200	J1224 54	25A	FO1200	*J1230 24	12A	FO1200
AMFSD1T	J1224 41	22B	FO1200	J1227 77	36B	FO1200	*J1230 26	13A	FO1200
AMFSD2T	J1224 56	26A	FO1200	J1226 71	33B	FO1200	J1227 75	35B	FO1200
	*J1230 27	14A	FO1200						
AMFSD3T	J1224 48	22A	FO1200	J1224 52	24A	FO1200	*J1230 30	15A	FO1200
AMFSR1U	J1208 78	38A	FO0601	*J1227 70	34A	FO1200			
AMFSR2U	J1208 72	35A	FO0601	*J1227 72	35A	FO1200			
AMFSR3U	J1208 77	36B	FO0601	*J1227 74	36A	FO1200			
AMFSR4U	J1208 71	33B	FO0601	*J1227 76	37A	FO1200			
AMPS0A	*J1224 50	23A	FO1200	*J1227 71	33B	FO1200			
AMPS1A	*J1224 43	23B	FO1200	J1227 73	34B	FO1200			
AMRSTAV	J05 60		FO5300	*J1218 40	19A	FO5300	J1221 24	13A	FO1200
	J1227 49	24B	FO0901	J1228 35	16B	FO0901	J1228 66	32B	FO0901
	J1233 36	17A	FO1000	J1234 64	30A	FO0500			

Table 5-6. Left Hand Assembly Key Signal L00kup
-Continued

Signal			Distribution						
AMWRK0	*J1119 66	31A	FO5402	J1320 01		FO0702	J1321 01		FO0702
	J1322 01		FO0702	J1323 01		FO0702	J1335 01		FO0200
A0RLDA	J1215 23	12A	FO0601	*J1216 22	12A	FO1401			
A0RLD0V	*J1215 25	11A	FO0601	J1313 79		FO0603	J1314 79		FO0602
	J1315 79		FO0602	J1316 79		FO0601			
A0RSB0	*J1216 63	33B	FO0601	J1313 63		FO0603	J1314 63		FO0602
	J1315 63		FO0602	J1316 63		FO0601			
A0RSHA	*J1214 36	17A	FO0601	J1218 17	09B	FO0601			
A0RSH0V	*J1218 14	08B	FO0601	J1313 78		FO0603	J1314 78		FO0602
	J1315 78		FO0602	J1316 78		FO0601			
A0RSIA	J1215 22	14A	FO0601	*J1216 27	13B	FO0601			
A0RSI0V	*J1215 24	13A	FO0601	J1316 39		FO0601			
A0R15AV	*J1212 42	18B	FO0601	J1312 37		FO0601			
APACB0	*J1214 64	30A	FO0901	J1216 04	04A	FO0901			
APACC0	*J1213 47	25B	FO0901	J1227 61	31B	FO0901	J1228 47	23A	FO0901
	J1228 79	37B	FO0901						
APACLA	*J1216 01	02B	FO0901	J1227 63	31A	FO0901	J11228 50	24A	FO0901
	J1228 80	38B	FO0901						
APAC11U	*J1228 38	18A	FO0901	J1316 51		FO0801	J1338 34	16A	FO0901
	J1341 19	09B	FO5202						
APAC12U	*J1228 40	19A	FO0901	J1316 34		FO0801	J1338 29	14B	FO0901
	J1341 21	10B	FO5202						
APAC13U	*J1228 42	20A	FO0901	J1l316 46		FO0801	J1338 35	17B	FO0901
	J1341 23	1IB	FO5202						
APAC14U	*J1228 46	21A	FO0901	J1316 14		FO0801	J1338 48	22A	FO0901
	J1341 25	12B	FO5202						
APAC15U	J1227 64	30A	FO0901	*J1228 36	17A	FO0901			
APAC21U	*J1227 54	26A	FO0901	J1315 51		FO0801	J1338 41	22B	FO0901
	J1341 29	13B	FO5202						
APAC22U	*J1227 56	28B	FO0901	J1315 34		FO0801	J1338 47	25B	FO0901
	J1341 31	14B	FO5202						
APAC23U	J1226 20	10A	FO0901	*J1227 60	28A	FO0901	J1315 46		FO0801
	J1341 34	15B	FO5202						
APAC24U	J1226 22	11A	FO0901	*J1227 62	29A	FO0901	J1315 14		FO0801
	J1341 33	16A	FO5202						
APAC25U	*J1227 52	25A	FO0901	J1228 78	38A	FO0901			

Table 5-6. Left Hand Assembly Key Signal L00kup
-Continued

Signal			Distribution						
APAC31U	J1226 19	09B	FO0901	*J1228 70	34A	FO0901	1314 51		FO0802
	J1327 03	02B	FO5202						
APAC32U	*J1228 72	35A	FO0901	J1314 34		FO0802	J1327 05	03B	FO5202
	J1327 49	24B	FO0901	J1327 66	32B	FO0901	J1332 49	24B	FO0901
	J1332 66	32B	FO0901						
APADC0T	*J1226 24	12A	FO0901	J1339 29	14B	FO0901			
APADC1T	*J1226 26	13A	FO0901	J1339 35	17B	FO0901			
APADC2T	*J1226 27	14A	FO0901	J1340 35	17B	FO0901			
APADC3T	*J1226 30	15A	FO0901	J1340 47	25B	FO0901			
APADC4T	*J1226 33	16A	FO0901	J1339 47	25B	FO0901			
APADC5T	*J1226 23	11B	FO0901	J1339 53	28B	FO0901			
APADC6T	*J1226 25	12B	FO0901	J1339 59	31B	FO0901			
APADC7T	*J1226 29	13B	FO0901	J1339 76	37A	FO0901			
APAD00	J1326 29		FO0901	J1329 29		FO0901	J1330 20		FO0901
	J1333 29		FO0901	*J1339 33	16B	FO0901			
APAD10	J1326 31		FO0901	J1329 31		FO0901	J1330 31		FO0901
	J1333 31		FO0901	*J1339 39	19B	FO0901			
APAD20	J1326 80		FO0901	*J1329 80		FO0901	J1330 80		FO0901
	J1333 80		FO0901	*J1340 39	19B	FO0901			
APAD30	J1326 43		FO0901	J1329 43		FO0901	J1330 43		FO0901
	J1333 43		FO0901	*J1340 51	27B	FO0901			
APAD40	J1326 27		FO0901	J1329 27		FO0901	J1330 27		FO0901
	J1333 27		FO0901	*J1339 51	27B	FO0901			
APAD50	J1326 48		FO0901	J1329 48		FO0901	J1330 48		FO0901
	J1333 48		FO0901	*J1339 57	30B	FO0901			
APAD60	J1326 63		FO0901	J1329 63		FO0901	J1330 63		FO0901
	J1333 63		FO0901	*J1339 63	33B	FO0901			
APAD70	J1326 17		FO0901	*J1329 17		FO0901	J1330 17		FO0901
	J1333 17		FO0901	*J1339 80	39A	FO0901			
APA0BA	J1326 08		FO0901	J1326 38		FO0901	J1326 60		FO0901
	J1329 08		FO0901	J1329 38		FO0901	J1329 60		FO0901
	J1330 08		FO0901	J1330 38		FO0901	J1330 60		FO0901
	J1333 08		FO0901	J1333 38		FO0901	J1333 60		FO0901
	*J1338 30	15A	FO0901						
APA1BA	J1326 09		FO0901	J1326 35		FO0901	J1326 61		FO0901
	J1329 09		FO0901	J1329 35		FO0901	J1329 61		FO0901

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Table 5-6. Left Hand Assembly Key Signal L00kup
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Signal			Distribution					
	J1330 09		FO0901	J1330 35		FO0901	J1330 61	FO0901
	J1333 09		FO0901	J1333 35		FO0901	J1333 61	FO0901
	*J1338 33	16B	FO0901					
APA2BA	J1326 10		FO0901	J1326 39		FO0901	J1326 62	FO0901
	J1329 10		FO0901	J1329 39		FO0901	J1329 62	FO0901
	J1330 10		FO0901	J1330 39		FO0901	J1330 62	FO0901
	J1333 10		FO0901	J1333 39		FO0901	J1333 62	FO0901
	*J1338 39	19B	FO0901					
APA3BA	J1326 18		FO0901	J1326 36		FO0901	J1326 64	FO0901
	J1329 18		FO0901	J1329 36		FO0901	J1329 64	FO0901
	J1330 18		FO0901	J1330 36		FO0901	J1330 64	FO0901
	J1333 18		FO0901	J1333 36		FO0901	J1333 64	FO0901
	*J1338 46	21A	FO0901					
APA4BA	J1326 23		FO0901	J1326 40		FO0901	J1326 70	FO0901
	J1329 23		FO0901	J1329 40		FO0901	J1329 70	FO0901
	J1330 23		FO0901	J1330 40		FO0901	J1330 70	FO0901
	J1333 23		FO0901	J1333 40		FO0901	J1333 70	FO0901
	*J1338 45	24B	FO0901					
APA5BA	J1326 24		FO0901	J1326 37		FO0901	J1326 72	FO0901
	J1329 24		FO0901	J1329 37		FO0901	J1329 72	FO0901
	J1330 24		FO0901	J1330 37		FO0901	J1330 72	FO0901
	J1333 24		FO0901	J1333 37		FO0901	J1333 72	FO0901
	*J1338 51	27B	FO0901					
APBHL0	*J1122 33	16B	FO0602	J1123 18	09A	FO5202	J1123 43	22B FO5202
APBHM0	*J1122 39	19B	FO0603	J1123 17	08B	FO5202	J1123 45	23B FO5202
APCM1TA	J1328 25	12B	FO5202	J1331 51	25B	FO0902	*J1332 55	27B FO0901
APCM1TB	J1328 23	11B	FO5202	J1331 57	29B	FO0902	*J1332 61	31B FO0901
APCM1TC	J1328 21	10B	FO5202	J1331 54	26A	FO0902	*J1332 60	28A FO0901
APCM1TD	J1328 19	09B	FO5202	J1331 62	29A	FO0902	*J1332 63	31A FO0901
APCM2TA	J1328 33	16A	FO5202	J1331 69	32A	FO0902	*J1332 73	34B FO0901
APCM2TB	.11328 34	15B	FO5202	J1331 75	35B	FO0902	*J1332 79	37B FO0901
APCM2TC	J1328 31	14B	FO5202	J1331 70	34A	FO0902	*J1332 74	36A FO0901
APCM2TD	J1328 29	13B	FO5202	J1331 76	37A	FO0902	*J1332 80	38B FO0901
APCM3TA	*J1327 55	27B	FO0901	J1328 41	19B	FO5202	J1328 51	25B FO0901
APCM3TB	*J1327 61	31B	FO0901	J1328 39	18B	FO5202	J1328 57	29B FO0901
APCM3TC	*J1327 60	28A	FO0901	J1328 37	17B	FO5202	J1328 54	26A FO0901

Table 5-6. Left Hand Assembly Key Signal L00kup
-Continued

Signal				Distribution					
APCM3TD	*J1327 63	31A	FO0901	J1328 35	16B	FO5202	J1328 62	29A	FO0901
APCM4TA	*J1327 73	34B	FO0901	J1328 50	24A	FO5202	J1328 69	32A	FO0901
APCM4TB	*J1327 79	37B	FO0901	J1328 47	23A	FO5202	J1328 75	35B	FO0901
APCM4TC	*J1327 74	36A	FO0901	J1328 45	23B	FO5202	J1328 70	34A	FO0901
APCM4TD	*J1327 80	38B	FO0901	J1328 43	22B	FO5202	J1328 76	37A	FO0901
APML100B	*J1333 59		FO0901						
APML101B	*J1333 57		FO0901						
APML102B	*J1333 56		FO0901						
APML103B	*J1333 55		FO0901						
APML104B	*J1333 65		FO0901						
APML105B	*J1333 66		FO0901						
APML106B	*J1333 68		FO0901						
APML107B	*J1333 69		FO0901						
APML140B	*J1333 13		FO0901						
APML141B	*J1333 11		FO0901						
APML142B	*J1333 15		FO0901						
APML143B	*J1333 14		FO0901						
APML144B	*J1333 22		FO0901						
APML145B	*J1333 19		FO0901						
APML146B	*J1333 21		FO0901						
APML147B	*J1333 20		FO0901						
APML150B	*J1333 46		FO0901						
APML151B	*J1333 47		FO0901						
APML152B	*J1333 74		FO0901						
APML153B	*J1333 75		FO0901						
APML154B	*J1333 76		FO0901						
APML155B	*J1333 77		FO0901						
APML156B	*J1333 78		FO0901						
APML157B	*J1333 79		FO0901						
APML160B	*J1333 49		FO0901						
APML161B	*J1333 50		FO0901						
APML162B	*J1333 51		FO0901						
APML163B	*J1333 52		FO0901						
APML164B	*J1333 53		FO0901						
APML165B	*J1333 54		FO0901						
APML166B	*J1333 71		FO0901						

Table 5-6. Left Hand Assembly Key Signal L00kup
-Continued

Signal		Distribution
APML167B	*J1333 73	FO0901
APML170B	*J1333 01	FO0901
APML171B	*J1333 03	FO0901
APML172B	*J1333 04	FO0901
APML173B	*J1333 05	FO0901
APML174B	*J1333 06	FO0901
APML175B	*J1333 07	FO0901
APML176B	*J1333 25	FO0901
APML177B	*J1333 26	FO0901
APML200B	*J1330 59	FO0901
APML201B	*J1330 57	FO0901
APML202B	*J1330 56	FO0901
APML203B	*J1330 55	FO0901
APML204B	*J1330 65	FO0901
APML205B	*J1330 66	FO0901
APML206B	*J1330 68	FO0901
APML207B	*J1330 69	FO0901
APML240B	*J1330 13	FO0901
APML241B	*J1330 11	FO0901
APML242B	*J1330 15	FO0901
APML243B	*J1330 14	FO0901
APML244B	*J1330 22	FO0901
APML245B	*J1330 19	FO0901
APML246B	*J1330 21	FO0901
APML247B	*J1330 20	FO0901
APML250B	*J1330 46	FO0901
APML251B	*J1330 47	FO0901
APML252B	*J1330 74	FO0901
APML253B	*J1330 75	FO0901
APML254B	*J1330 76	FO0901
APML255B	*J1330 77	FO0901
APML256B	*J1330 78	FO0901
APML257B	*J1330 79	FO0901
APML260B	*J1330 49	FO0901
APML261B	*J1330 50	FO0901
APML262B	*J1330 51	FO0901

Table 5-6. Left Hand Assembly Key Signal L00kup
-Continued

Signal		Distribution
APML263B	*J1330 52	FO0901
APML264B	*J1330 53	FO0901
APML265B	*J1330 54	FO0901
APML266B	*J1330 71	FO0901
APML267B	*J1330 73	FO0901
APML270B	*J1330 01	FO0901
APML271B	*J1330 03	FO0901
APML272B	*J1330 04	FO0901
APML273B	*J1330 05	FO0901
APML274B	*J1330 06	FO0901
APML275B	*J1330 07	FO0901
APML276B	*J1330 25	FO0901
APML277B	*J1330 26	FO0901
APMM100B	*J1329 59	FO0901
APMM101B	*J1329 57	FO0901
APMM102B	*J1329 56	FO0901
APMM103B	*J1329 55	FO0901
APMM104B	*J1329 65	FO0901
APMM105B	*J1329 66	FO0901
APMM106B	*J1329 68	FO0901
APMM107B	*J1329 69	FO0901
APMM140B	*J1329 13	FO0901
APMM141B	*J1329 11	FO0901
APMM142B	*J1329 15	FO0901
APMM143B	*J1329 14	FO0901
APMM144B	*J1329 22	FO0901
APMM145B	*J1329 19	FO0901
APMM146B	*J1329 21	FO0901
APMM147B	*J1329 20	FO0901
APMM150B	*J1329 46	FO0901
APMM151B	*J1329 47	FO0901
APMM152B	*J1329 74	FO0901
APMM153B	*J1329 75	FO0901
APMM154B	*J1329 76	FO0901
APMM155B	*J1329 77	FO0901
APMM156B	*J1329 78	FO0901

Table 5-6. Left Hand Assembly Key Signal L00kup
-Continued

Signal		Distribution
APMM157B	*J1329 79	FO0901
APMM160B	*J1329 49	FO0901
APMM161B	*J1329 50	FO0901
APMM162B	*J1329 51	FO0901
APMM163B	*J1329 52	FO0901
APMM164B	*J1329 53	FO0901
APMM165B	*J1329 54	FO0901
APMM166B	*J1329 71	FO0901
APMM167B	*J1329 73	FO0901
APMM170B	*J1329 01	FO0901
APMM171B	*J1329 03	FO0901
APMM172B	*J1329 04	FO0901
APMM173B	*J1329 05	FO0901
APMM174B	*J1329 06	FO0901
APMM175B	*J1329 07	FO0901
APMM176B	*J1329 25	FO0901
APMM177B	*J1329 26	FO0901
APMM200B	*J1326 59	FO0901
APMM201B	*J1326 57	FO0901
APMM202B	*J1326 56	FO0901
APMM203B	*J1326 55	FO0901
APMM204B	*J1326 65	FO0901
APMM205B	*J1326 66	FO0901
APMM206B	*J1326 68	FO0901
APMM207B	*J1326 69	FO0901
APMM240B	*J1326 13	FO0901
APMM241B	*J1326 11	FO0901
APMM242B	*J1326 15	FO0901
APMM243B	*J1326 14	FO0901
APMM244B	*J1326 22	FO0901
APMM245B	*J1326 19	FO0901
APMM246B	*J1326 21	FO0901
APMM247B	*J1326 20	FO0901
APMM250B	*J1326 46	FO0901
APMM251B	*J1326 47	FO0901
APMM252B	*J1326 74	FO0901

Table 5-6. Left Hand Assembly Key Signal L00kup
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Signal		Distribution					
APMM253B	*J1326 75	FO0901					
APMM254B	*J1326 76	FO0901					
APMM255B	*J1326 77	FO0901					
APMM256B	*J1326 78	FO0901					
APMM257B	*J1326 79	FO0901					
APMM260B	*J1326 49	FO0901					
APMM261B	*J1326 50	FO0901					
APMM262B	*J1326 51	FO0901					
APMM263B	*J1326 52	FO0901					
APMM264B	*J1326 53	FO0901					
APMM265B	*J1326 54	FO0901					
APMM266B	*J1326 71	FO0901					
APMM267B	*J1326 73	FO0901					
APMM270B	*J1326 01	FO0901					
APMM271B	*J1326 03	FO0901					
APMM272B	*J1326 04	FO0901					
APMM273B	*J1326 05	FO0901					
APMM274B	*J1326 06	FO0901					
APMM275B	*J1326 07	FO0901					
APMM276B	*J1326 25	FO0901					
APMM277B	*J1326 26	FO0901					
AP100B	*J1332 62	29A	FO0901	*J1333 01	FO0901	*J1333 13	FO0901
	*J1333 46		FO0901	*J1333 49	FO0901	*J1333 59	FO0901
AP101B	J1332 54	26A	FO0901	*J1333 03	FO0901	*J1333 11	FO0901
	*J1333 47		FO0901	*J1333 50	FO0901	*J1333 57	FO0901
AP102B	J1332 57	29B	FO0901	*J1333 04	FO0901	*J1333 15	FO0901
	*J1333 51		FO0901	*J1333 56	FO0901	*J1333 74	FO0901
AP103B	J1332 51	25B	FO0901	*J1333 05	FO0901	*J1333 14	FO0901
	*J1333 52		FO0901	*J1333 55	FO0901	*J1333 75	FO0901
AP104B	J1332 76	37A	FO0901	*J1333 06	FO0901	*J1333 22	FO0901
	*J1333 53		FO0901	*J1333 65	FO0901	*J1333 76	FO0901
AP105B	J1332 70	34A	FO0901	*J1333 07	FO0901	*J1333 19	FO0901
	*J1333 54		FO0901	*J1333 66	FO0901	*J1333 77	FO0901
AP106B	J1332 75	35B	FO0901	*J1333 21	FO0901	*J1333 25	FO0901
	*J1333 68		FO0901	*J1333 71	FO0901	*J1333 78	FO0901
AP107B	J1332 69	32A	FO0901	*J1333 20	FO0901	*J1333 26	FO0901

Table 5-6. Left Hand Assembly Key Signal L00kup
-Continued

Signal			Distribution					
	*J1333 69		FO0901	*J1333 73	FO0901	*J1333 79		FO0901
AP108B	J1327 62	29A	FO0901	*J1329 01	FO0901	*J1329 13		FO0901
	*J1329 46		FO0901	*J1329 49	FO0901	*J1329 59		FO0901
AP109B	J1327 54	26A	FO0901	*J1329 03	FO0901	*J1329 11		FO0901
	*J1329 47		FO0901	*J1329 50	FO0901	*J1329 57		FO0901
AP110B	J1327 57	29B	FO0901	*J1329 04	FO0901	*J1329 15		FO0901
	*J1329 51		FO0901	*J1329 56	FO0901	*J1329 74		FO0901
AP111B	J1327 51	25B	FO0901	*J1329 05	FO0901	*J1329 14		FO0901
	*J1329 52		FO0901	*J1329 55	FO0901	*J1329 75		FO0901
AP112B	J1327 76	37A	FO0901	*J1329 06	FO0901	*J1329 22		FO0901
	*J1329 53		FO0901	*J1329 65	FO0901	*J1329 76		FO0901
AP113B	J1327 70	34A	FO0901	*J1329 07	FO0901	*J1329 19		FO0901
	*J1329 54		FO0901	*J1329 66	FO0901	*J1329 77		FO0901
API14B	J1327 75	35B	FO0901	*J1329 21	FO0901	*J1329 25		FO0901
	*J1329 68		FO0901	*J1329 71	FO0901	*J1329 78		FO0901
AP115B	J1327 69	32A	FO0901	*J1329 20	FO0901	*J1329 26		FO0901
	*J1329 69		FO0901	*J1329 73	FO0901	*J1329 79		FO0901
AP200B	*J1330 01		FO0901	*J1330 13	FO0901	*J1330 46		FO0901
	*J1330 49		FO0901	*J1330 59	FO0901	J1332 64	30A	FO0901
AP201B	*J1330 03		FO0901	*J1330 11	FO0901	*J1330 47		FO0901
	*J1330 50		FO0901	*J1330 57	FO0901	J1332 56	28B	FO0901
AP202B	*J1330 04		FO0901	*J1330 15	FO0901	*J1330 51		FO0901
	*J1330 56		FO0901	*J1330 74	FO0901	J1332 59	30B	FO0901
AP203B	*J1330 05		FO0901	*J1330 14	FO0901	*J1330 52		FO0901
	*J1330 55		FO0901	*J1330 75	FO0901	J1332 53	26B	FO0901
AP204B	*J1330 06		FO0901	*J1330 22	FO0901	*J1330 53		FO0901
	*J1330 65		FO0901	*J1330 76	FO0901	J1332 78	38A	FO0901
AP205B	*J1330 07		FO0901	*J1330 19	FO0901	*J1330 54		FO0901
	*J1330 66		FO0901	*J1330 77	FO0901	J1332 72	35A	FO0901
AP206B	*J1330 21		FO0901	*J1330 25	FO0901	*J1330 68		FO0901
	*J1330 71		FO0901	*J1330 78	FO0901	J1332 77	36B	FO0901
AP207B	*J1330 20		FO0901	*J1330 26	FO0901	*J1330 69		FO0901
	*J1330 73		FO0901	*J1330 79	FO0901	J1332 71	33B	FO0901
AP208B	*J1326 01		FO0901	*J1326 13	FO0901	*J1326 46		FO0901
	*J1326 49		FO0901	*J1326 59	FO0901	J1327 64	30A	FO0901
AP209B	*J1326 03		FO0901	*J1326 11	FO0901	*J1326 47		FO0901

Table 5-6. Left Hand Assembly Key Signal L00kup
-Continued

Signal			Distribution						
	*J1326 50		FO0901	*J1326 57		FO0901	*J1327 56	28B	FO0901
AP210B	*J1326 04		FO0901	*J1326 15		FO0901	*J1326 51		FO0901
	*J1326 56		FO0901	*J1326 74		FO0901	J1327 59	30B	FO0901
AP211B	*J1326 05		FO0901	*J1326 14		FO0901	*J1326 52		FO0901
	*J1326 55		FO0901	*J1326 75		FO0901	J1327 53	26B	FO0901
AP212B	*J1326 06		FO0901	*J1326 22		FO0901	*J1326 53		FO0901
	*J1326 65		FO0901	*J1326 76		FO0901	J1327 78	38A	FO0901
AP213B	*J1326 07		FO0901	*J1326 19		FO0901	*J1326 54		FO0901
	*J1326 66		FO0901	*J1326 77		FO0901	J1327 72	35A	FO0901
AP214B	*J1326 21		FO0901	*J1326 25		FO0901	*J1326 68		FO0901
	*J1326 71		FO0901	*J1326 78		FO0901	J1327 77	36B	FO0901
AP215B	*J1326 20		FO0901	*J1326 26		FO0901	*J1326 69		FO0901
	*J1326 73		FO0901	*J1326 79		FO0901	J1327 71	33B	FO0901
ARIBRA	J1215 38	20A	FO0401	*J1221 35	17B	FO0401			
ARIBR0V	*J1215 40	19A	FO0401	J1229 24	12A	FO0401	J1234 42	20A	FO0401
	J1334 04		FO1300						
ASKBWA	J1213 50	23A	FO0901	*J1214 80	39A	FO1402	J1221 46	21A	FO1402
ASKDFA	J1213 48	22A	FO0901	*J1312 62		FO0603			
ASKDIA	J1213 46	21A	FO0901	*J1214 39	19B	FO1402	J1317 72	34A	FO1402
ASKMCA	J1213 49	26B	FO0901	J1221 43	23B	FO1402	J1312 45		FO1401
ASKTSA	J1213 43	23B	FO0901	*J1214 31	15B	FO1401	J1317 71	36A	FO1402
ASTFL0	J1214 29	14B	FO1401	*J1334 80		FO300			
ASW07J	J1115 48	22A	FO5002	*J1334 26		FO1300			
ASW08K	J1117 69	35B	FO5002	*J1334 11		FO1300			
AT1FFJ	J1206 64	30A	FO1402	J1213 71	36A	FO1402	J1219 54	25A	FO1200
	*J1234 49	26B	FO1200						
AT1FFK	J1219 24	13A	FO1200	*J1234 47	25B	FO1200			
AT1G0A	J1214 46	21A	FO1402	J1218 29	15B	FO1402	*J1221 09	04B	FO1402
AT1G00V	J1216 10	07A	FO1402	J1216 29	14B	FO1401	J1217 30	15A	FO1401
	*J1218 30	14B	FO1402	J1220 37	18B	FO1401	J1220 74	35B	FO1401
	J1221 54	25A	FO1402						
AT1NBA	J1218 39	19B	FO1200	*J1219 52	24A	FO1200			
AT1NB0V	J1214 41	22B	FO1402	*J1218 42	18B	FO1200	J1221 01	02B	FO1402
	J1312 54		FO1500						
AT1VBA	*J1206 57	30B	FO1402	J1220 19	09B	FO1402			
AT1VB0	J1206 68	32A	FO1000	J1214 59	31B	FO0500	J1214 62	29A	FO0500

Table 5-6. Left Hand Assembly Key Signal L00kup
-Continued

Signal	Distribution								
	J1216 03	02A	FO1402	J1216 05	03B	FO0901	J1220 26	14A	FO1401
	J1216 53	28B	FO1200	J1219 35	17B	FO1402	J1219 70	33A	FO1200
	*J1220 21	10B	FO1402	J1221 77	38B	FO1402			
AT1WTA	J1134 52	26A	FO5201	J1206 60	28A	FO1402	J1213 73	36B	FO1402
	*J1214 43	23B	FO1402	J1217 42	20A	FO1402			
AT1WT0V	J1133 65	34B	FO5201	*J1134 54	25A	FO5201			
AT2FFJ	J1206 74	35B	FO0500	J1214 42	20A	FO0601	J1214 76	37A	FO1402
	J1217 01	02B	FO0601	J1217 09	04B	FO1200	J1217 56	26A	FO0601
	J1219 08	06A	FO1200	J1219 41	22B	FO1200	J1220 40	19A	FO1200
	*J1234 43	23B	FO1200	J1312 18		FO0603	J1312 18		FO1402
AT2FFK	J1219 26	14A	FO1200	*J1234 45	24B	FO1200			
AT2FJA	J1214 06	05A	FO1200	*J1216 57	30B	FO1200			
AT2FJ0	*J1214 04	04A	FO1200	J1234 48	22A	FO1200	J1234 56	26A	FO1200
AT2NBA	J1212 35	18A	FO1200	*J1219 06	05A	FO1200			
AT2NB0V	*J1212 37	17A	FO1200	J1221 66	31A	FO1401			
AT2XBA	J1218 47	24A	FO1200	*J1219 45	24B	FO1200	J1221 26	14A	FO1200
	J1312 24		FO1500						
AT2XB0V	J1216 37	18B	FO1401	*J1218 49	23A	FO 1200			
AWFNIA	J1214 75	37B	FO1402	*J1221 05	03B	FO1402	*J1224 19	09B	FO1402
AXBSTA	J1214 68	32A	FO0901	J1215 17	09B	FOI100	J1219 13	06B	FO1100
	J1312 41		FO1500	*J1318 76	37A	FOI I0	J1325 68		FO0701
AXBST0V	*J1215 14	08B	FOI100	J1216 31	15B	FO 1401			
AXBWT0	J1214 69	35A	FO1402	J1312 13		FO1402			
AXCBAA	*J1213 11	05B	FO1100	J121940	19A	FOI100			
AXCBA0	*J1219 38	18A	FO1100	J1312 23		FO0601			
AXDFS0V	*J1215 34	15A	FO1401	J1216 35	17B	FO1401			
AXDIS0V	J1214 37	18B	FO1402	J1216 08	06A	FO1402	*J1218 25	11A	FO1402
AXFHB0	J1214 03	02A	FO1000	*J1220 33	16B	FO1401	J1221 37	18B	FO0401
	J1224 17	08B	FO1402						
AXFHRA	*J1213 23	11B	FO0902	J1214 24	13A	FO1000	J1220 31	15B	FO1401
AXFLB0	J1214 57	30B	FO0500	J1217 21	01B	FO1402	*J1219 30	15A	FO1402
AXFLRA	*J1213 35	17B	FO0902	J1219 34	16A	FO1402			
AXFTA0	*J1217 20	11A	FO1401	J1219 37	18B	FO1402			
AXFTH0	J1206 66	31A	FO1000	J1217 14	09A	FOI000	*J1220 22	12A	FO1401
AXFTI0	J1216 07	03A	FO1402	*J1220 30	15A	FO1402			
AXFT00	J1216 24	13A	FO1401	*J1220 27	13B	FO1401			

Table 5-6. Left Hand Assembly Key Signal L00kup
-Continued

Signal	Distribution								
AXMPY0V	J1207 57	29B	FO1200	J1208 49	24B	FO0601	J1208 66	32B	FO0601
	J1216 13	06B	FO0603	J121738	18A	FO1402	*J1218 18	09A	FO1402
	J1220 20	11A	FO1200						
AXRSW0V	*J1212 72	34A	FO1401	J1220 65	34B	FO1401			
AXSHFOV	J1207 49	24B	FO1401	J1214 38	18A	FO0601	*J1215 03	03A	FO1401
	J1217 03	02A	FO0601	J1217 06	05A	FO0603	J1217 45	24B	FO0603
	J1217 52	24A	FO0601	J1219 49	26B	FO1200			
AXSSW0V	*J1212 26	12B	FO1401	J1220 35	17B	FO1401			
AXTCC0	J1219 68	32A	FO1200	*J1221 69	35A	FO1402			
AXTCITA	*J1207 55	27B	FO1200	J1226 45	23B	FO1200			
AXTCITB	*J1207 61	31B	FO1200	J1226 43	22B	FO1200			
AXTCITC	*J1207 60	28A	FO1200	J1226 41	19B	FO1200			
AXTCITD	*J1207 63	31A	FO1200	J1226 39	18B	FO1200			
AXTCLA	*J1219 66	31A	FO1200	J1226 50	24A	FO1200			
AXTCT1U	*J1226 38	18A	FO1200	J1332 14	06A	FO1200	J1332 27	14A	FO1200
AXTCT2U	*J1226 40	19A	FO1200	J1332 10	05A	FO1200	J1332 26	13A	FO1200
AXTCT3U	*J1226 42	20A	FO1200	J133208	04A	FO1200	J1332 24	12A	FO1200
AXTCT5U	J1218 64	33A	FO1200	J1220 42	20A	FO1200	J1224 23	11 B	FO1200
	*J1226 36	17A	FO1200						
AXTFFJ	J1219 43	23B	FO1200	*J1234 31	15B	FO1200			
AXTFFK	J1217 11	05B	FO1200	J1219 10	07A	FO1200	J 121956	26A	FO1200
	*J1234 33	16B	FO1200						
AXTFJ0	*J1219 33	16B	FO1200	J1234 34	16A	FO1200			
AXTJ1A	J1216 55	29B	FO1402	J1213 74	35B	FO1402	J121740	19A	FO1402
	J1219 29	14B	FO1200	*J1221 47	25B	FO1402			
AXTJ2A	*J1217 15	07B	FO1200	J121903	02A	FO1200	J121931	15B	FO1200
AXT0VAV	*J1218 66	32A	FO1200	J1220 18	I0A	FO1200	J1224 30	15A	FO1200
	J1224 35	17B	FO1200	J1226 47	23A	FO1200			
AXTSS0V	J1214 34	16A	FO1401	*J1218 24	13A	FO1401			
AX1BI0	J1214 25	12B	FO1402	*.11219 15	07B	FO1000	J1325 35		FO0701
AX1CGA	J1219 23	11B	FO1402	*J1221 33	16B	FO1401			
AX1CM0	*J1219 27	13B	FO1402	J1221 49	26B	FO1402			
AX1FIA	*J1214 27	13B	FO1402	J1317 73	36B	FO1402			
AX1NC0	J1221 52	24A	FO1402	*J1317 76	37A	FO1402			
AX2NC0	J1217 13	06B	FO1200	*J1221 45	24B	FO1402			
AZRQ40E	J1206 18	I0A	FO1100	*J1223 35	17B	FO1100			

Table 5-6. Left Hand Assembly Key Signal L00kup
-Continued

Signal	Distribution								
AZRQ41E	J1206 14	09A	FO1100	*J1223 39	19B	FO1100			
AZRQ42E	J1206 20	11A	FO1100	*J1223 42	20A	FO1100			
A10MA04	*J1106 69	35A	FO5402	J1115 06	05A	FO4900	J1116 06	05A	FO4700
	J1209 48	22A	FO5100	J1219 65	34B	FO5402	J1219 76	37A	FO5402
	J1222 38		FO5402	J1222 39		FO5402	J1229 06	03A	FO0102
A10MB04	*J1106 76	37A	FO5402	J1225 63	32B	FO0401	J1229 72	35A	FO0401
	J1233 75	37B	FO0402	J1234 75	37B	FO0402	J1308 65		FO5402
	J1308 66		FO5402	J1325 36		FO0401			
A10MC04	*J1106 59	31B	FO5402	J1229 20	10A	FO0401	J1229 34	16A	FO0401
	J1233 52	24A	FO0401	J1234 22	12A	FO5100	J1308 76		FO5402
	J1308 78		FO5402						
A10MZA	J1106 70	33A	FO5402	J1106 74	35B	FO5402	J1106 79	39B	FO5402
	*J1110 21	10B	FO5402	J1119 68	32A	FO5402			
A10MZ04	*J1106 11	05B	FO5402	J1110 17	08B	FO5402	J1110 64	30A	FO5402
	J1110 70	33A	FO5402	J1122 61	32B	FO5402	J1219 71	36A	FO5402
	J1222 42		FO5402	J1222 45		FO5402	J1233 66	31A	FO0401
A10NBA	J1126 69	32A	FO5100	*J1219 80	39A	FO5402	J1226 51	25B	FO0300
	J1230 69	32A	FO0300	J1231 69	32A	FO0200	J1232 37	17B	FO0200
	J1232 51	25B	FO0200						
A10NCA	*J1219 69	35A	FO5402	J1230 37	17B	FO0200	J1230 51	25B	FO0200
	J1231 37	17B	FO0200	J1231 51	25B	FO0200	J1232 69	32A	FO0200
A5MSQJ	J1110 62	29A	FO5402	J1110 68	32A	FO5402	*J1233 61	32B	FO5402
	J1338 59	31B	FO5402						
A5MSQK	J113243	23B	FO5100	*J1233 59	31B	FO5402	J134041	22B	FO5402
A5MZAA	*J1110 66	31A	FO5402	J1227 37	17B	FO5201	J1313 05		FO0603
	J1314 05		FO0602	J1315 05		FO0602	J1316 05		FO0601
	J1334 36		FO1300						
A5MZA04	*J1106 21	10B	FO5402	J1115 22	12A	FO5002	J1116 22	12A	FO5002
	J1119 24	13A	FO5100	J1128 09	06B	FO4801	J1129 09	06B	FO4801
	J1222 46		FO5402	J1222 47		FO5402	J1225 09	06B	FO0902
	J1233 06	05A	FO0500	J1234 06	05A	FO5300			
ASMZBA	J1106 20	11A	FO5402	J1106 26	14A	FO5402	J1106 30	15A	FO5402
	J1106 38	18A	FO5402	J1106 55	29B	FO5402	*J1110 60	28A	FO5402
A5MZB04	*J1106 23	11B	FO5402	J1115 38	18A	FO5002	J1116 38	18A	FO5300
	J1119 34	16A	FO5402	J1128 23	12B	FO4801	J1129 23	12B	FO4801
	J1209 72	35A	FO4402	J1222 48		FO5402	J1222 52		FO5402

Table 5-6. Left Hand Assembly Key Signal L00kup
-Continued

Signal				Distribution						
	J1223	37	18B	FOII00	J1225	23	12B	FO0902	J1233 22	12A	FO5201
A5MZC04	*J1106	33	16B	FO5402	J1115	52	24A	FO5002	J1116 52	24A	FO5300
	J1128	37	18B	FO4801	J1129	37	18B	FO4801	J120906	03A	FO4900
	J1222	62		FO5402	J1222	66		FO5402	J1225 37	18B	FO0902
	J1233	38	18A	FOI000	J1234	38	18A	FO0401	J1234 38		FO1200
A5MZD04	*J1106	35	17B	FO5402	J1115	66	31A	FO5002	J1116 66	31A	FO5002
	J1128	49	26B	FO4801	J1129	49	26B	FO4801	J1129 63	32B	FO5001
	J1209	20	10A	FO4900	J1222	71		FO5402	J1222 72		FO5402
	J1225	49	26B	FO0902	J1229	48	22A	FO1100	J1234 52	24A	FO1200
A5MZE04	*J1106	57	30B	FO5402	J1115	75	37B	FO5201	J1116 75	37B	FO5201
	J1128	63	32B	FO5001	J1128	77	38B	FO5001	J1129 77	38B	FO5001
	J1209	34	16A	FO4900	J1222	73		FO5402	J1222 75		FO5402
	J1225	77	38B	FO0500	J1229	60	29A	FO1100	J1234 66	31A	FO0500
A5SQFAV	J1122	59	31B	FO5402	*J1218	78	36A	FO5402	J1219 73	36B	FO5402
	J1320	04		FO0702	J1321	04		FO0702	J1322 04		FO0702
	J1323	04		FO0702							
A5SQF0	J03	39		FO5402	J1218	76	37A	FO5402	*J1338 63	33B	FO5402
A5SQT0	J03	41		FO5402	J1221	42	20A	FO0401	*J1340 45	24B	FO5402
CCTBD0	J02	14		FO5204	J1105	73	37B	FO5204	J1126 66		FO5204
CDTBA0	J02	15		FO5203	J1105	79	39B	FO5204	J1123 42		FO5204
CLSC2A	J02	66		FO5402	J1I106	13	06B	FO5402	J1119 70	33A	FO5402
	J1211	19		FO5402							
CLTBX0	J02	12		FO5204	J1105	75	39A	FO5204	J1114 71		FO5204
CLTBY0	J02	13		FO5204	J121241		23B	FO5204	J1115 71		FO5204
DDIPSA	*J06	14		FO5300	J111639		19B	FO5300	J1116 41	22B	FO5300
	J1131	01	02B	FO4801	J1131	06	05A	FO4801	J1131 09	04B	FO4801
	J1131	29	14B	FO4801	J1131	33	16B	FO4801	J1131 38	18A	FO4801
	J1131	41	22B	FO4801	J1131	45	24B	FO4801	J1131 52	24A	FO4801
	J1132	03	02A	FO4801	J113223		11B	FO4801			
DDSNCT	*J02	49		FO0102	J1341	62	29A	FO0102			
DD0PCT	*J02	26		FO0102	J1342	51	25B	FO0102			
DD00CT	*J02	28		FO0102	J1342	57	29B	FO0102			
DD01CT	*J02	30		FO0102	J1342	54	26A	FO0102			
DD02CT	*J02	31		FO0102	J1342	62	29A	FO0102			
DD03CT	*J02	33		FO0102	J1342	69	32A	FO0102			
DD04CT	*J02	35		FO0102	J1342	75	35B	FO0102			

Table 5-6. Left Hand Assembly Key Signal L00kup
-Continued

Signal				Distribution						
DD05CT	*J02	38		FO0102	J1342	70	34A	FO0102		
DD06CT	*J02	40		FO0102	J1342	76	37A	FO0102		
DD07CT	*J02	42		FO0102	J1341	57	29B	FO0102		
DMPECB1	J02	18		FO5002	J1117	74	35A	FO5002	J1125 51	FO5002
DMPEDB1	J02	20		FO5002	J1117	75	39A	FO5002	J1125 53	FO5002
DMT0ABC1	J02	16		FO5002	J1117	76	37A	FO5002	J1125 62	FO5002
DRQIABC1	J02	58		FO5002	J1125	64		FO5002	J1134 39 19B	FO5002
D0RNCB1	J02	22		FO5002	J1125	55		FO5002	J1212 79 39B	FO5002
KDBAKA	J04	35		FO1000	J1211	10		FO1000	J1212 38 20A	FO1000
KDCTBA	J04	50		FO1902	J1109	77	38B	FO4900	J1308 37	FO1902
KLBZ52X	J04	30		FO5203	J1213	66	31A	FO5204		
KLBZ62X	J04	31		FO5203	J1213	68	32A	FO5204		
KLBZ72X	*J04	29		FO5203	J1213	70	33A	FO5204		
KRBSEA	J04	37		FO2602	J1133	62	29A	FO5201		
KSW06D4	J04	32		FO2500	J1222	53		FO2500	J1315 30	FO0801
KSW07D4	J04	33		FO2500	J1222	55		FO2500	J1315 13	FO0801
KSW08D4	J04	34		FO2500	J1222	56		FO2500	J1314 57	FO0802
LADBRA	J1118	30	15A	FO5300	*J1119	57	30B	FO5300		
LADB0AV	J1107	62	29A	FO4900	*J1108	13	06A	FO4900	J1111 49 26B	FO4900
LADB3AV	J1117	52	26A	FO4801	*J1120	77	38A	FO4801		
LADB30V	*J1117	54	25A	FO4801	J1128	45	24B	FO4801		
LADG0R	J1107	10	07A	FO4900	J1107	38	18A	FO4900	J1107 52 24A	FO4900
	*J1109	01	02B	FO4900						
LADG0S	*J1107	04	04A	FO4900	J1109	05	03B	FO4900		
LADMGA	J1107	08	06A	FO4900	*J1109	06	05A	FO4900		
LADRS0	J1116	34	16A	FO5300	*J1118	31	15B	FO5300	J1210 77 38B	FO5300
	J1218	38	20A	FO5300	J1311	03	02A	FO0102	J1334 18	FO1300
LADRXK	*J1116	33	16B	FO5300	J1118	34	16A	FO5300	J1209 17 09B	FO4900
	J1209	31	15B	FO4900						
LAD0B0E	J05	21		FO4801	J1108	11	07A	FO4900	J1124 51 25B	FO4801
	J1127	68	32A	FO5002	*J1128	35	17B	FO4801		
LAD0B1E	J05	22		FO4801	J1124	57	29B	FO4801	J1127 47 25B	FO5002
	*J1128	39	19B	FO4801	J1328	77	36B	FO0902		
LAD0B2E	J05	23		FO4801	J1124	54	26A	FO4801	J1127 41 22B	FO5002
	*J1128	42	20A	FO4801	J1328	72	35A	FO0902		
LAD0B3E	J05	24		FO4801	J1120	75	39A	FO4801	J1124 62 29A	FO4801

Table 5-6. Left Hand Assembly Key Signal L00kup
-Continued

Signal	Distribution								
	J1127 48	22A	FO5002	*J1128 38	18A	FO4801	J1328 78	38A	FO0902
LAI00D	*J1127 01	02B	FO5002						
LAI01D	*J1127 09	04B	FO5002						
LAI02D	*J1127 15	07B	FO5002						
LAI03D	*J1127 22	12A	FO5002						
LAI04D	*J1127 14	09A	FO5002						
LAI05D	*J1127 21	10B	FO5002						
LAI06D	*J1127 27	13B	FO5002						
LAI07D	*J1127 38	18A	FO5002						
LAI08D	*J1127 30	15A	FO5002						
LAI09D	*J1127 33	16B	FO5002						
LAI10D	*J1127 39	19B	FO5002						
LAI11D	*J1127 52	24A	FO5002						
LAI12D	*J1127 46	21A	FO5002						
LAI13D	*J1127 45	24B	FO5002						
LAI14D	*J1127 51	27B	FO5002						
LAI15D	*J1127 66	31A	FO5002						
LAPACA	J1117 21	11B	FO0500	*J1119 15	07B	FO0500			
LAPAC0V	*J1117 19	10B	FO0500	J1118 21	10B	FO5002	J1119 59	31B	FO0500
LAPG00	*J1107 36	17A	FO4900	J1214 30	15A	FO1401	J1214 33	16B	FO1402
	J1217 18	10A	FOI000	J1221 04	04A	FO1401	J1224 18	10A	FO1401
LAPIEA	*J1110 57	30B	FO5001	J1112 62	29A	FO5001			
LAPIED4	*J1112 60	28A	FO5002	J1127 05	03B	FO5001	J1127 07	03A	FO5001
	J1127 13	06B	FO5001	J1127 19	09B	FO5001	J1127 20	11A	FO5001
	J1127 25	12B	FO5001	J1127 26	14A	FO5001	J1127 31	15B	FO5001
	J1127 36	17A	FO5001	J1127 37	18B	FO5001	J1127 42	20A	FO5001
	J1127 43	23B	FO5001	J1127 49	26B	FO5001	J1127 50	23A	FO5001
	J1127 56	26A	FO5001	J1127 70	33A	FO5001	J1211 07		FO5002
LAPIFJ	J1110 55	29B	FO5002	J1112 68	32A	FO5002	*J1116 61	32B	FO5002
LAPIFK	*J1116 59	31B	FO5002	J111974	35B	FO5002			
LAPIID	*J1112 66	31A	FO5002						
LAPIJA	J1117 64	33A	FO5002	*J1119 63	33B	FO5002			
LAPIJ0V	J1116 68	32A	FO5002	*J1117 66	32A	FO5002			
LAPRQAV	*J1120 53	26B	FO5002	J1332 35	16B	FO0500	J1341 78	38A	FO0500
LAPRQ0	*J1119 69	35A	FO5002	J1120 51	27B	FO5002			
LAPTBA	J1109 76	37A	FO4900	*J1110 80	39A	FO0902			

Table 5-6. Left Hand Assembly Key Signal L00kup
-Continued

Signal	Distribution									
LAPTB0	*J1109	80	39A	FO4900	J1209	36	17A	FO4900			
LAPTRKQ	J1107	42	20A	FO4900	*J1209	39	19B	FO4900			
LAPXCA	J1108	47	24A	FO4900	*J1111	51	27B	FO4900			
LAPXC0V	*J1108	49	23A	FO4900	J1328	49	24B	FO0902	J1328	66	32B	FO0902
	J1331	49	24B	FO0902	J1331	66	32B	FO0902				
LAP0FJ	*J1116	19	09B	FO5002	J1206	10	07A	FO5002				
LAP0FK	*J1116	21	10B	FO5002	J1119	65	34B	FO5002				
LAP0JA	J1117	20	10A	FO5002	*J1118	27	13B	FO5002				
LAP0J0V	J1116	18	10A	FO5002	*J1117	18	09A	FO5002				
LAP1T0	*J1107	51	27B	FO4900	J1109	48	22A	FO4900	J1111	45	24B	FO4900
LAP1XA	J1107	40	19A	FO4900	*J1109	46	21A	FO4900				
LBD0B0E	J05	25		FO4801	J1124	69	32A	FO4801	J1127	54	25A	FO5002
	*J1128	47	25B	FO4801	J1328	53	26B	FO0902				
LBD0B1E	J05	26		FO4801	J1124	75	35B	FO4801	J1127	35	17B	FO5002
	*J1128	51	27B	FO4801	J1328	59	30B	FO0902				
LBD0B2E	J05	27		FO4801	J1124	70	34A	FO4801	J1127	29	14B	FO5002
	*J1128	56	26A	FO4801	J1328	56	28B	FO0902				
LBD0B3E	J05	28		FO4801	J1124	76	37A	FO4801	J1127	34	16A	FO5002
	*J1128	52	24A	FO4801	J1328	64	30A	FO0902				
LBITGA	*J1118	55	29B	FO4900	J1120	47	24A	FO4900				
LBITG0V	J1109	11	05B	FO4900	J1109	34	16A	FO4900	J1112	47	25B	FO4900
	J1119	55	29B	FO5300	*J1120	49	23A	FO4900	J1122	71	36A	FO5201
	J1132	13	06B	FO4900	J1209	07	05B	FO4900				
LBM042X	J1123	39	18B	FO5201	*J1341	06	03A	FO5202				
LBM052X	J112341		19B	FO5202	*J1331	06	03A	FO5202				
LBM061X	J1123	19	09B	FO5202	*J1331	20	10A	FO5202				
LBM071X	J1123	21	10B	FO5202	*J1331	36	17A	FO5202				
LBM081X	J1123	23	11B	FO5202	*J1208	36	17A	FO5202				
LBM091X	J1123	25	12B	FO5202	*J1207	36	17A	FO5202				
LBM101X	J1123	29	13B	FO5202	J1328	20		FO5202	*J1328	20	10A	FO5201
LBM111X	J1123	31	14B	FO5202	J1328	36		FO5202	*J1328	36	17A	FO5201
LBM121X	J1123	34	15B	FO5202	J1328	04		FO5202	*J1328	04	02A	FO5201
LBM131X	J1123	33	16A	FO5202	J1327	36		FO5202	*J1327	36	17A	FO5201
LBM141X	J1123	35	16B	FO5202	J1341	20		FO5202	*J1341	20	10A	FO5201
LBM151X	J1123	37	17B	FO5202	J1327	04		FO5202	*J1327	04	02A	FO5201
LBM161X	J1123	07	04B	FO5202	J1327	20		FO5202	*J1327	20	10A	FO5201

Table 5-6. Left Hand Assembly Key Signal L00kup
-Continued

Signal				Distribution					
LBSDLA	J1132 40	19A	FO5201	*J1133 72	34A	FO5201			
LBSDL0	1130 68	32A	FO5201	*J1132 38	18A	FO5201			
LBSRDJ	J1109 37	18B	FO5100	*J1115 78	38A	FO5201	J1118 54	25A	FO5002
LBSRDK	J1107 53	28B	FO4900	J1109 26	14A	FO4900	J1111 47	25B	FO4900
	J1112 41	22B	FO4900	*J1115 76	37A	FO5201	J1119 50	23A	FO5100
	J1130 75	37B	FO5201	J1133 73	36B	FO5201	J1205 49	24B	FO4900
LBSRJA	J1117 47	24A	FO5201	*J1122 75	37B	FO5201			
LBSRJ0	J1115 77	38B	FO5201	J1116 79	39B	FO5201	*J111749	23A	FO5201
LBSRKA	J1117 50	22A	FO5201	*J1122 72	34A	FO5201			
LBSRK0	J1115 79	39B	FO5201	*J1117 48	21A	FO5201			
LBSSFJ	*J1116 78	38A	FO5201	J1122 53	28B	FO5201			
LBSSHA	J1117 04	02A	FO5201	*J112257	30B	FO5201	J113070	33A	FO5201
	J1205 05	03B	FO5201						
LBSSH0	*J1117 03	03A	FO5201	J1122 77	38B	FO5201	J1133 47	25B	FO5201
	J1135 65	34B	FO5201	J1227 48	22A	FO5201			
LBSSJA	J111971	36A	FO5201	*J113059	31B	FO5201	J1227 50	24A	FO5201
LBSSJ0	J1116 77	38B	FO5201	*J111972	34A	FO5201			
LBSSLA	J1132 65	34B	FO4801	*J1135 69	35A	FO5201			
LBSSMA	J1132 68	32A	FO4801	*J1133 51	27B	FO5201	J1135 74	35B	FO5201
LBTXEJQ	J1109 08	06A	FO4900	J1109 50	23A	FO4900	J1109 54	25A	FO4900
	J1110 07	03A	FO4900	*J1209 13	07A	FO4900	J1233 26	14A	FO5201
LBTXEKQ	J1133 71	36A	FO5201	*J1209 11	07B	FO4900			
LBYAIA	*J1111 20	11A	FO5100	J1120 52	26A	FO5100	J1122 40	19A	FO5100
LBYAI0V	J1119 54	25A	FO5100	*J1120 54	25A	FO5100			
LBYAJ0	J1115 40	19A	FO5100	*J1122 38	18A	FO5100			
LBYAVJ	*J1115 37	18B	FO5100	J11 19 20	11A	FO5100			
LBYAVK0	*J1115 35	17B	FO5100	J1118 46	21A	FO5100			
LBYCK0	*J1118 43	23B	FO5100	J1223 09 -	06B	FO5100	J1223 23	12B	FO5100
LBYCTA	J1109 25	12B	FO5100	*J1132 63	33B	FO5100	J1223 08	04A	FO5100
	J1223 22	11A	FO5100						
LBYCT0	J1115 60	28A	FO5100	J1119 26	14A	FO5100	*J1130 33	16B	FO5100
	J1132 59	31B	FO5100	J1223 14	06A	FO5100	J1223 26	13A	FO5100
LBYC10E	J1116 01	02B	FO4700	J1122 36	17A	FO5100	J1131 22	12A	FO5100
	*J1223 07	05B	FO5100	J1234 26	14A	FO5100			
LBYC11E	J1120 79	39B	FO5100	J1132 56	26A	FO5100	*J1223 11	07B	FO5100
LBYC12E	J1119 19	09B	FO5100	*J1223 13	07A	FO5100			

Table 5-6. Left Hand Assembly Key Signal L00kup
-Continued

Signal	Distribution								
LBYC13E	J1115 01	02B	FO4900	J1118 37	18B	FO5100	J1119 25	12B	FO5002
	J1120 74	35A	FO5100	*J1223 10	05A	FO5100			
LBYC20E	J1117 11	07A	FO5100	*J1223 21	11IB	FO5100			
LBYC21E	J1122 49	26B	FO5000	*J1223 27	13B	FO5100			
LBYC22E	J1111 79	39B	FO5100	J1117 27	13B	FO5100	*J1223 25	14A	FO5100
LBYDLA	*J1131 55	29B	FO5100	J1224 38	18A	FO5100			
LBYDMA	*J1131 64	30A	FO5100	J1224 40	19A	FO5100			
LBYDPA	*J1131 63	33B	FO5100	J1224 42	20A	FO5100			
LBYDT0	J1209 49	26B	FO5100	*J1224 36	17A	FO5100			
LBYKCA	J1118 41	22B	FO5100	*J1131 20	11A	FO5100			
LBYKTA	J1118 48	22A	FO5100	*J1119 22	12A	FO5100			
LBYLCA	*J1122 06	05A	FO5100	J1131 61	32B	FO5100	J1131 62	29A	FO5100
	J1131 70	33A	FO5100	J1132 53	28B	FO4801			
LBYMIA	*J1119 52	24A	FO5100	J1122 23	11B	FO5100			
LBYMV0	*J1122 27	13B	FO5100	J1128 14	06A	FO4801	J1128 26	13A	FO4801
	J1128 40	19A	FO4801	J1128 54	25A	FO4801	J1129 14	06A	FO4801
	J1129 26	13A	FO4801	J1129 40	19A	FO4801	J1129 54	25A	FO4801
LBYM0A	*J1119 14	09A	FO5100	J1122 25	12B	FO5100			
LBYNTAV	*J1120 63	30A	FO5100	J1130 36	17A	FO5100			
LBYNT0	*J1111 73	36B	FO5100	J1120 61	31A	FO5100			
LBYPEJ	J1110 05	03B	FO5100	*J1116 07	03A	FO4700			
LBYPJA	*J1118 51	27B	FO4700	J1119 40	19A	FO4700			
LBYPJ0	J1116 05	03B	FO4700	*J1119 38	18A	FO4700			
LBYPTA	*J1110 01	02B	FO5100	J113030	15A	FO5100			
LBYT1JQ	J1111 22	12A	FO5100	J1111 30	15A	FO5002	J1111 62	29A	FO5100
	J1115 08	06A	FO5100	J1130 37	18B	FO5100	*J1209 56	26A	FO5100
LBYT2KQ	J1115 10	07A	FO5100	J1122 08	06A	FO5100	*J1209 51	27B	FO5100
LBYT2J	*J1115 13	06B	FO5100	J1122 10	07A	FO5100	J1130 38	18A	FO5100
	J1209 50	23A	FO5100						
LBYXEA	*J1130 35	17B	FO5100	J1132 48	22A	FO5100			
LBYXE0	J1118 17	08B	FO4900	J1118 47	25B	FO4700	J113024	13A	FO5100
	J1131 69	35A	FO5100	*J1132 46	21A	FO5100			
LBY0CA	J1110 04	04A	FO5100	J1111 24	13A	FO5100	J1118 49	26B	FO4700
	*J1122 30	15A	FO5100	J1126 66	32B	FO5100	J1130 40	19A	FO5100
LBY030	*J1130 11	05B	FO5100	J1131 66	31A	FO5100			
LBY1CAV	J1119 56	26A	FO5100	*J1120 80	38B	FO5100			

Table 5-6. Left Hand Assembly Key Signal L00kup
-Continued

Signal			Distribution						
LBY2L0	J1119 17	08B	FO5100	*J1122 45	24B	FO5100			
LBY2TA	*J1119 21	10B	FO5100	J1130 31	15B	FO5100			
LBY3CAV	*J1120 72	34A	FO5100	J1223 19	01B	FO5100			
LBY4C0V	*J1117 13	06A	FO5100	J1118 14	09A	FO4900			
LBY470	*J1130 09	04B	FO5100	J1131 53	28B	FO5100			
LBY6C0V	*J1117 26	12B	FO5100	J1118 62	29A	FO4900	J1132 18	10A	FO5002
LCB0IA	J1111 75	37B	FO5100	*J1132 09	04B	FO4801	J1137 08	08B	FO4801
LCB0PA	*J1131 51	27B	FO4801	J1142 01	02A	FO4801			
LCB0RA	*J1132 27	13B	FO4801	J1136 01	02A	FO4802			
LCB00A	*J1131 04	04A	FO4801	J1142 08	08B	FO4801			
LCB01A	*J1131 07	03A	FO4801	J1141 01	02A	FO4801			
LCB02A	*J1131 15	07B	FO4801	J1141 08	08B	FO4801			
LCB03A	**J1131 36	17A	FO4801	J1140 01	02A	FO4801			
LCB04A	*J1131 31	15B	FO4801	J1140 08	08B	FO4801			
LCB05A	*J1131 39	19B	FO4801	J1139 01	02A	FO4801			
LCB06A	*J1131 50	23A	FO4801	J1139 08	08B	FO4801			
LCB07A	*J1131 43	23B	FO4801	J1138 01	02A	FO4801			
LCMINA	*J1111 31	15B	FO5002	J1117 73	37B	FO5002	J1130 56	26A	FO5002
LCMIN0V	J1115 70	33A	FO5002	*J111771	36B	FO5002			
LCMRC	J1111 34	16A	FO5002	*J1115 61	32B	FO5002			
LCMRQA	*J I1111 36	17A	FO5002	J1117 65	33B	FO5002	J1122 50	23A	FO5002
LCMRQ0V	J1115 68	32A	FO5002	*J1 117 68	32B	FO5002			
LCPAD0	*SIC	C	FO4802	J1131 24	13A	FO5100	J1135 77	38B	FO5002
LCPIN0	*J1130 47	25B	FO5002	J1132 07	03A	FO4801			
LCPRFJ	*J1115 19	09B	FO5002	J1132 25	12B	FO4801			
LCPRQ0	J1115 18	10A	FO5002	*J1122 46	21A	FO5002			
LCRSJ0	J1116 48	22A	FO5300	*J1206 09	04B	FO5300			
LCRSTJ	*J1116 43	23B	FO5300	J1127 53	28B	FO5300	J1127 59	31B	FO5300
	J1127 62	29A	FO5300	J1127 71	36A	FO5300	J1127 77	38B	FO5300
	J1234 08	06A	FO5300						
LCRSTK	*J1116 45	24B	FO5300	J1118 29	14B	FO5300	J1118 42	20A	FO5002
	J1119 37	18B	FO4900	J1130 34	16A	FO5100	J1132 55	29B	FO4801
LCRSXJ	J111646	21A	FO5300	*J1234 13	06B	FO5300			
LCTMD0V	J1111 40	19A	FO5002	*J1117 70	34B	FO5002			
LCTRKA	*J1119 30	15A	FO5402	J1126 51	25B	FO5002	J1204 69	32A	FO4103
	J1205 37	17B	FO5100	J1205 51	25B	FO5002	J1228 51	25B	FO5002

Table 5-6. Left Hand Assembly Key Signal Lookup-Continued

Signal	Distribution									
LC0FFA	*SIG	C	FO4802	J1125 30		FO4900	J1224 05	03B	FO4900
LDATA3E	J1117 38	20A	FO5002	*J1128 76	37A	FO5002			
LDAT30V	*J1117 40	19A	FO5002	J1119 47	25B	FO5002			
LDBISA	J05 58		FO4900	*J1109 22	12A	FO4900			
LDBLPAV	J05 57		FO4900	*J1108 46	22B	FO4900			
LDBLPR	*J1107 20	11A	FO4900	J1109 19	09B	FO4900			
LDBLPS	J1107 22	12A	FO4900	J1108 41	23B	FO4900	*J1109 21	10B	FO4900
LDBTDA	*J1109 15	07B	FO4900	J1135 78	38A	FO1000			
LDCG00	J04 51		FO4900	*J1107 50	23A	FO4900			
LDCTB0	*J1109 75	37B	FO4900	J1209 26	13A	FO4900			
LDCTRKQ	J1107 54	25A	FO4900	*J1209 27	13B	FO4900			
LDCXCA	*J1107 55	29B	FO4900	J1108 50	22A	FO4900			
LDCXC0V	J05 37		FO4900	*J1108 48	21A	FO4900			
LDCOBA	*TB06	B06	FO5002	SI 4		FO5300			
LDCOBAV	*J1120 48	21A	FO4700	J1124 48	22A	FO4700	J1129 59	30B	FO5001
	J1223 01	02B	FO5100	J1227 39	18B	FO5201	J1120 48	21A	FO5001
LDC0CAV	J02 61		FO5002	J1123 52	25A	FO4700	J1123 68	33A	FO4700
	J1124 77	36B	FO4801	J1126 05	03B	FO4900	*J1134 72	34A	FO4700
	J1223 04	02A	FO5100	J1227 41	19B	FO5201	J1134 72	34A	FO5002
LDC0DAV	J1124 72	35A	FO4801	*J1134 78	36A	FO4103	J1204 79	37B	FO4103
	J1223 06	03A	FO5100	J1227 43	22B	FO5201			
LDC0EAV	J1124 13	07A	FO5201	J1124 30	15A	FO5201	J1124 78	38A	FO4801
	*J1134 77	38A	FO5201	J1223 05	04B	FO5100	J1227 45	23B	FO5201
LDC0FAV	J1124 37	17B	FO4700	J1126 79	37B	FO5100	*J1134 13	06A	FO0902
	J1328 71	33B	FO0902	J1342 03	02B	FO4700	J1342 19	09B	FO4700
	J1342 35	16B	FO4700						
LDC0GAV	J1124 39	18B	FO4700	J1126 19	09B	FO5002	J1126 61	31B	FO5002
	*J1134 24	13A	FO4700	J1342 09	05B	FO4700	J1342 25	12B	FO4700
	J1342 41	19B	FO4700						
LDC0HAV	J1124 43	22B	FO4700	J1124 52	25A	FO4801	*J1134 30	14B	FO4700
	J1342 15	07B	FO4700	J1342 31	14B	FO4700	J1342 45	23B	FO4700
LDC0JAV	J1124 50	24A	FO4700	J1124 68	33A	FO4801	*J1134 56	28B	FO4700
	J1205 41	19B	FO5100	J1205 61	31B	FO4900	J1342 18	09A	FO4700
	J1342 34	15B	FO4700	J1342 47	23A	FO4700			
LDCIXA	J1107 56	26A	FO4900	*J1109 52	24A	FO4900			
LDDME0	J1133 68	32A	FO5100	*J1135 52	24A	FO4900			

Table 5-6. Left Hand Assembly Key Signal Lookup-Continued

Signal	Distribution									
LDINBD	*J1112	69	35A	FO5002						
LDINCD	*J1112	80	39A	FO5002						
LDINHB	J02	56		FO5002	*J1112 69	35A	FO5002	*J1112 80	39A	FO5002
LDRQIAV	*J1134	03	03A	FO5002	J1315 57		FO0801			
LDRQI0	J1112	65	34B	FO5002	J1112 76	37A	FO5002	*J1119 33	16B	FO5002
	J1126	53	26B	FO5002	.11134 04	02A	FO5002			
LDRSDA	*J1118	36	17A	FO5002	.11122 65	34B	FO5002			
LDRSTAV	J02	51		FO5002	*J1120 56	28B	FO5002			
LDRST0	J1120	55	29B	FO5002	*J1122 69	35A	FO5002			
LDSC10	J1124	14	06A	FO5201	J1124 27	14A	FO5201	*J1133 21	01B	FO5201
	J1207	46	21A	FO5202	J1208 46	21A	FO5202	J1328 27	14A	FO5202
	J1331	14	06A	FO5202	J1331 27	14A	FO5201	J1331 46	21A	FO5202
	J1341	14	06A	FO5202						
LDSC20	J124	10	05A	FO5201	J1124 26	13A	FO5201	*J1133 27	13B	FO5201
	J1207	42	20A	FO5202	J1208 42	20A	FO5202	J1328 26	13A	FO5202
	J1331	10	05A	FO5202	J1331 26	13A	FO5201	J1331 42	20A	FO5202
	J1341	10	05A	FO5202						
LDSC40	J1124	08	04A	FO5201	J1124 24	12A	FO5201	*J1132 21	01B	FO5201
	J1207	40	19A	FO5202	J1208 40	19A	FO5202	J1328 24	12A	FO5202
	J1331	08	04A	FO5202	J1331 24	12A	FO5201	J1331 40	19A	FO5202
	J1341	08	04A	FO5202						
LDUFR1U	J1124	59	30B	FO4801	*J1126 54	26A	FO5002			
LDUFR2U	J1124	56	28B	FO4801	*J1126 56	28B	FO5002			
LDUFR3U	J1124	64	30A	FO4801	*J1126 60	28A	FO5002			
LDUFR4U	J1124	71	33B	FO4801	*J1126 62	29A	FO5000			
LDUSMA	*J1132	15	07B	FO4900	J1135 56	26A	FO4900			
LDVINA	*J1119	27	13B	FO5002	J1120 29	15B	FO5002	J1130 52	24A	FO5002
LDVIN0V	J1118	01	02B	FO5002	*J112030	14B	FO5002	J1122 11	05B	FO5002
	J1122	17	08B	FO4900						
LDVMAA	J1109	04	04A	FO4900	*J1122 21	01B	FO4900	J1224 01	02B	FO4900
LDVSPA	J1117	62	29A	FO5002	*J1122 15	07B	FO5002	J120605	03B	FO5300
LDVSP0V	J1116	42	20A	FO5300	*J1117 60	28A	FO5002	J118 40	19A	FO5002
LDVSTA	J02	53		FO5002	*J1118 07	03A	FO5002			
LD0RN0V	*J1212	80	38B	FO5002	J1314 43		FO0802			
LENADA	J1134	36	16A	FO5002	*J1135 75	37B	FO5002			
LENAD0V	J1111	29	14B	FO5002	J1111 60	28A	FO5100	*J1134 34	15A	FO5002

Table 5-6. Left Hand Assembly Key Signal Lookup-Continued

Signal	Distribution									
LENCB0T	*J1205	08	04A	FO5201	J1230	05	03B	FO5203			
LENCB1T	J1123	13	07A	FO5202	J1123	30		FO5202	*J1205 10	05A	FO5201
	J1313	61		FO0603	J1314	61		FO0603	J1315 61		FO0602
	J1316	61		FO0602							
LENCB2T	J1123	30	15A	FO5201	*J1205	14	06A	FO5201			
LENCB3T	J1123	48	22A	FO5201	*J1205	13	07A	FO5201			
LENCB5T	J03	46		FO5202	J1314	30		FO5203	*J1205 07	04B	FO5201
LENCB6T	J03	47		FO5202	J1314	48		FO5203	*J1205 09	05B	FO5201
LENCB7T	J03	45		FO5202	J1314	13		FO5203	*J1205 11	06B	FO5201
LENSY0	J1131	59	31B	FO5100	J1131	60	28A	FO5100	J1131 68	32A	FO5100
	*J1132	45	24B	FO5100							
LESC10	J02	01		FO5203	*J1132	30	15A	FO5201	J1312 73		FO0603
	J1313	59		FO0603	J1314	59		FO0603	J1315 59		FO0602
	J1316	59		FO0601	J1325	65		FO0701	J1327 14	06A	FO5202
	J1327	27	14A	FO5202	J1327	46	21A	FO5201	J1328 14	06A	FO5202
	J1328	46	21A	FO5202	J1341	27	14A	FO5202			
LESC20	J02	02		FO5203	*J1132	33	16B	FO5201	J1312 74		FO0603
	J1313	62		FO0603	J1314	62		FO0602	J1315 62		FO0602
	J1316	62		FO0602	J1325	66		FO0701	J1327 10	05A	FO5202
	J1327	26	13A	FO5202	J1327	42	20A	FO5202	J1328 10	05A	FO5202
	J1328	42	20A	FO5202	J1341	26	13A	FO5202			
LESC40	J02	03		FO5203	*J1132	39	19B	FO5201	J1312 71		FO0603
	J1325	69		FO0701	J1327	08	04A	FO5202	J1327 24	12A	FO5201
	J1327	40	19A	FO5202	J1328	08	04A	FO5202	J1328 40	19A	FO5202
	J1341	24	12A	FO5202							
LFBAID	*J1127	06	05A	FO5002							
LFBBD0T	*J1126	24	12A	FO5002	J1132	74	35B	FO4801			
LFBBD1T	J1122	76	37A	FO5002	*J1126	26	13A	FO5002	J113270	33A	FO4801
LFBBD2T	J1120	15	07B	FO4801	*J1126	27	14A	FO5002			
LFBBD3T	J1120	11	07A	FO4801	*J1126	30	15A	FO5002			
LFBHFJ	*J1116	55	29B	FO5002	J1118	78	38A	FO5002	J1126 22	11A	FO5002
LFBHK0	J1116	60	28A	FO5002	*J1119	75	37B	FO5002			
LFBLBA	J1111	77	38B	FO5102	J1117	59	31B	FO5002	*J1118 39	19B	FO5102
LFBLB0V	J1115	56	26A	FO5002	*J1117	57	30B	FO5002			
LFBLDA	J1108	64	33A	FO5002	J1119	76	37A	FO5002	*J1206 11	05B	FO5002
LFBLD0V	*J1108	66	32A	FO5002	J1115	34	16A	FO5002	J1127 08	06A	FO5002

Table 5-6. Left Hand Assembly Key Signal Lookup-Continued

Signal	Distribution									
	J1128	66	32A	FO5002	J1128	78	38A	FO5002	J1129 66	32A	FO5002
	J1129	78	38A	FO5002							
LFBRCJ	*J1115	31	15B	FO5002	J1118	52	24A	FO5002	J1228 49	24B	FO5002
LFBRCK	*J1115	33	16B	FO5002	J1118	25	12B	FO5002	J1206 13	06B	FO5002
LFBRDJ	J1111	53	28B	FO5100	*J1115	49	26B	FO5002			
LFBRDK	*J1115	47	25B	FO5002	J1118	56	26A	FO5002			
LFBRER	J1119	78	38A	FO5002	*J1122	80	39A	FO5002			
LFBRES	J1118	69	35A	FO5002	*J1119	80	39A	FO5002	J1122 78	38A	FO5002
LFBRQA	J1117	79	39B	FO5002	*J1118	80	39A	FO5002	J1122 48	22A	FO5002
LFBRQ0V	J1115	54	25A	FO5002	*J1117	80	38B	FO5002			
LFBSC4U	J1126	20	10A	FO5002	*J1228	62	29A	FO5002			
LFBSC5U	J1115	30	15A	FO5002	J1116	62	29A	FO5002	J1118 76	37A	FO5002
	J1120	65	33B	FO5002	*J1228	52	25A	FO5002			
LFBSDA	*J1119	51	27B	FO5002	J1206	42	20A	FO5204			
LFBSHA	J1117	61	31A	FO5002	*J1118	50	23A	FO5002	J1126 21	01B	FO5002
LFBSH0V	*J1117	63	30A	FO5002	J1119	49	26B	FO5002	J1128 62	30A	FO5002
	J1128	74	36A	FO5002	J1129	62	30A	FO5002	J1129 74	36A	FO5002
	J1228	61	31B	FO5002							
LFBS5AV	J1119	79	39B	FO5002	*J1120	68	32B	FO5002			
LFSTVR	J1132	78	38A	FO4900	*J1133	75	37B	FO4900			
LFSTVS	J02	55		FO4900	*J1132	80	39A	FO4900	J1133 77	38B	FO4900
LHCR1A	J05	44		FO5202	J1128	17		FO5202	*J1133 30	15A	FO5201
LHCR2A	J05	46		FO5202	J1128	23		FO5202	*J1133 33	16B	FO5201
LHCR3A	J05	49		FO5202	J1128	40		FO5202	*J1133 39	19B	FO5201
LHCR4A	J03	48		FO5202	J1314	27		FO5203	J1314 46		FO5203
	*J1132	72	34A	FO5201	J1314	14		FO5203			
LHCTR1U	J1105	23	12A	FO5201	J1133	36	17A	FO5201	*J1227 38	18A	FO5201
LHCTR2U	J1105	20	10A	FO5201	J1133	31	15B	FO5201	*J1227 40	19A	FO5201
LHCTR3U	J1105	15	07B	FO5201	J1133	37	18B	FO5201	*J1227 42	20A	FO5201
	J1314	60		FO0602	J1316	60		FO0601			
LHCTR4U	J1123	14	06A	FO5202	J1123	27	14A	FO5202	J1123 46	21A	FO5202
	J1132	71	36A	FO5201	J1133	49	26B	FO5201	*J1227 46	21A	FO5201
	J1230	04	02A	FO5203							
LHCTR5U	J122	79	39B	FO5201	*J1227	36	17A	FO5201			
LHCT1AV	*J1105	25	11A	FO5201	J1132	34	16A	FO5201	J1133 17	08B	FO5201
LHCT2AV	*J1105	18	09A	FO5201	J1132	29	14B	FO5201	J1133 23	11B	FO5201

Table 5-6. Left Hand Assembly Key Signal Lookup-Continued

Signal	Distribution								
LHCT3AV	*J1105 10	06B	FO5201	J1132 17	08B	FO5201	J1132 35	17B	FO5201
	J1313 60		FO0603	J1315 60		FO0602			
LIBENA	*J1133 66	31A	FO5100	J1341 52	25A	FO0102	J1342 52	25A	FO0102
	J1342 68	33A	FO0102						
LIBLPR	*J1131 74	35B	FO4900	J1132 49	26B	FO4900	J133870	33A	FO0401
LIBLPS	J1131 71	36A	FO4900	*J1132 51	27B	FO4900			
LIBPFJ	*J1115 07	03A	FO4900	J1342 53	26B	FO0102			
LIBPJA	*J1118 19	09B	FO4900	J1122 03	02A	FO4900			
LIBPJ0	J1115 05	03B	FO4900	*J1122 09	04B	FO4900			
LIBWJA	*J1130 76	37A	FO5201	J1133 76	37A	FO5201			
LIBWJ0	*J1133 80	39A	FO5201	J1233 24	13A	FO5201			
LIBWTJ	J1133 74	35B	FO5201	*J1233 25	12B	FO5201			
LICRSAV	*J1120 66	32A	FO5300	J1206 04	04A	FO5300			
LITABA	*J1119 46	21A	FO5100	J1122 43	23B	FO5100			
LITINA	*J1118 20	11A	FO5002	J1130 54	25A	FO5002			
LITLB0	J1118 24	13A	FO5002	*J1122 51	27B	FO5002			
LITMAA	*J1119 01	02B	FO5100	J1120 38	20A	FO5100			
LITMA0V	J1109 35	17B	FO5100	J1119 48	22A	FO5100	*J1120 40	19A	FO5100
LITNLA	J1107 48	22A	FO5100	J1122 47	25B	FO5002	*J1132 75	37B	FO4801
	J1134 73	37B	FO4801						
LITNL0V	J1124 49	24B	FO4801	J1124 66	32B	FO4801	J1126 63	31A	FO5002
	*J1134 71	36B	FO4801						
LITRFJ	J1118 26	14A	FO5000	J1119 05	03B	FO5100	J1132 79	39B	FO4801
	*J1234 25	12B	FO5100						
LITRFK	J1118 35	17B	FO5100	*J1234 23	11B	FO5100			
LITRJA	J1122 04	04A	FO5100	*J1130 23	11B	FO5100			
LITRJ0	*J1122 01	02B	FO5100	J1234 24	13A	FO5100			
LIOLC0	J1127 65	34B	FO4801	*J1132 57	30B	FO4801			
LLBSEA	J1132 64	30A	FO5201	*J1133 69	35A	FO5201			
LLBSE0	J1130 66	31A	FO5201	*J1132 60	28A	FO5201			
LLBZ12X	*J1123 06	03A	FO5202	J1206 37	18B	FO5204			
LLBZ22X	*J1123 22	1IA	FO5202	J1206 38	18A	FO5204			
LLBZ32X	*J1123 38	18A	FO5202	J1206 40	19A	FO5204			
LLSBA2X	J1123 03	02B	FO5202	J1124 06		FO5201	*J1124 06	03A	FO5201
LLSBB2X	J1123 05	03B	FO5202	J1124 22		FO5201	*J1124 22	11A	FO5201
LMMANR	J1111 42	20A	FO5002	J1118 05	03B	FO5002	J1118 38	18A	FO5002

Table 5-6. Left Hand Assembly Key Signal Lookup-Continued

Signal	Distribution								
	*J1119 39	19B	FO4900	J1132 77	38B	FO4801	J1133 54	25A	FO5002
	J1224 03	02A	FO4900						
LMMANS	J1118 53	28B	FO4900	J1119 04	04A	FO5100	J1119 35	17B	FO4900
	J1132 20	11A	FO5002	J1135 54	25A	FO4900	*J1224 07	03A	FO4900
	J1341 49	24B	FO0102	J1342 49	24B	FO0102	J1342 66	32B	FO0102
LMPEC0V	*J1117 72	34A	FO5002	J1126 59	30B	FO5002	J1314 30		FO0802
LMPED0V	*J1117 77	38A	FO5002	J1314 13		FO0802			
LMRSJA	*J1119 45	24B	FO5300	J1120 59	31B	FO5300			
LMRSJ0V	J1115 24	13A	FO5300	*J1120 57	30B	FO5300			
LMRSTK	*J1115 23	11B	FO5300	J1122 74	35B	FO5002	J1206 01	02B	FO5300
LMTOA0V	*J1117 78	36A	FO5002	J1126 57	29B	FO5002	J1313 57		FO0802
LNORMA	J1120 33	17B	FO5002	*J1133 52	24A	FO5002			
LNORM0V	J1112 74	35B	FO5002	J1112 78	38A	FO5002	*J112031	16B	FO5002
LOPOFAV	*J1117 01		FO5100	J1122 55		FO5201			
LPARN1X	*J1124 36	17A	FO4700	J1130 26	14A	FO5100	J1131 78	38A	FO5100
LPARN2X	J1118 45	24B	FO4700	*J1124 38	18A	FO4700	J1131 49	26B	FO4801
LPINPA	*J1119 06	05A	FO4700	J1120 06	05A	FO4700			
LPINP0V	*J1120 08	04A	FO4700	J1342 40	19A	FO4700			
LPRMLTA	*J1123 73	34B	FO4700	J1342 27	14A	FO4700			
LPRMLTB	*J1123 79	37B	FO4700	J1342 08	04A	FO4700			
LPRMLTC	*J1123 74	36A	FO4700	J1342 10	05A	FO4700			
LPRMLTD	*J1123 80	38B	FO4700	J1342 14	06A	FO4700			
LPRMMTA	*J1123 55	27B	FO4700	J1342 42	20A	FO4700			
LPRMMTB	*Jl1123 61	31B	FO4700	J1342 46	21A	FO4700			
LPRMMTC	*J1123 60	28A	FO4700	J1342 24	12A	FO4700			
LPRMMTD	*J1123 63	31A	FO4700	J1342 26	13A	FO4700			
LPRM02X	J1124 40	19A	FO4700	*J1342 38	18A	FO4700			
LPRM22X	J1124 42	20A	FO4700	*J1342 22	1 IA	FO4700			
LPRM52X	J1124 46	21A	FO4700	*J1342 06	03A	FO4700			
LRBSE0	J1130 61	32B	FO5201	*J1133 60	28A	FO5201			
LRQIB0V	J1126 55	27B	FO5000	*J1134 42	18B	FO5000			
LRQIHJ	*J1115 43	23B	FO5000	J1206 08	06A	FO5002			
LRQIHK	*J1115 45	24B	FO5000	J1119 29	14B	FO5002			
LRQ0V01	*J02 60		FO5000	J1124 53	26B	FO04801	J1125 05		FO5002
	J1316 13		FO0801						
LRST1DI	J1107 06	05A	FO4900	J1107 26	14A	FO4900	J1116 64	30A	FO5002

Table 5-6. Left Hand Assembly Key Signal Lookup-Continued

Signal	Distribution								
	J1116 73	36B	FO5201	J1125 61		FO5300	*J1127 60	28A	FO5300
LRST2DI	J1125 56		FO5300	*J1127 57	30B	FO5300	J1131 72	34A	FO4900
	J1133 79	39B	FO4900	J1233 20	11A	FO5201			
LRST3DI	J1125 63		FO5300	*J1127 63	33B	FO5300			
LRST4DI	J1115 04	04A	FO4700	J1115 36	17A	FO5002	J1115 50	23A	FO5002
	J1116 04	04A	FO4900	J1116 20	11A	FO5002	J1125 75		FO5300
	*J1127 75	37B	FO5300	J1209 43	23B	FO5100			
LRST5DI	J1115 64	30A	FO5000	J1115 80	39A	FO5201	J1125 73		FO5300
	*J1127 72	34A	FO5300						
LRODEJ	*J1116 37	18B	FO5300	J1313 43		FO0802			
LRODEK	*J1116 35	17B	FO5300	J1133 56	26A	FO5002			
LSDANAV	*J1105 80	38B	FO5204	J1213 60	28A	FO5204			
LSDCGAV	*J1105 71	36B	FO5204	J1213 61	32B	FO5204			
LSDLSAV	*J1105 70	34B	FO5204	J1213 55	29B	FO5204			
LSDLS0	J1105 69	35B	FO5204	*J1206 35	17B	FO5204			
LSDLXAV	*J1105 77	38A	FO5204	J1213 62	29A	FO5204			
LSDLYAV	*J1212 46	22B	FO5204	J1213 64	30A	FO5204			
LSDWC0	J1128 05	04B	FO4801	J1128 33	16B	FO4801	J1129 05	04B	FO4801
	J1129 33	16B	FO4801	*J1213 59	31B	FO5203			
LSRSTDI	J1125 71		FO4801	*J1127 69	35A	FO4801	J1132 04	04A	FO4801
	J1132 08	06A	FO4801	J1133 24	13A	FO4801	J1135 03	02A	FO4801
	J1135 04	04A	FO4801	J1135 08	06A	FO4801	J1135 11	O5B	FO4801
	J1135 17	08B	FO4801	J1135 18	01A	FO4801	JI1135 23	11B	FO4801
	J1135 24	13A	FO4801						
LSWRSAV	J02 77		FO5300	*J1117 25	11A	FO5300	J1120 23	12A	FO5300
	J1206 07	03A	FO5300						
LSWRS0V	J02 74		FO5300	J1116 40	19A	FO5300	J1117 23	12A	FO5300
	*J1120 25	11A	FO5300						
LTCG10V	J1109 36	17A	FO4900	*J1120 24	13A	FO4900			
LTCG20V	J1110 03	02A	FO4900	*J1120 18	09A	FO4900			
L.TCMG0T	J1104 21	10B	FO4900	*J1126 08	04A	FO4900			
LTCMG1T	J1120 22	14A	FO4900	*J1126 10	05A	FO4900			
LTCMG2T	J1120 20	01A	FO4900	*J1126 14	06A	FO4900			
LTCMG6T	J1107 45	24B	FO4900	*J1126 09	05B	FO4900			
LTCMG7T	J1107 47	25B	FO4900	*J1126 11	06B	FO4900			
LTCM00T	*J1104 24	12A	FO4900	J1122 73	36B	FO5201			

Table 5-6. Left Hand Assembly Key Signal Lookup-Continued

Signal	Distribution								
LTCM01T	*J1104 26	13A	FO4900	J1132 62	29A	FO5201	J1133 64	30A	FO5201
LTCM02T	*J1104 27	14A	FO4900	J1108 27	13B	FO4900			
LTCM03T	*J1104 30	15A	FO4900	J1108 33	17B	FO4900			
LTCM04T	*J1104 33	16A	FO4900	J1107 49	26B	FO4900			
LTCM05T	*J1104 23	1 B	FO4900	J1108 36	16A	FO4900			
LTCM06T	*J1104 25	12B	FO4900	.J1108 35	18A	FO4900			
LTCM07T	*J1104 29	13B	FO4900	J1108 39	19B	FO4900			
LTCM10T	*J1104 08	04A	FO4900	J1132 47	25B	FO4900			
LTCM11T	*J1104 10	05A	FO4900	J1131 65	34B	FO4900			
LTCM12T	*J1104 14	06A	FO4900	J1109 17	08B	FO4900			
LTCM13T	*J1104 13	07A	FO4900	.J1107 24	13A	FO4900			
LTCM14T	*J1104 17	08B	FO4900	J1108 23	12A	FO4900			
LTCM15T	*J1104 07	04B	FO4900	J1108 22	14A	FO4900			
LTCM16T	*J1104 09	05B	FO4900	J113276	37A	FO4900			
LTC020V	*J1108 26	12B	FO4900	J1112 43	23B	FO4900	J1112 49	26B	FO4900
LTC030V	*J1108 31	16B	FO4900	J1119 53	28B	FO5300			
LTC050V	J1107 60	28A	FO4900	*J1108 34	15A	FO4900	J1109 56	26A	FO4900
LTC060V	*J1108 37	17A	FO4900	J1109 13	06B	FO4900	J1109 24	13A	FO4900
LTC070V	*J1108 42	18B	FO4900	J1109 10	07A	FO4900			
LTC140V	*J1108 25	11A	FO4900	J1209 37	18B	FO4900			
LTC150V	*J1108 24	13A	FO4900	J1209 19	10B	FO4900			
LTG1EA	J1104 05	03B	FO4900	*J1109 30	15A	FO4900			
LTSAG0E	J1118 03	02A	FO5002	J1126 03	02B	FO4900	J1128 03	03B	FO4801
	*J1129 07	05B	FO4801	J1132 11	05B	FO4900			
LTSAG1E	J1122 13	06B	FO5002	J1126 06	03A	FO4900	J1128 01	02B	FO4801
	*J1129 11	07B	FO4801						
LTSAG2E	J1122 19	09B	FO4900	J1126 04	02A	FO4900	J1128 04	02A	FO4801
	*J1129 13	07A	FO4801	J1341 64	30A	FO0102			
LTSAG3E	J1117 51	27B	FO4801	J1128 06	03A	FO4801	*J11129 10	05A	FO4801
	J1205 03	02B	FO5201						
LTSA3AV	*J1117 53	26B	FO4801	J1120 69	35B	FO4801			
LTSA30V	*J1120 70	34B	FO4801	J1129 19	01B	FO4801			
LTSBG0E	J1128 17	09B	FO4801	*J1129 21	11B	FO4801	J1205 06	03A	FO5201
LTSBG1E	J1128 15	08B	FO4801	*J1129 27	13B	FO4801	J1205 04	02A	FO5201
LTSBG2E	J1123 08	04A	FO5202	J1123 24	12A	FO5202	J1123 40	19A	FO5202
	J1128 18	09A	FO4801	*J1129 25	14A	FO4801	J1134 23	12A	FO5203

Table 5-6. Left Hand Assembly Key Signal Lookup-Continued

Signal	Distribution								
LTSBG3E	J1123 10	05A	FO5202	J1123 26	13A	FO5202	J1123 42	20A	FO5202
	J1128 20	10A	FO4801	*J1129 24	12A	FO4801	J1134 06	05A	FO5203
	J1205 03		FO5201	J1205 06		FO5201	J1205 04		FO5201
	J1314 08		FO5203						
LTSB2AV	J03 50		FO5202	*J1134 25	11A	FO5203	J1230 03	02B	FO5203
	J1314 24		FO5203	J1314 40		FO5203	J1314 10		FO5203
	J1314 42		FO5203						
LTSB3AV	J03 49		FO5202	*J1134 08	04A	FO5203	J1230 06	03A	FO5203
	J1314 26		FO5203						
LTSCG0E	*J1128 07	05B	FO4801	J1129 31	15B	FO4801	J1342 59	30B	FO0102
LTSCG1E	*J1128 11	07B	FO4801	J1129 29	14B	FO4801	J1342 56	28B	FO0102
LTSCG2E	*J1128 13	07A	FO4801	J1129 30	15A	FO4801	J1342 64	30A	FO0102
LTSCG3E	J1117 41	23B	FO4801	*J1128 10	05A	FO4801	J1129 34	16A	FO4801
	J1342 71	33B	FO0102						
LTSC3AV	*J1117 46	22B	FO4801	J1120 73	37B	FO4801			
LTSC30V	*J1120 71	36B	FO4801	J1128 19	10B	FO4801			
LTSDG0E	*J1128 21	11B	FO4801	J1129 43	23B	FO4801	J1205 59	30B	FO4900
	J1342 77	36B	FO0102						
LTSDG1E	J1104 03	02B	FO4900	J1104 19	09B	FO4900	*J1128 27	13B	FO4801
	J1129 41	22B	FO4801	J1205 57	29B	FO4900	J1342 72	35A	FO0102
LTSDG2E	J1104 06	03A	FO4900	J1104 22	11A	FO4900	*J1128 25	14A	FO4801
	J1129 46	21A	FO4801	J1205 55	27B	FO4900	J1342 78	38A	FO0102
LTSDG3E	J1104 04	02A	FO4900	J1104 20	10A	FO4900	*J1128 24	12A	FO4801
	J1129 48	22A	FO4801	J1205 53	26B	FO4900	J1341 59	30B	FO0102
LTSEG0E	J05 29		FO4801	J1127 40	19A	FO5002	J1128 31	15B	FO4801
	*J1129 35	17B	FO4801	J1331 71	33B	FO0902			
LTSEG1E	J05 30		FO4801	J1127 23	11B	FO5002	J1128 29	14B	FO4801
	*J1129 39	19B	FO4801	J1331 77	36B	FO0902			
LTSEG2E	J05 31		FO4801	J1127 17	08B	FO5002	J1128 30	15A	FO4801
	*J1129 42	20A	FO4801	J1331 72	35A	FO0902			
LTSEG3E	J05 32		FO4801	J1117 45	25B	FO4801	J1127 18	01A	FO5002
	J1128 34	16A	FO4801	*J1129 38	18A	FO4801	J1331 78	38A	FO0902
LTSE3AV	*J1117 43	24B	FO4801	J1120 27	13B	FO4801			
LTSE30V	*J1120 26	12B	FO4801	J1129 45	24B	FO4801			
LTSFG0E	J05 33		FO4801	J1127 24	13A	FO5002	J1128 43	23B	FO4801
	*J1129 47	25B	FO4801	J1331 53	26B	FO0902			

Table 5-6. Left Hand Assembly Key Signal Lookup-Continued

Signal	Distribution									
LTSFG1E	J05	34		FO4801	J1127	11	05B	FO5002	J1128 41	22B	FO4801
	*J1129	51	27B	FO4801	J1331	59	30B	FO0902			
LTSFG2E	J05	35		FO4801	J1127	03	02A	FO5002	J1128 46	21A	FO4801
	*J1129	56	26A	FO4801	J1331	56	28B	FO0902			
LTSFG3E	J05	36		FO4801	J1127	04	04A	FO5002	J1128 48	22A	FO4801
	*J1129	52	24A	FO4801	J1331	64	30A	FO0902			
LTSGCR	*J1132	01	02B	FO4801	J1137	05	04B	FO4801			
LTSGER	*J1133	22	12A	FO4801	J1138	09	10B	FO4801			
LTSGPR	*J1135	06	05A	FO4801	J1142	05	04B	FO4801			
LTSG0R	J1130	06	05A	FO5100	*J1135	22	12A	FO4801	J1142 09	10B	FO4801
LTSG1R	J1130	08	06A	FO5100	*J1135	01	02B	FO4801	J1141 05	04B	FO4801
LTSG2R	J1130	10	07A	FO5100	*J1135	14	09A	FO4801	J1141 09	10B	FO4801
LTSG3R	J1130	13	06B	FO5100	*J1135	09	04B	FO4801	J1140 05	04B	FO4801
LTSG4R	J1130	01	02B	FO5100	*J1135	21	10B	FO4801	J1140 09	10B	FO4801
LTSG5R	J1130	04	04A	FO5100	*J1135	15	07B	FO4801	J1139 05	04B	FO4801
LTSG6R	J1130	05	03B	FO5100	*J1135	27	13B	FO4801	J1139 09	10B	FO4801
LTSG7R	J1130	07	03A	FO5100	*J1132	06	05A	FO4801	J1138 05	04B	FO4801
LVCTGD	J05	03		FO4900	*J1112	51	27B	FO4900			
LVCTMD	J05	01		FO4900	*J1112	45	24B	FO4900			
LVMTC1U	J05	51		FO4900	*J1205	54	26A	FO4900			
LVMTC2U	J05	52		FO4900	*J1205	56	28B	FO4900			
LVMTC3U	J05	53		FO4900	*J1205	60	28A	FO4900			
LVMTC4U	J05	54		FO4900	*J1205	62	29A	FO4900			
LVMTGA	*J1100	09	04B	FO4900	J1205	63	31A	FO4900			
LWDDE0T	J02	08		FO5203	*J1230	08	04A	FO5203			
LWDDE1T	J02	09		FO5203	*J1230	10	05A	FO5203			
LWDDE2T	J02	06		FO5203	*J1230	14	06A	FO5203			
LWDDE3T	J02	07		FO5203	*J1230	13	07A	FO5203			
LWDDE4T	J02	10		FO5203	*J1230	17	08B	FO5203			
LWDDE5T	J02	11		FO5203	*J1230	07	04B	FO5203			
LWDDE6T	J02	04		FO5203	*J1230	09	05B	FO5203			
LWDDE7T	J02	05		FO5203	*J1230	11	06B	FO5203			
LOB1S0	J1128	36	17A	FO4801	J1128	50	23A	FO4801	*J1132 66	31A	FO4801
LOB2S0	J1129	36	17A	FO4801	J1129	50	23A	FO4801	*J1132 69	35A	FO4801
LOB3S0V	*J1120	13	06A	FO4801	J1128	08	04A	FO4801	J1128 22	11A	FO4801
LOB4S0V	*J1120	10	06B	FO4801	J1129	08	04A	FO4801	J1129 22	11A	FO4801'

Table 5-6. Left Hand Assembly Key Signal Lookup-Continued

Signal	Distribution								
LODBBA	*J1109 27	13B	FO5100	J1110 24	13A	FO5100	J1122 42	20A	FO5100
LODBIA	*J1109 14	09A	FO5100	J1110 26	14A	FO5100			
LODCLAV	*J1108 30	14B	FO5100	J1205 50	24A	FO5100			
LODCL0	J1108 29	15B	FO5100	*J1110 22	12A	FO5I00			
LODLC5U	J1105 59	31B	FO5100	J1109 68	32A	FO5100	*J1205 36	17A	FO5100
LODL5AV	*J1105 57	30B	FO5100	J1205 47	23A	FO5100			
LOFINA	J1130 49	26B	FO5002	*J1132 14	09A	FO5002			
LOMXLTA	J1123 71	33B	FO4700	*J1124 73	34B	FO4801	J1131 34	16A	FO4801
LOMXLTB	J1123 77	36B	FO4700	*J1124 79	37B	FO4801	J1131 37	18B	FO4801
LOMXLTC	J1123 72	35A	FO4700	*J1124 74	36A	FO4801	J1131 56	26A	FO4801
LOMXLTD	J1123 78	38A	FO4700	*J1124 80	38B	FO4801	J1131 48	22A	FO4801
LOMXMTA	J1123 53	26B	FO4700	*J1124 55	27B	FO4801	J1131 10	07A	FO4801
LOMXMTB	J1123 59	30B	FO4700	*J1124 61	31B	FO4801	J1131 05	03B	FO4801
LOMXMTC	J1123 56	28B	FO4700	*J1124 60	28A	FO4801	J1131 13	06B	FO4801
LOMXMTD	J1123 64	30A	FO4700	*J1124 63	31A	FO4801	J1131 42	20A	FO4801
LOPBXA	*J1132 52	24A	FO5100	J1134 79	39B	FO5100			
LOPBX0V	J1130 25	12B	FO5100	J1131 76	37A	FO5100	*J1134 80	38B	FO5100
LOPDVAV	J1133 70	33A	FO5100	*J1134 18	09A	FO5100			
LOPEBAV	J1119 77	38B	FO5002	*J1120 46	22B	FO5100	J1122 41	22B	FO5100
LOPRG1U	J1119 23	11B	FO5002	*J1126 70	34A	FO5100	J1134 20	10A	FO5100
LOPRG2U	J1117 05	03B	FO5100	J1118 60	28A	FO4900	*J1126 72	35A	FO5100
LOPRG3U	J1115 46	21A	FO5002	J1120 41	23B	FO5100	*J1126 74	36A	FO5100
LOPRG4U	J1120 64	33A	FO5300	*J1126 76	37A	FO5100			
LOPRLA	J1126 80	38B	FO5100	*J1131 80	39A	FO5100			
LOPOFAV	*J1117 01	02B	FO5100	J1122 55	29B	FO5201			
LOSTJA	J1108 52	26A	FO5100	*J1109 66	31A	FO5100			
LOSTJ0V	*J1108 54	25A	FO5100	J1116 54	25A	FO5100			
LOSTRJ	J1109 23	11B	FO5100	*J1116 49	26B	FO5100	J1118 22	12A	FO5002
	J1118 33	16B	FO5100	J1131 03	02A	FO4801	J1131 08	06A	FO4801
	J1131 11	05B	FO4801	J1131 30	15A	FO4801	J1131 35	17B	FO4801
	J1131 40	19A	FO4801	J1131 46	21A	FO4801	J1131 47	25B	FO4801
	J1131 54	25A	FO4801						
LOTACJ	J1109 70	33A	FO5100	*J1115 55	29B	FO5100	J1119 18	10A	FO5100
	J1123 49	24B	FO4700	J1123 66	32B	FO4700			
LOTACK	J1109 20	11A	FO5100	J1111 26	14A	FO5100	*J1115 57	30B	FO5100
	J1119 10	07A	FO4700	J1130 42	20A	FO5100			

Table 5-6. Left Hand Assembly Key Signal Lookup-Continued

Signal	Distribution								
LOTAJ0	*J1107 43	23B	FO5100	J1109 18	10A	FO5100	J1115 62	29A	FO5100
LOTSFA	J1107 46	21A	FO5I00	*J1111 55	29B	FO5100			
LOTSMA	J1107 41	22B	FO5100	*J1109 39	19B	FO5100			
L2LSR3E	J1128 59	30B	FO5001	*J1129 64	31A	FO5001			
L3LSR3E	*J1128 64	31A	FO5001	J1129 73	36B	FO5001			
L4LSR3E	J1128 73	36B	FO5001	*J1129 76	37A	FO5001			
RA401AF	*J03 52		FO4103	A02C D		FO4103			
RA403AF	*J03 53		FO4103	A02D D		FO4103			
RA401C	*J1305 52		FO4103	A04B D		FO4103			
RA403C	*J1305 50		FO4103	A04C D		FO4103			
RA405C	*J1305 41		FO4103	A04D D		FO4103			
RA407C	*J1305 36		FO4103	A04E D		FO4103			
RA409C	*J1305 31		FO4103	A04F 2A		FO4402			
RA411C	*J 1305 27		FO4103	A04G D		FO4103			
RA405D	*J1305 14		FO4103	A03A D		FO4102			
RA407D	*J1305 09		FO4103	A03G D		FO4102			
RA409D	*J1305 06		FO4103	A03N D		FO4102			
RA411D	*J1305 02		FO4103	A04A D		FO4103			
RA401L	*J1305 11		FO4103	A03A B		FO4102			
RA402L	J1305 07		FO4103	A03G B		FO4102			
RA403L	*J1305 08		FO4103	A03N B		FO4102			
RA404L	*J1305 04		FO4103	A04A B		FO4103			
RA405L	*J1305 53		FO4103	A04B B		FO4103			
RA406L	*J1305 49		FO4103	A04C B		FO4103			
RA407L	*J1305 47		FO4103	A04D B		FO4103			
RA408L	*J1305 37		FO4103	A04E B		FO4103			
RA409L	*J1305 35		FO4103	AO4F B		FO4103			
RA410L	*J1305 30		FO4103	A04G B		FO4103			
RA411L	*J03 54		FO4102	A02C B		FO4103			
RA412L	*J03 55		FO4102	A02D B		FO4103			
RAS330V	*J04 09		FO4102	J1303 01		FO4102	J1304 01		FO4103
	J1305 01		FO4103	J1306 01		FO4103	J1307 01		FO4104
RBEGEK	J04 43		FO4402	J1208 30	15A	FO4402			
RCAL10V	J1204 39	18B	FO4402	*J1212 56	28B	FO4402			
RCAL20V	J1204 41	19B	FO4402	*J1212 57	30B	FO4402			
RCAL30V	J1204 43	22B	FO4402	*J1212 68	32B	FO4402			

Table 5-6. Left Hand Assembly Key Signal Lookup-Continued

Signal	Distribution							
RC0L1AV	J1212 55	29B	FO4402	J1303 42	FO4402			
RC0L2AV	J1212 59	31B	FO4402	J1303 40	FO4402			
RC0L3AV	J1212 65	33B	FO4402	J1303 46	FO4402			
RC0L4AV	J1212 69	35B	FO4402	J1303 45	FO4402			
RC0L0S	*A03B 4A		FO4402	*A03C 4A	FO4402	*A03D 4A		FO4402
	*A03E 4A		FO4402	*A03F 4A	FO4402	*A03H 4A		FO4402
	*A03J 4A		FO4402	*A03K 4A	FO4402	*A03L 4A		FO4402
	*A03M 4A		FO4402	*A03P 4A	FO4402	*A03Q 4A		FO4402
	*A03R 4A		FO4402	*A03S 4A	FO4402	*A03T 4A		FO4402
	J1303 70		FO4402					
RC0L1S	*A03A 4A		FO4402	*A03G 4A	FO4402	*A03N 4A		FO4402
	*A03B 4A		FO4402	*A04A 4A	FO4402	*A04H 4A		FO4402
	*A06D 4A		FO4402	*A06E 4A	FO4402	*A06F 4A		FO4402
	*A07L 4A		FO4402	*A04M 4A	FO4402	*A10G 4A		FO4402
	*A10H 4A		FO4402	*A10K 4A	FO4402	*A10L 4A		FO4402
	J1303 69		FO4402					
RC0L2S	*A02C 4A		FO4402	A020D 4A	FO4402	*A02E 4A		FO4402
	*A02F 4A		FO4402	*A04C 4A	FO4402	*A04D 4A		FO4402
	*A04E 4A		FO4402	*A04F 4A	FO4402	*A04G 4A		FO4402
	*A08A 4A		FO4402	*A08B 4A	FO4402	*A08G 4A		FO4402
	*A08H 4A		FO4402	*A08J 4A	FO4402	*A08K 4A		FO4402
	*A08L 4A		FO4402	*A08M 4A	FO4402	J1303 72		FO4402
RC0L5S	*A02A 4A		FO4402	*A02B 4A	FO4402	*A06A 4A		FO4402
	*A06G 4A		FO4402	*A03H 4A	FO4402	*A03J 4A		FO4402
	*A03K 4A		FO4402	*A06L 4A	FO4402	*A06M 4A		FO4402
	*A07A 4A		FO4402	*A07B 4A	FO4402	*A07C 4A		FO4402
	*A07D 4A		FO4402	*A07E 4A	FO4402			
	*A07F 4A		FO4402	*A07K 4A	FO4402	J1303 63		FO4402
RC0L6S	*A07G 4A		FO4402	*A07H 4A	FO4402	*A07J 4A		FO4402
	*A10A 4A		FO4402	*A10B 4A	FO4402	*A10C 4A		FO4402
	*A10D 4A		FO4402	*A10E 4A	FO4402	*A10F 4A		FO4402
	A10J 4A		FO4402	*A10M 4A	FO4402	J1303 62		FO4402
	J02 45		FO4402	J1303 62	FO4402	*A06B 4A		FO4402
	*A06C 4A		FO4402					
RC0MP0	J1204 71	33B	FO4103	J1305 68	FO4103			
RC01DAV	*J1212 18	09A	FO4402	J1303 71	FO4402			

Table 5-6. Left Hand Assembly Key Signal Lookup-Continued

Signal	Distribution								
RC01D0	J1212 20	10A	FO4402	*J1216 72	34A	FO4402	J1218 61	31A	FO4402
RC02DAV	*J1218 63	30A	FO4402	J1221 10	07A	FO4402			
RD405AF	*J03 63		FO4102	A02E D		FO4103			
RD407AF	*J03 56		FO4102	A06A B		FO4104			
RD409AF	*J03 59		FO4102	A06B B		FO4104			
RD411AF	*J03 62		FO4102	A06C B		FO4104			
RD401BF	*J1307 52		FO4104	A06G D		FO4104			
RD403BF	*J1307 50		FO4104	A06H D		FO4104			
RD405BF	*J1307 41		FO4104	A06J D		FO4104			
RD407BF	*J1307 36		FO4104	A06K D		FO4104			
RD409BF	*J1307 31		FO4104	A06L D		FO4104			
RD411BF	*J1307 27		FO4104	A06M D		FO4104			
RD401L	*J1307 53		FO4104	A06G B		FO4104			
RD402L	*J1307 49		FO4104	A06H B		FO4104			
RD403L	*J1307 47		FO4104	A06J B		FO4104			
RD404L	*J1307 37		FO4104	A06K B		FO4104			
RD405L	*J1307 35		FO4104	A06L B		FO4104			
RD406L	*J1307 30		FO4104	A06M B		FO4104			
RD407L	*J03 57		FO4102	A06A D		FO4104			
RD408L	*J03 58		FO4102	A06B D		FO4104			
RD409L	*J03 60		FO4102	A06C D		FO4104			
RD410L	*J03 61		FO4103	A02E B		FO4103			
RD412L	*J1305 75		FO4103	A02B D		FO4103			
RE401L	*J1306 59		FO4103	A01A D		FO4103			
RE402L	*J1306 60		FO4103	A01B D		FO4103			
RE403L	*J1306 55		FO4103	A01C D		FO4103			
RE404L	*J1305 59		FO4103	A10D D		FO4103			
RE405L	*J1305 60		FO4103	A01E D		FO4103			
RE406L	*J1305 55		FO4103	A01F D		FO4103			
REGNTA	*J04 26		FO4402	J1204 35	16B	FO4402	J1204 49	24B	FO4402
REL1K0E	*J04 18		FO4102	J1204 04	02A	FO4102	J1204 20	10A	FO4102
	J1207 14	06A	FO4104	J1207 27	14A	FO4104	J1336 14	06A	FO4104
REL1K1E	*J04 19		FO4102	J1204 06	03A	FO4102	J1204 22	11A	FO4102
	J1207 10	05A	FO4104	J1207 26	13A	FO4104	J1336 10	05A	FO4104
REL1K3E	J04 21		FO4102	J1216 74	35B	FO4104	J1220 73	36B	FO4104
	J1336 13	07A	FO4104						

Table 5-6. Left Hand Assembly Key Signal Lookup-Continued

Signal				Distribution						
RFL0D01	*J1303	79		FO4102	*J1303	80	FO4102	A09G	04	FO4104
RFL0D02	*J1303	75		FO4102	A09H	04	FO4104			
RFL0D03	*J1303	73		FO4102	A09J	04	FO4104			
RFL0D04	*J1303	59		FO4102	A09K	04	FO4104			
RFL0D05	*J1303	60		FO4102	A09L	04	FO4104			
RFL0D06	*J1303	55		FO4102	A09M	04	FO4104			
RFL0D07	*J1304	79		FO4103	*J1304	80	FO4103	A09A	04	FO4104
RFL0D08	*J1304	75		FO4103	A09B	04	FO4104			
RFL0D09	*J1304	73		FO4103	A09C	04	FO4104			
RFL0D10	*J1304	59		FO4103	A09D	04	FO4104			
RFL0D11	*J1304	60		FO4103	A09E	04	FO4104			
RFL0D12	*J1304	55		FO4103	A09F	04	FO4104			
RFL1AA	*J04	61		FO4102	J1204	03	02B	FO4102	J1207	08	04A	FO4104
RFL1BA	*J04	62		FO4102	J1204	05	03B	FO4102				
RFL1CA	*J04	20		FO4102	J1204	19	09B	FO4102	J1207	24	12A	FO4104
RFL1DA	*J04	76		FO4102	J1204	21	10B	FO4102				
RFPTS2X	*J1208	22	11A	FO4402	J1311	04	04A	FO4402				
RF409L	J03	69		FO4104	J1307	59		FO4104				
RF410L	J03	70		FO4104	J1307	60		FO4104				
RF411L	J03	71		FO4104	J1307	55		FO4104				
RGA01L	*J1303	26		FO4102			A03B D	FO4102				
RGA02L	*J1303	25		FO4102			A03B B	FO4102				
RGA03L	*J1303	13		FO4102	A03C D			FO4102				
RGA04L	*J1303	15		FO4102			A03C B	FO4102				
RGA05L	*J1303	14		FO4102			A03E D	FO4102				
RGA06L	*J1303	11		FO4102			A03E B	FO4102				
RGA07L	*J1303	09		FO4102			A03F D	FO4102				
RGA08L	*J1303	07		FO4102			A03F B	FO4102				
RGA09L	*J1303	06		FO4102	A03H D			FO4102				
RGA10L	*J1303	08		FO4102			A03H B	FO4102				
RGA11L	*J1303	02		FO4102			A03J D	FO4102				
RGA12L	*J1303	04		FO4102			A03J B	FO4102				
RGB01L	*J1303	52		FO4102			A03L D	FO4102				
RGB02L	*J1303	53		FO4102			A03L B	FO4102				
RGB03L	*J1303	50		FO4102	A03M D			FO4102				
RGB04L	*J1303	49		FO4102	A03M B			FO4102				

Table 5-6. Left Hand Assembly Key Signal Lookup-Continued

Signal		Distribution		
RGB05L	*J1303 41	FO4102	A03P D	FO4102
RGB06L	*J1303 47	FO4102	A03P B	FO4102
RGB07L	*J1303 36	FO4102	A03Q D	FO4102
RGB08L	*J1303 37	FO4102	A03Q B	FO4102
RGB09L	*J1303 31	FO4102	A03S D	FO4102
RGB10L	*J1303 35	FO4102	A03S B	FO4102
RGB11L	*J1303 27	FO4102	A03T D	FO4102
RGB12L	*J1303 30	FO4102	A03T B	FO4102
RGC01L	*J1304 26	FO4103	A03D D	FO4102
RGC02L	*J1304 25	FO4103	A03D B	FO4102
RGC03L	*J1304 13	FO4103	A03K D	FO4102
RGC04L	*J1304 15	FO4103	A03K B	FO4102
RGC05L	*J1304 14	FO4103	A03R D	FO4102
RGC06L	*J1304 11	FO4103	A03R B	FO4102
RGC07L	*J1304 09	FO4103	A06D D	FO4104
RGC08L	*J1304 07	FO4103	A06D B	FO4104
RGC09L	*J1304 06	FO4103	A06E D	FO4104
RGC10L	*J1304 08	FO4103	A06E B	FO4104
RGC11L	*J1304 02	FO4103	A06F D	FO4104
RGC12L	*J1304 04	FO4103	A06F B	FO4104
RGD01L	*J1304 52	FO4103	A07L D	FO4104
RGD02L	*J1304 53	FO4103	A07L B	FO4104
RGD03L	*J1304 50	FO4103	A07M D	FO4104
RGD04L	*J1304 49	FO4103	A07M B	FO4104
RGD05L	*J1304 41	FO4103	A04H D	FO4103
RGD06L	*J1304 47	FO4103	A04H B	FO4103
RGD07L	*J1304 36	FO4103	A10G D	FO4103
RGD08L	*J1304 37	FO4103	A10G B	FO4103
RGD09L	*J1304 31	FO4103	A10H D	FO4103
RGD10L	*J1304 35	FO4103	A10H B	FO4103
RGD11L	*J1304 27	FO4103	A10K D	FO4103
RGD12L	*J1304 30	FO4103	A10K B	FO4103
RGE01L	*J1305 26	FO4103	A10L D	FO4103
RGE02L	*J1305 25	FO4103	A10L B	FO4103
RGE03L	*J1305 13	FO4103	A02F D	FO4103
RGE04L	*J1305 15	FO4103	A02F B	FO4103

Table 5-6. Left Hand Assembly Key Signal Lookup-Continued

Signal				Distribution							
RGE05L	*J1305	80		FO4103	A02A	D	FO4103				
RGE06L	*J1305	79		FO4103	A02A	B	FO4103				
RGE10L	*J1305	73		FO4103	A07K	B	FO4104				
RGF01L	*J1307	26		FO4104	A07A	D	FO4104				
RGF02L	*J1307	25		FO4104	A07A	B	FO4104				
RGF03L	*J1307	13		FO4104	A07B	D	FO4104				
RGF04L	*J1307	15		FO4104	A07B	B	FO4104				
RGF05L	*J1307	14		FO4104	A07C	B	FO4104				
RGF06L	*J1307	11		FO4104	A07C	D	FO4104				
RGF07L	*J1307	09		FO4104	A07D	D	FO4104				
RGF08L	*J1307	07		FO4104	A07D	B	FO4104				
RGF09L	*J1307	06		FO4104	A07E	D	FO4104				
RGF10L	*J1307	08		FO4104	A07E	B	FO4104				
RGF11L	*J1307	02		FO4104	A07F	D	FO4104				
RGF12L	*J1307	04		FO4104	A07F	B	FO4104				
RGP01S	*A08C	2A		FO4402	J1306	70	FO4402				
RGP02S	*A08D	2A		FO4402	J1306	69	FO4402				
RGP03S	*A08E	2A		FO4402	J1306	72	FO4402				
RGP04S	*A08F	2A		FO4402	J1306	71	FO4402				
RGP05S	*A09	S12		FO4402	*A09J1	9	FO4402	J1306	66		FO4402
RGP06S	*A09	S11		FO4402	*A09J1	10	FO4402	J1306	63		FO4402
RGP07S	*A09	S10		FO4402	*A09J1	11	FO4402	J1306	62		FO4402
RGP08S	*A09	S9		FO4402	*A09J1	12	FO4402	J1306	61		FO4402
RGP09S	*A09	S8		FO4402	*A09J1	13	FO4402	J1307	70		FO4402
RGP10S	*A09	S7		FO4402	*A09J1	14	FO4402	J1307	69		FO4402
RGP11S	*A09	S6		FO4402	*A09J1	1	FO4402	J1307	72		FO4402
RGP12S	*A09	S5		FO4402	*A09J1	2	FO4402	J1302	71		FO4402
RGP13S	*A09	S4		FO4402	*A09J1	3	FO4402	J1302	66		FO4402
RGP14S	*A09	S3		FO4402	*A09J1	6	FO4402	J1302	63		FO4402
RGP15S	*A09	S2		FO4402	*A09J1	7	FO4402	J1302	62		FO4402
RGP16S	*A09	S1		FO4402	*A09J1	8	FO4402	J1302	61		FO4402
RGRUNAV	J04	66		FO4402	J1303	66	FO4402				
RGSELJ	*J04	40		FO4102	J1216	65	34B FO4104				
RGSELK	*J04	41		FO4102	J1336	08	04A FO4104				
RGUPAA	J1207	13	07A	FO4104	*J1216	69	35A FO4104	J1220	71	36A	FO4104
RGUPBA	J1207	30	15A	FO4104	*J1220	72	34A FO4104				

Table 5-6. Left Hand Assembly Key Signal Lookup-Continued

Signal	Distribution							
RHCL00T	*J1205 24	12A	FO4103	J1302 13	FO4103			
RHCL01T	*J1205 26	13A	FO4103	J1302 10	FO4103			
RHCL02T	*J1205 27	14A	FO4103	J1302 17	FO4103			
RHCL03T	*J1205 30	15A	FO4103	J1302 19	FO4103			
RHCL04T	*J1205 33	16A	FO4103	J1302 39	FO4103			
RHCL05T	*J1205 23	11B	FO4103	J1302 35	FO4103			
RHCL06T	*J1205 25	12B	FO4103	J1302 41	FO4103			
RHCL07T	*J1205 29	13B	FO4103	J1302 45	FO4103			
RHCL09T	*J1205 34	15B	FO4103	J1302 61	FO4103			
RHCL12T	*J1231 27	14A	FO4103	J1302 69	FO4103			
RHCL13T	*J1231 30	15A	FO4103	J1302 71	FO4103			
RHC01D	A09A 12		FO4104	A09B 12	FO4104	A09C 12		FO4104
	A09D 12		FO4104	A09E 12	FO4104	A09F 12		FO4104
	A09G 12		FO4104	A09H 12	FO4104	A09J 12		FO4104
	A09K 12		FO4104	A09L 12	FO4104	A09M 12		FO4104
	*J1302 03		FO4103					
RHC02D	A09A 11		FO4104	A09B 11	FO4104	A09C 11		FO4104
	A09D 11		FO4104	A09E 11	FO4104	A09F 11		FO4104
	A09G 11		FO4104	A09H 11	FO4104	A09J 11		FO4104
	A09K 11		FO4104	A09L 11	FO4104	A09M 11		FO4104
	*J1302 05		FO4103					
RHC03D	A09A 10		FO4104	A09B 10	FO4104	A09C 10		FO4104
	A09D 10		FO4104	A09E 10	FO4104	A09F 10		FO4104
	A09G 10		FO4104	A09H 10	FO4104	A09J 10		FO4104
	A09K 10		FO4104	A09L 10	FO4104	A09M 10		FO4104
	*J1302 23		FO4103					
RHC04D	A09A 09		FO4104	A09B 09	FO4104	A09C 09		FO4104
	A09D 09		FO4104	A09E 09	FO4104	A09F 09		FO4104
	A09G 09		FO4104	A09H 09	FO4104	A09J 09		FO4104
	A09K 09		FO4104	A09L 09	FO4104	A09M 09		FO4104
	*J1302 21		FO4103					
RHC05D	A09A 08		FO4104	A09B 08	FO4104	A09C 08		FO4104
	A09D 08		FO4104	A09E 08	FO4104	A09F 08		FO4104
	A09G 08		FO4104	A09H 08	FO4104	A09J 08		FO4104
	A09K 08		FO4104	A09L 08	FO4104	A09M 08		FO4104
	*J1302 25		FO4103					

Table 5-6. Left Hand Assembly Key Signal Lookup-Continued

Signal	Distribution							
RCH06D	A09A 07		FO4104	A09B 07	FO4104	A09C 07		FO4104
	A09D 07		FO4104	A09E 07	FO4104	A09F 07		FO4104
	A09G 07		FO4104	A09H 07	FO4104	A09J 07		FO4104
	A09K 07		FO4104	A09L 07	FO4104	A09M 07		FO4104
	*J1302 33		FO4103					
RHC07D	A09A 06		FO4104	A09B 06	FO4104	A09C 06		FO4104
	A09D 06		FO4104	A09E 06	FO4104	A09F 06		FO4104
	A09G 06		FO4104	A09H 06	FO4104	A09J 06		FO4104
	A09K 06		FO4104	A09L 06	FO4104	A09M 06		FO4104
	*J1302 53		FO4103					
RHC08D	A09A 05		FO4104	A09B 05	FO4104	A09C 05		FO4104
	A09D 05		FO4104	A09E 05	FO4104	A09F 05		FO4104
	A09G 05		FO4104	A09H 05	FO4104	A09J 05		FO4104
	A09K 05		FO4104	A09L 05	FO4104	A09M 05		FO4104
	*J1302 51		FO4103					
RHC10D	A09A 03		FO4104	A09B 03	FO4104	A09C 03		FO4104
	A09D 03		FO4104	A09E 03	FO4104	A09F 03		FO4104
	A09G 03		FO4104	A09H 03	FO4104	A09J 03		FO4104
	A09K 03		FO4104	A09L 03	FO4104	A09M 03		FO4104
	*J1302 57		FO4103					
RHC11D	A09A 02		FO4104	A09B 02	FO4104	A09C 02		FO4104
	A09D 02		FO4104	A09E 02	FO4104	A09F 02		FO4104
	A09G 02		FO4104	A09H 02	FO4104	A09J 02		FO4104
	A09K 02		FO4104	A09L 02	FO4104	A09M 02		FO4104
	*J1302 75		FO4103					
RHC12D	A09A 01		FO4104	A09B 01	FO4104	A09C 01		FO4104
	A09D 01		FO4104	A09E 01	FO4104	A09F 01		FO4104
	A09G 01		FO4104	A09H 01	FO4104	A09J 01		FO4104
	A09K 01		FO4104	A09L 01	FO4104	A09M 01		FO4104
	*J1302 73		FO4103					
RKILM0	J1204 77	36B	FO4103	J1305 78	FO4103			
RLDL00E	J1207 03	02B	FO4104	J1303 21	FO4102			
RLDL01E	J1207 05	03B	FO4104	J1303 22	FO4102			
RLDL02E	J1207 07	04B	FO4104	J1303 43	FO4102			
RLDL03E	J1207 09	05B	FO4104	J1304 21	FO4103			
RLDL10E	J1207 11	06B	FO4104	J1304 22	FO4103			

Table 5-6. Left Hand Assembly Key Signal Lookup-Continued

Signal	Distribution											
RLDL11E	J1207	15	07B	FO4104	J1304	43		FO4103				
RLDL12E	J1207	18	09A	FO4104	*J1305	21		FO4103				
RLDL13E	J1207	17	08B	FO4104	*J1305	22		FO4103				
RLDL20E	*J1305	43		FO4103	J1336	03	02B	FO4104				
RLDL21E	J1207	19	09B	FO4104	*J1306	21		FO4103				
RLDL22E	J1207	21	01B	FO4104	*J1306	22		FO4103				
RLDL23E	J1207	23	11B	FO4104	*J1306	43		FO4103				
RLDL30E	J1207	25	12B	FO4104	J1307	21		FO4104				
RLDL31E	J1207	29	13B	FO4104	J1307	22		FO4104				
RLDL32E	J1207	31	14B	FO4104	J1307	43		FO4104				
RLDL33E	*J04	55		FO4102	J1207	34	15B	FO4104				
RLDL40E	*J04	57		FO4102	J1207	33	16A	FO4104				
RLDL41E	*J04	59		FO4102	J1336	11	06B	FO4104				
RLENCAV	J1216	71	36A	FO4402	J1306	45		FO4402				
RLENDAV	*J1218	03	03A	FO4103	J1231	21	01B	FO4103				
RLENGAV	J1216	73	36B	FO4402	J1217	61	32B	FO4402	J1307	45		FO4402
RLENT0E	J1206	20	10A	FO4103	J1231	20	10A	FO4103	*J1306	78		FO4103
RLENT1E	J1205	22	11A	FO4103	J1231	22	11A	FO4103	*J1306	77		FO4103
RLENT2E	J1205	19	09B	FO4103	J1231	19	09B	FO4103	*J1306	76		FO4103
RLENT3E	J1205	21	10B	FO4103	J1218	04	02A	FO4103	*J1306	68		FO4103
RLEN1AV	J1217	78	38A	FO4402	J1307	42		FO4402				
RLEN1NA	J 1306	42		FO4402	J1307	51		FO4402				
RLEN2AV	J1217	72	34A	FO4402	J1307	40		FO4402				
RLEN2NB	J1306	40		FO4402	J1307	54		FO4402				
RLEN3AV	J1217	79	39B	FO4402	J1307	46		FO4402				
RLEN3NC	J1306	46		FO4402	J1307	48		FO4402				
RLRHMJ	*J04	42		FO4102	J1303	05		FO4102	J1304	05		FO4103
	J1305	05		FO4103	J1306	05		FO4103	J1307	05		FO4104
RLRQ1D4	J03	44		FO0500	J1222	76		FO0500	J1332	37	17B	FO0500
	J1341	72	35A	FO0500								
RMUX51X	*J1208	04	02A	FO4502	J1311	08	06A	FO4502				
RMUX72X	*J1207	06	03A	FO4104	J1217	53	28B	FO4104				
RMUX82X	*J1207	22	11A	FO4104	J1217	60	28A	FO4104				
RMU112X	J1217	62	29A	FO4104	*J1336	06	03A	FO4104				
RMXC1D4	J05	65		FO4502	J1211	66		FO4502	J1212	61	31A	FO4502
	J1222	78		FO4502								

Table 5-6. Left Hand Assembly Key Signal Lookup-Continued

Signal	Distribution									
RMXC2D4	J05	67		FO4502	J1211	65		FO4502	J1212 64	33A	FO4502
	J1222	61		FO4502							
RMXC3D4	J05	69		FO4502	J1211	63		FO4502	J1212 51	27B	FO4502
	J1222	63		FO4502							
RMXC54U	J04	69		FO4502	J1208	13	07A	FO4502			
RMXL10V	J1208	14	06A	FO4502	J1208	27	14A	FO4402	*J1212 63	30A	FO4502
RMXL20V	J1208	10	05A	FO4502	J1208	26	13A	FO4402	*J1212 66	32A	FO4502
RMXL30V	J1208	08	04A	FO4502	J1208	24	12A	FO4402	*J1212 53	26B	FO4502
RM1LE0	J1204	75	35B	FO4103	*J1305	77		FO4103			
RRAZH0	J1204	73	34B	FO4103	*J1305	76		FO4103			
RRWVD0V	J05	16		FO4104	*J1134	01	02B	FO4103			
RSENAJQ	J04	23		FO4402	*J1209	80	39A	FO4402	J1216 50	23A	FO4402
RSENAKQ	J04	22		FO4402	*J1209	79	39B	FO4402			
RSWPEA	J1204	50	24A	FO4402	J1204	63	31A	FO4402	*J1216 46	21A	FO4402
RSWTF1U	*J1204	38	18A	FO4402	J1208	29	13B	FO4402			
RSWTF2U	*J1204	40	19A	FO4402	J1208	31	14B	FO4402			
RSWTF3U	*J1204	42	20A	FO4402	J1208	34	15B	FO4402			
RSWTF4U	*J1204	46	21A	FO4402	J1208	33	16A	FO4402			
RSWTL1U	*J1204	54	26A	FO4402	J1208	19	09B	FO4402			
RSWTL2U	*J1204	56	28B	FO4402	J1208	21	01B	FO4402			
RSWTL3U	*J1204	60	28A	FO4402	J1208	23	11B	FO4402			
RSWTL4U	*J1204	62	29A	FO4402	J1208	25	12B	FO4402			
RS1G10V	*J1212	70	34B	FO4402	J1217	66	31A	FO4402			
RS1G20	J1217	68	32A	FO4402	*J1221	11	05B	FO4402			
RTA000V	*J1134	07	04B	FO4102	J1303	03		FO4102			
RTA010V	*J1134	10	06B	FO4102	J1303	29		FO4102			
RTA020V	*J1134	14	08B	FO4102	J1303	20		FO4102			
RTA030V	*J1134	19	O1B	FO4102	J1304	03		FO4103			
RTA040V	*J1134	26	12B	FO4102	J1304	29		FO4103			
RTA050V	*J1134	31	16B	FO4102	J1304	20		FO4103			
RTA060V	*J1134	37	17A	FO4102	J1305	03		FO4103			
RTA070V	*J1134	40	19A	FO4102	J1305	29		FO4103			
RTA080V	*J1134	43	24B	FO4102	J1204	80	38B	FO4103	J1305 20		FO4103
RTA100V	*J1134	46	22B	FO4102	J1306	03		FO4103			
RTA110V	*J1134	48	21A	FO4102	J1306	29		FO4103			
RTA120V	*J1134	53	26B	FO4102	J1306	20		FO4103			

Table 5-6. Left Hand Assembly Key Signal Lookup-Continued

Signal				Distribution							
RTA130V	*J1134	57	30B	FO4102	J1307	03		FO4104			
RTA140V	*J1134	60	28A	FO4102	J1307	29		FO4104			
RTA150V	*J1134	63	30A	FO4102	J1307	20		FO4104			
RTA160V	J04	47		FO4102	*J1134	66	32A	FO4102			
RTA170V	J04	48		FO4102	*J1134	68	32B	FO4102			
RTA180V	J04	49		FO4102	*J1134	70	34B	FO4102			
RTA190V	J04	53		FO4102	*J1134	49	23A	FO4102			
RTMT00	J1208	03	02B	FO4502	J1211	05		FO4502	*A05A	1	FO4502
RTMT10	J1208	05	03B	FO4502	J1211	09		FO4502	*A05A	2	FO4502
RTMT20	J1208	07	04B	FO4502	J1211	17		FO4502	*A05B	1	FO4502
RTMT30	J1208	09	05B	FO4502	J1211	20		FO4502	*A05B	2	FO4502
RTMT40	J1208	11	06B	FO4502	J1211	24		FO4502	*A05B	4	FO4502
RTMT60	J1208	15	07B	FO4502	J1211	26		FO4502	*A05B	8	FO4502
RTON00T	J1134	09	05B	FO4102	*J1204	08	04A	FO4102			
RTON01T	J1134	15	07B	FO4102	*J1204	10	05A	FO4102			
RTON02T	J1134	17	09B	FO4102	*J1204	14	06A	FO4102			
RTON03T	J1134	21	11B	FO4102	*J1204	13	07A	FO4102			
RTON04T	J1134	27	13B	FO4102	*J1204	17	08B	FO4102			
RTON05T	J1134	33	17B	FO4102	*J1204	07	04B	FO4102			
RTON06T	J1134	35	18A	FO4102	*J1204	09	05B	FO4102			
RTON07T	J1134	38	20A	FO4102	*J1204	11	06B	FO4102			
RTON08T	J1134	45	25B	FO4102	*J1204	15	07B	FO4102			
RTON10T	J1134	41	23B	FO4102	*J1204	24	12A	FO4102			
RTON11T	J1134	50	22A	FO4102	*J1204	26	13A	FO4102			
RTON12T	J1134	51	27B	FO4102	*J1204	27	14A	FO4102			
RTON13T	J1134	59	31B	FO4102	*J1204	30	15A	FO4102			
RTON14T	J1134	62	29A	FO4102	*J1204	33	16A	FO4102			
RTON15T	J1134	61	31A	FO4102	*J1204	23	11B	FO4102			
RTON16T	J1134	64	33A	FO4102	*J1204	25	12B	FO4102			
RTON17T	J1134	65	33B	FO4102	*J1204	29	13B	FO4102			
RTON18T	J1134	69	35B	FO4102	*J1204	31	14B	FO4102			
RTON19T	J1134	47	24A	FO4102	*J1204	34	15B	FO4102			
RTS01AD	*J1306	52		FO4103	A08A	D		FO4103			
RTS02AD	*J1306	53		FO4103	A08A	B		FO4103			
RTS03AD	*J1306	50		FO4103	A08B	D		FO4103			
RTS04AD	*J1306	49		FO4103	A08B	B		FO4103			

Table 5-6. Left Hand Assembly Key Signal Lookup-Continued

Signal				Distribution			
RTS05AD	*J1306	41		FO4103	A08C	D	FO4103
RTS06AD	*J1306	47		FO4103	A08C	B	FO4103
RTS07AD	*J1306	36		FO4103	A08D	D	FO4103
RTS08AD	*J1306	37		FO4103	A08D	B	FO4103
RTS09AD	*J1306	31		FO4103	A08E	D	FO4103
RTS10AD	*J1306	35		FO4103	A08E	B	FO4103
RTS11AD	*J1306	27		FO4103	A08F	D	FO4103
RTS12AD	*J1306	30		FO4103	A08F	B	FO4103
RTS01BD	*J1306	26		FO4103	A08G	D	FO4103
RTS02BD	*J1306	25		FO4103	A08G	B	FO4103
RTS03BD	*J1306	13		FO4103	A08H	D	FO4103
RTS04BD	*J1306	15		FO4103	A08H	B	FO4103
RTS05BD	*J1306	14		FO4103	A08J	D	FO4103
RTS06BD	J1306	11		FO4103	A08J	B	FO4103
RTS07BD	J1306	09		FO4103	A08K	D	FO4103
RTS08BD	*J1306	7		FO4103	A08K	B	FO4103
RTS09BD	*J1306	6		FO4103	A08L	D	FO4103
RTS10BD	J1306	8		FO4103	A08L	B	FO4103
RTS11BD	*J1306	2		FO4103	A08M	D	FO4103
RTS12BD	*J1306	4		FO4103	A08M	B	FO4103
RUX5DD4	J05	61		FO4502	*J1311	06	05A FO4502
RVCSR1U	J1134	05	03B	FO4103	*J1204	70	34A FO4103
RVCSR2U	J05	15		FO4104	*J1204	72	35A FO4103
RVCSR3U	J05	13		FO4104	*J1204	74	36A FO4103
RVCSR4U	J05	14		FO4104	*J1204	76	37A FO4103
RXSWDD4	J05	63		FO4402	*J1311	01	02B FO4402
ROACH0	J05	71		FO4104	*J1217	55	29B FO4104
ROWA10	J1204	53	26B	FO4402	*J1217	80	39A FO4402
ROWA20	J1204	55	27B	FO4402	*J1217	74	36B FO4402
ROWA30	J1204	57	29B	FO4402	*J1217	73	36B FO4402
ROWA40	J1204	59	30B	FO4402	*J1217	63	33B FO4402
ROWB1AV	J1217	69	35A	FO4402	J1304	42	FO4402
ROWB1NA	J1304	51		FO4402	J1305	42	FO4402
ROWB2AV	J1217	65	34B	FO4402	J1304	40	FO4402
ROWB2NB	J1304	54		FO4402	J1305	40	FO4402
ROWB3AV	J1217	75	37B	FO4402	J1304	46	FO4402

Table 5-6. Left Hand Assembly Key Signal Lookup-Continued

Signal	Distribution											
ROWB3NC	J1304	48		FO4402	J1305	46		FO4402				
ROWB4AV	J1217	57	30B	FO4402	J1221	06	05A	FO4402	J1305	45		FO4402
ROWB5AV	J1221	08	06A	FO4402	J1304	45		FO4402				
ROWR1AV	J04	11		FO4402	J1217	76	37A	FO4402				
ROWR2AV	J04	12		FO4402	J1217	71	36A	FO4402				
ROWR3AV	J04	13		FO4402	J1217	77	38B	FO4402				
ROWR4AV	J04	14		FO4402	J1221	13	06B	FO4402				
ROW01S	*A02A	2A		FO4402	*A04C	2A		FO4402	*A06B	2A		FO4402
	*A06D	2A		FO4402	J1304	70		FO4402				
ROW02S	*A02B	2A		FO4402	*A03B	2A		FO4402	*A04D	2A		FO4402
	*A06C	2A		FO4402	*A06E	2A		FO4402	J1304	69		FO4402
ROW03S	*A03C	2A		FO4402	*A04E	2A		FO4402	*A06F	2A		FO4402
	*A07G	2A		FO4402	*A07K	2A		FO4402	J1304	72		FO4402
ROW04S	*A03E	2A		FO4402	*A04F	2A		FO4402	*A07A	2A		FO4402
	*A07H	2A		FO4402	*A07L	2A		FO4402	J1304	71		FO4402
ROW05S	*A03F	2A		FO4402	*A04G	2A		FO4402	*A07B	2A		FO4402
	*A07J	2A		FO4402	*A04M	2A		FO4402	J1304	66		FO4402
ROW06S	*A02C	2A		FO4402	*A03H	2A		FO4402	*A04H	2A		FO4402
	*A07C	2A		FO4402	*A10J	2A		FO4402	J1304	63		FO4402
ROW07S	*A02D	2A		FO4402	*A03J	2A		FO4402	*A07D	2A		FO4402
	*A10H	2A		FO4402	*A10M	2A		FO4402	J1304	62		FO4402
ROW08S	*A02E	2A		FO4402	*A03L	2A		FO4402	*A07E	2A		FO4402
	*A10A	2A		FO4402	*A10G	2A		FO4402	J1304	61		FO4402
ROW09S	*A03M	2A		FO4402	*A07F	2A		FO4402	*A08G	2A		FO4402
	*A10A	2A		FO4402	*A10K	2A		FO4402	J1305	70		FO4402
ROW10S	*A03P	2A		FO4402	*A06G	2A		FO4402	*A08H	2A		FO4402
	*A10C	2A		FO4402	*A10L	2A		FO4402	J1303	69		FO4402
ROW11S	*A02F	2A		FO4402	*A03Q	2A		FO4402	*A03H	2A		FO4402
	*A08J	2A		FO4402	*A10D	2A		FO4402	J1305	72		FO4402
ROW12S	*A03A	2A		FO4402	J03	64		FO4402	*A03S	2A		FO4402
	*A03J	2A		FO4402	*A03K	2A		FO4402	*A10E	2A		FO4402
	J1305	71		FO4402								
ROW13S	J03	65		FO4402	*A03G	2A		FO4402	*A03T	2A		FO4402
	*A03K	2A		FO4402	*A08L	2A		FO4402	*A10F	2A		FO4402
	J1305	66		FO4402								
ROW14S	J02	46		FO4402	J1305	63		FO4402	J03	66		FO4402

Table 5-6. Left Hand Assembly Key Signal Lookup-Continued

Signal	Distribution								
	*A03D 2A		FO4402	*A03N 2A		FO4402	*A06L 2A		FO4402
	*A08M 2A		FO4402						
ROW 15S	*A03K 2A		FO4402	J03 67		FO4402	*A04A 2A		FO4402
	*A06M 2A		FO4402	*A08A 2A		FO4402	J1305 62		FO4402
ROW 16S	J03 68		FO4402	*A03R 2A		FO4402	*A04B 2A		FO4402
	*A06A 2A		FO4402	*A08B 2A		FO4402	J1305 61		FO4402
R1IDSCA	J1209 74	36A	FO4402	J1212 62	29A	FO4402	*J1217 64	30A	FO4402
RIDSW0V	J1204 45	23B	FO4402	J1209 77	38B	FO4402	*J1212 60	28A	FO4402
R1NVE0V	J04 15		FO4402	J1209 75	37B	FO4402	J1216 48	22A	FO4402
R5MZBA	*J1122 63	33B	FO5402	J1204 37	17B	FO4402	J1204 51	25B	FO4402
	J1303 19		FO4102	J1304 19		FO4103	J1305 19		FO4103
	J1306 19		FO4103	J1307 19		FO4104			
SPI001	*J1125 65								
SPI002	*J1125 66								
SPI003	*J1125 72								
SPI004	*J1125 74								
SPI005	*J1125 76								
SPI006	*J1125 77								
SPI007	*J1308 17								
SPI008	*J1211 36								
SPI009	*J1211 38								
SPI010	*J1211 53								
SPI011	*J1211 51								
SPI012	*J1222 08								
SPI013	*J1222 10								
SPI014	*J1222 05								
SPI015	*J1222 07								
SPI016	*J1222 09								
SPI017	*J1222 20								
SPI018	*J1222 26			J1118 50		FO5203			
SPI019	*J1222 24								
SPI020	*J1222 17								
SPI021	*J1222 19								
SPI022	*J1222 36			J1118 47		FO5203			
SPI023	*J1308 46								
SPI024	*J1222 23			J1218 05		FO5201			

Table 5-6. Left Hand Assembly Key Signal Lookup-Continued

Signal	Distribution											
SPI025	*J1222	25										
SPI026	*J1222	29										
SPI027	*J1308	48										
SPI028	*J1308	52										
SPI029	*J1222	35										
SPI030	*J1222	37										
SPI031	*J1308	47										
SPI032	*J1308	25										
SPI033	*J1308	42										
SPI034	*J1308	45										
SPI035	*J1308	51										
SPI036	*J1308	08										
SPI037	*J1211	71										
SPI038	*J1308	26										
SPI039	*J1308	38										
SPI040	*J1308	39										
SPI041	*J1308	41										
SPI042	*J1211	72										
SPI043	*J1211	73										
SPI044	*J1211	76										
SPI045	*J1211	78										
SPI046	*J1308	10										
SPI047	*J1308	29										
SPI048	*J1308	35										
SPI049	*J1308	36										
VTESTD4	J04	38		FO3500	J1222	41		FO3500				
XJCMSG	J01	38		FO4801	*J1137	40	07B	FO4801				
XJCMSH	J01	37		FO4801	*J1137	38	06B	FO4801				
XJCMST	J1119	43	23B	FO5300	J1131	26	14A	FO5100	J1132	05	03B	FO4801
	*J1137	07	05B	FO4801								
XJENSG	J01	36		FO4801	*J1138	36	13B	FO4801				
XJENSH	J01	35		FO4801	*J1138	34	12B	FO4801				
XJENST	J1119	41	22B	FO5300	J1132	41	22B	FO5100	J1133	26	14A	FO4801
	J1135	79	39B	FO5002	*J1138	11	11B	FO4801				
XJINCG	J01	40		FO4801	*J1137	36	13B	FO4801				
XJINCH	J01	39		FO4801	*J1137	34	12B	FO4801				

Table 5-6. Left Hand Assembly Key Signal Lookup-Continued

Signal	Distribution										
XJ0PCG	J01	02		FO4801	*J1142	40	07B	FO4801			
XJ0PCH	J01	01		FO4801	*J1142	38	06B	FO4801			
XJ0PCT	J1118	18	10A	FO4900	J1119	08	06A	FO4700	J1131 57	30B	FO5100
	J1135	10	07A	FO4801	*J1142	07	05B	FO4801			
XJ00CG	J01	04		FO4801	*J1142	36	13B	FO4801			
XJ00CH	J01	03		FO4801	*J1142	34	12B	FO4801			
XJ00CT	J1123	51	25B	FO4700	J1129	03	03B	FO4801	J1132 54	25A	FO5100
	J1135	26	14A	FO4801	*J1142	11	11B	FO4801			
XJ001CG	J01	06		FO4801	*J1141	40	07B	FO4801			
XJ01CH	J01	05		FO4801	*J1141	38	06B	FO4801			
XJ01CT	J1123	57	29B	FO4700	J1129	01	02B	FO4801	J1135 05	03B	FO4801
	*J1141	07	05B	FO4801							
XJ02CG	J01	08		FO4801	*J1141	36	13B	FO4801			
XJ02CH	J01	07		FO4801	*J1141	34	12B	FO4801			
XJ02CT	J1123	54	26A	FO4700	J1129	04	02A	FO4801	J1135 20	1A	FO4801
	*J1141	11	11B	FO4801							
XJ03CG	J01	10		FO4801	*J1140	40	07B	FO4801			
XJ03CH	J01	09		FO4801	*J1140	38	06B	FO4801			
XJ03CT	J1123	62	29A	FO4700	J1126	71	33B	FO5100	J1129 06	03A	FO4801
	J1135	07	03A	FO4801	*J1140	07	05B	FO4801			
XJ04CG	J01	12		FO4801	*J1140	36	13B	FO4801			
XJ04CH	J01	11		FO4801	*J1140	34	12B	FO4801			
XJ04CT	J1123	69	32A	FO4700	J1126	73	34B	FO5100	J1129 17	09B	FO4801
	J1135	19	09B	FO4801	*J1140	11	11B	FO4801			
XJ05CG	J01	14		FO4801	*J1139	40	07B	FO4801			
XJ05CH	J01	13		FO4801	*J1139	38	06B	FO4801			
XJ05CT	J1123	75	35B	FO4700	J1129	15	08B	FO4801	J1130 22	12A	FO5100
	J1135	13	06B	FO4801	*J1139	07	05B	FO4801			
XJ06CG	J01	16		FO4801	*J1139	36	13B	FO4801			
XJ06CH	J01	15		FO4801	*J1139	34	12B	FO4801			
XJ06CT	J1123	70	34A	FO4700	J1126	75	35B	FO5100	J1129 18	09A	FO4801
	J1135	25	12B	FO4801	*J1139	11	IB	FO4801			
XJ07CG	J01	18		FO4801	*J1138	40	07B	FO4801			
XJ07CH	J01	17		FO4801	*J1138	38	06B	FO4801			
XJ07CT	J1123	76	37A	FO4700	J1126	77	36B	FO5100	J1129 20	10A	FO4801
	J132	10	07A	FO4801	*J1138	07	05B	FO4801			

Table 5-6. Left Hand Assembly Key Signal Lookup-Continued

Signal	Distribution					
5VPULL	J1303 48	FO4402	J1303 51	FO4402	J1303 54	FO4402
	J1305 48	FO4402	J1305 51	FO4402	J1305 54	FO4402
	J1306 48	FO4402	J1306 51	FO4402	J1306 54	FO4402
	J1308 63	FO4402				

Table 5-7. Center Section Key Signal Lookup

Signal	Distribution					
CCCCRA	J1125 30	FO3803	*J1126 62	FO3802		
CCCDRA	J1124 24	FO3803	J1124 68	FO3803	*J1126 42	FO3802
CCCHEA	J110 16	FO3702	*J1126 73	FO3802		
CCCHE0	*J1126 35	FO3802	J1127 35	FO3802		
CCCVEA	*J1125 70	FO3803	J1129 18	FO3902		
CCDAXE	J1119 60	FO4002	*J1124 40	FO3803		
CCDAXW	J1119 56	FO4002	*J1124 42	FO3803		
CCDAYN	J1121 60	FO4002	*J1124 78	FO3803		
CCDAYS	J1121 56	FO4002	*J1124 80	FO3803		
CCDDZA	J1125 80	FO3803	*J1126 50	FO3802		
CCDR1A	J1125 38	FO3803	*J1126 59	FO3802		
CCDR2A	J1125 34	FO3803	*J1126 74	FO3802		
CCREC0	*J1126 68	FO3802	*J1127 68	FO3802		
CCRE3A	*J1126 23	FO3802	J1127 22	FO3802		
CCRE4A	*J1126 24	FO3802	J1127 30	FO3802		
CCRMCA	J1110 36	FO3703	*J1125 48	FO3803	J1126 55	FO3802
	J1127 55	FO3802				
CCRSX0	J1125 14	FO3803	*J1126 38	FO3802	*J1127 38	FO3802
CCRSY0	J1125 78	FO3803	*J1126 70	FO3802	*J1127 70	FO3802
CCRX10	*J1126 47	FO3802	*J1127 47	FO3802		
CCRX20	*J1126 49	FO3802	*J1127 49	FO3802		
CCRY10	*J1126 33	FO3802	*J1127 33	FO3802		
CCRY20	*J1126 29	FO3802	*J1127 29	FO3802		
CCRZA0	*J1126 52	FO3802	*J1127 52	FO3802		
CCST0A	*J1125 04	FO3803	J1126 78	FO5203		
CCTBD0	J02 14	FO5203	*J1126 66	FO5203		
CCXCC0	J1124 22	FO3803	*J1125 26	FO3803		
CCXE1A	J1125 20	FO3803	*J1126 64	FO3802		
CCXE2A	J1125 19	FO3803	*J1126 56	FO3802		
CCXE3A	J1125 13	FO3803	*J1126 63	FO3802		
CCXSNA	J1124 14	FO3803	*J1125 10	FO3803		
CCXSN0	J1124 18	FO3803	*J1125 06	FO3803	J1126 72	FO5203
CCYCC0	J1124 66	FO3803	*J1125 62	FO3803		
CCYE1A	J1125 72	FO3803	*J1126 65	FO3802		
CCYE2A	J1125 71	FO3803	*J1126 60	FO3802		
CCYE3A	J1125 77	FO3803	*J1126 61	FO3802		

Table 5-7. Center Section Key Signal Lookup - Continued

Signal	Distribution								
CCYSNA	J1124	62	FO3803	*J1125	75	FO3803			
CCYSN0	J1124	64	FO3803	*J1125	74	FO3803	J1126	69	FO5203
CCZAD0	*J1125	66	FO3803	*J1126	54	FO3803			
CDFLAA	*J01	40	FO2501	*P01	17	FO4002			
CDTBA0	J02	15	FO5203	*J1123	42	FO5203			
CDXSN0	*J1110	21	FO3702	J1113	25	FO3702			
CDXTST	J1123	26	FO5204	*P01	11	FO4002			
CDYSN0	*J1110	24	FO3702	J1113	55	FO3702			
CDYTST	J1123	24	FO5204	*P01	13	FO4001			
CFSRFN	*MTI	06	FO4501	MTI	08	FO4501	J01	41	FO4501
	J1109	03	FO4501	P03	41	FO4501			
CFSRFP	*MTI	01	FO4501	MT1	03	FO4501	J01	42	FO4501
	J1109	05	FO4501	P03	42	FO4501			
CFSX0V	*MTI	04	FO4501	MTI	07	FO4501	J01	46	FO4501
	J1109	35	FO4501	P03	46	FO4501			
CFSY0V	*MT1	02	FO4501	MTI	05	FO4501	J01	47	FO4501
	J1109	39	FO4501	P03	47	FO4501			
CHACTK	J1110	15	FO3702	*J1110	17	FO3702			
CLCVC0	*J1112	19	FO5401	J1123	47	FO4001	J1125	54	FO3802
	J1127	56	FO3701						
CLCVD0	*J1112	23	FO5401	J1129	21	FO3902			
CLDAXE	*J 1116	78	FO3704	J1119	52	FO4002			
CLDAXW	*J 1116	68	FO3704	J1119	54	FO4002			
CLDAX0	*J1114	72	FO3703	J1116	66	FO3704			
CLDAYN	*J1117	78	FO3704	J1121	52	FO4002			
CLDAYS	*J1117	68	FO3704	J1121	54	FO4002			
CLDAY0	*J1115	72	FO3704	J1117	66	FO3704			
CLDBX0	J1113	50	FO3702	*J1114	10	FO3703			
CLDBY0	J1113	51	FO3702	*J1115	10	FO3704			
CLDCX0	J1113	48	FO3702	*J1114	54	FO3703			
CLDCY0	J1113	49	FO3702	*J1115	54	FO3704			
CLDDCAS	J1110	03	FO3702	*J1112	14	FO5401	J1116	46	FO3704
	J1117	46	FO3704						
CLDDX0	J1113	43	FO3702	*J1114	56	FO3703			
CLDDY0	J1113	47	FO3702	*J1115	56	FO3704			
CLDOX0	*J1114	41	FO3703	J1116	11	FO3704			

Table 5-7. Center Section Key Signal Lookup - Continued

Signal			Distribution				
CLD0Y0	*J1115	41	FO3704	J1117 11	FO3704		
CLD1X0	*J1114	61	FO3703	J1116 21	FO3704		
CLD1Y0	*J1115	61	FO3704	J1117 21	FO3704		
CLD2X0	*J1114	46	FO3703	J1116 23	FO3704		
CLD2Y0	*J1115	46	FO3704	J1117 23	FO3704		
CLD3X0	*J1114	23	FO3703	J1116 30	FO3704		
CLD3Y0	*J1115	23	FO3704	J1117 30	FO3704		
CLD4X0	*J1114	26	FO3703	J1116 34	FO3704		
CLD4Y0	*J1115	26	FO3704	J1117 34	FO3704		
CLD5X0	*J1114	25	FO3703	J1116 50	FO3704		
CLD5Y0	*J1115	25	FO3704	J1117 50	FO3704		
CLD6X0	*J1114	30	FO3703	J1116 52	FO3704		
CLD6Y0	*J1115	30	FO3704	J1117 52	FO3704		
CLD7X0	*J1114	68	FO3703	J1116 60	FO3704		
CLD7Y0	*J1115	68	FO3704	J1117 60	FO3704		
CLD8X0	*J1114	69	FO3703	J1116 62	FO3704		
CLD8Y0	*J1115	69	FO3704	J1117 62	FO3704		
CLD9X0	*J1114	70	FO3703	J1116 64	FO3704		
CLD9Y0	*J1115	70	FO3704	J1117 64	FO3704		
CLLDXA	J1110	06	FO3702	*J1112 74	FO3701	J1127 74	FO3701
CLLDYA	J1110	14	FO3702	*J1112 76	FO3701		
CLLE4A	*J1113	46	FO3703	J1129 04	FO3902	J1129 06	FO3902
CLLGEA	*J1112	78	FO3701	J1113 13	FO3702		
CLLNAA	J01	38	FO2501	*J1115 16	FO3704		
CLLNA0	*J1113	79	FO3703	J1115 18	FO3704	J1115 20	FO3704
CLLNC0	*J1112	04	FO3701	J1113 64	FO3702		
CLLSAA	*J1112	06	FO3701	J1113 76	FO3702		
CLPEXA	*J1112	54	FO3701	J1114 21	FO3703	J1127 64	FO3701
CLPEYA	*J1112	56	FO3701	J1115 21	FO3704	J1123 48	FO4001
CLRXC0	*J1113	09	FO3703	J1114 06	FO3703		
CLRYCO	*J1113	77	FO3703	J1115 06	FO3704		
CLR120	*J1112	59	FO3701	J1114 01	FO3703	J1115 01	FO3704
CLR130	*J1112	61	FO3701	J1114 02	FO3703	J1115 02	FO3704
CLR140	*J1112	73	FO3701	J1114 13	FO3703	J1115 13	FO3704
CLR15A	J1114	07	FO3703	*J1114 16	FO3703	J1115 07	FO3704
CLR150	*J1112	75	FO3701	J1114 18	FO3703	J1114 20	FO3703

Table 5-7. Center Section Key Signal Lookup - Continued

Signal			Distribution					
CLSACA	J01	37	FO2501	*J1112	01	FO3701		
CLSAC0	*J1112	11	FO3701	J1114	14	FO3703	J1115 14	FO3704
CLSC1A	J01	73	FO5401	*J1112	22	FO5401		
CLSC2A	J01	77	FO5401	*J1112	34	FO5401		
CLSNX0	*J1113	26	FO3703	J1114	08	FO3703		
CLSNY0	*J1113	57	FO3703	J1115	08	FO3704		
CLSVEA	*J1113	37	FO3703	J1129	22	FO3902		
CLSXC0	*J1114	05	FO3703	J1114	66	FO3703		
CLSYCO	*J1115	05	FO3704	J1115	66	FO3704		
CLSOLA	*J1112	72	FO3701	J1113	78	FO3702		
CLTBX0	J02	12	FO5203	*J1114	71	FO5203		
CLTBY0	J02	13	FO5203	*J1115	71	FO5203		
CLTCCA	J01	75	FO5401	*J1112	20	FO5401		
CLTDXA	*J1110	09	FO3702	J1113	42	FO3702		
CLTDYA	*J1110	11	FO3702	J1113	60	FO3702		
CLVDC0	*J1113	80	FO3703	J1129	15	FO3902		
CLXDAT	*J1116	80	FO3704	J1123	06	FO5204		
CLXLCA	*J1112	05	FO3701	J1114	24	FO3703		
CLYDAT	*J1117	80	FO3704	J1123	04	FO5204		
CLYLCA	*J1112	03	FO3701	J1115	24	FO3704		
CL0SE0	*J01	52	FO5401	J1101	62	FO5401	J1112 21	FO5401
CRMCXA	J1110	60	FO3702	*J1114	42	FO3703		
CRMCYA	J1110	62	FO3702	*J1115	42	FO3704		
CSAR0A	J1121	80	FO4002	*J1123	37	FO4001		
CSAR00	J1121	77	FO4002	*J1123	38	FO4001		
CSHKMA	J1119	75	FO4002	J1121	75	FO4002	*J1123 43	FO4001
CSHKM0	J1119	74	FO4002	J1121	74	FO4002	*J1123 41	FO4001
CSLCXP	J119	62	FO4002	*J1123	80	FO4001		
CSLCX0	*J1110	61	FO3702	J1116	40	FO3704	J1116 42	FO3704
CSLCYP	J1121	62	FO4001	*J1123	70	FO4001		
CSLCY0	*J1110	63	FO3702	J1117	40	FO3704	J1117 42	FO3704
CSLXRP	J1119	66	FO4002	*J1123	53	FO4001		
CSLYRP	*J1121	66	FO4002	*J1123	55	FO4001		
CSSA0E	*J1119	14	FO4002	P01	01	FO4002		
CSSA0N	*J1121	14	FO4002	P01	06	FO4002		
CSSA0S	*J1121	26	FO4002	J1123	56	FO4001	J1123 60	FO4001

Table 5-7. Center Section Key Signal Lookup - Continued

Signal	Distribution								
	J1123	79	FO4001	P01	08	FO4002			
CSSA0W	*J1119	26	FO4002	J1123	66	FO4001	J1123	68	FO4001
	J1123	77	FO4001	P01	03	FO4002			
CSTABA	J1110	07	FO3702	*J1112	69	FO3701			
CSTBX0	*J1119	10	FO4002	J1123	23	FO5204			
CSTBY0	*J1121	10	FO4002	J 1123	14	FO5204			
CSWLNA	J1112	08	FO5401	*J1113	62	FO3703			
CSWLN0	J1110	59	FO3702	*J1113	65	FO3703			
CS14XR	J1119	72	FO4002	J1119	77	FO4002	J1119	80	FO4002
CS14YR	J1121	72	FO4002	J1121	78	FO4002	J1121	79	FO4002
CTACTA	J01	39	FO2501	*J1110	05	FO3702			
CTCPX0	*J1110	79	FO3702	J1114	19	FO3703			
CTCPY0	*J1 110	78	FO3702	J1115	19	FO3704			
CTTSWA	*SI 2A		FO4401	J01	45	FO4401			
CTTSWB	*SI 4A		FO4401	J01	46	FO4401			
CVATBP	J1123	54	FO5204	*J1129	34	FO3902			
CVDEN0	J1129	07	FO3902	J1129	38	FO3902			
CVSRC0	J1129	65	FO3902	J1129	72	FO3902			
CVVA0P	*J1132	79	FO3902	*J1132	80	FO3902	P02	06	FO3902
CVVMOM	*J1129	01	FO3902	J1132	03	FO3902	J1132	04	FO3902
DDREQG	J02	78	FO5002	*J1107	36	FO5002			
DDREQH	J02	77	FO5002	*J1107	34	FO5002			
DDSNCH	*J02	69	FO0101	J1106	34	FO0101			
DDSNCT	J02	75	FO0101	*J1106	11	FO0101			
DD0PCH	*J02	25	FO0101	J1102	38	FO0101			
DD0PCT	J02	27	FO0101	*J1102	07	FO0101			
DD0URG	J02	74	FO5002	*J1107	40	FO5002			
DD0URH	J02	73	FO5002	*J1107	38	FO5002			
DD00CH	*J02	31	FO0101	J1102	34	FO0101			
DD00CT	J02	34	FO0101	*J1102	11	FO0101			
DD01CH	*J02	35	FO0101	*J1103	38	FO0101			
DD01CT	J02	37	FO0101	*J1103	07	FO0101			
DD02CH	*J02	38	FO0101	J1103	34	FO0101			
DD02CT	J02	40	FO0101	*J1103	11	FO0101			
DD03CH	*J02	51	FO0101	J1104	38	FO0101			
DD03CT	J02	45	FO0101	*J1104	07	FO0101			

Table 5-7. Center Section Key Signal Lookup - Continued

Signal	Distribution						
DD04CH	*J02	55	FO0011	J1104 34	FO0101		
DD04CT	J02	57	FO0101	*J1104 11	FO0101		
DD05CH	*J02	58	FO0101	J1105 38	FO0101		
DD05CT	J02	60	FO0101	*J1105 07	FO0101		
DD06CH	*J02	62	FO0101	J1105 34	FO0101		
DD06CT	J02	61	FO0101	*J1105 11	FO0101		
DD07CH	*J02	65	FO0101	J1106 38	FO0101		
DD07CT	J02	67	FO0101	*J1106 07	FO0101		
KH000D4	*J01	01	FO2000	J1101 08	FO2000	J1110 30	FO3702
	J1112	24	FO3701	J1114 22	FO3703	J1115 22	FO3704
	J1127	63	FO3701	J1129 40	FO3902		
KH001D4	*J01	02	FO2000	J1101 10	FO2000	J1110 31	FO3702
	J1112	25	FO3701	J1113 01	FO3702	J111409	FO3703
	J1115	09	FO3704	J1129 43	FO3902		
KH002D4	*J01	03	FO2000	J1101 05	FO2000	J1110 32	FO3702
	J1112	26	FO3701	J1113 03	FO3702	J1114 64	FO3703
	J1115	64	FO3704	J1129 46	FO3902		
KH003D4	*J01	04	FO2000	J1101 07	FO2000	J1110 34	FO3702
	J1112	27	FO3701	J1113 07	FO3702	J1113 10	FO3702
	J1113	69	FO3702	J1114 32	FO3703	J1115 32	FO3704
	J1129	48	FO3902				
KH004D4	*J01	05	FO2000	J1101 09	FO2000	J1110 22	FO3702
	J1112	36	FO3701	J1113 04	FO3702	J1113 08	FO3702
	J1113	75	FO3702	J1114 34	FO3703	J1115 34	FO3704
	J1129	47	FO3902				
KH005D4	*J01	06	FO2000	J1101 20	FO2000	J111238	FO3701
	J1113	14	FO3702	J1113 30	FO3702	J1113 73	FO3702
	J1114	36	FO3703	J1115 36	FO3704	J1129 60	FO3902
KH006D4	*J01	07	FO2000	J1101 26	FO2000	J1112 40	FO3701
	J1113	11	FO3702	J1113 29	FO3702	J1113 71	FO3702
	J1114	38	FO3703	J1115 38	FO3704	J1129 59	FO3902
KH007D4	*J01	08	FO2000	J1101 24	FO2000	J1112 42	FO3701
	J1113	33	FO3702	J1113 34	FO3702	J1113 68	FO3702
	J1114	74	FO3703	J1115 74	FO3704	J1125 22	FO3803
	J1129	62	FO3902				
KH008D4	*J0	09	FO2000	J1101 17	FO2000	J1110 49	FO3702

Table 5-7. Center Section Key Signal Lookup - Continued

Signal	Distribution						
	J1112	46	FO3701	J1113 36	FO3702	J1113 66	FO3702
	J1113	74	FO3702	J1114 76	FO3703	J1115 76	FO3704
	J1126	09	FO3802	J1127 09	FO3802	J1129 61	FO3902
KH009D4	*J01	10	FO2000	J1101 19	FO2000	J1110 50	FO3702
	J1112	48	FO3701	J1113 06	FO3702	J1113 38	FO3702
	J1113	72	FO3702	J1114 80	FO3703	J1115 80	FO3704
	J1126	10	FO3802	J1127 10	FO3802	J1129 33	FO3902
KH010D4	*J01	11	FO2000	J1101 36	FO2000	J1110 51	FO3702
	J1112	50	FO3701	J1113 05	FO3702	J1113 35	FO3702
	J1113	70	FO3702	J1114 78	FO3703	J1115 78	FO3704
	J1126	04	FO3802	J1127 04	FO3802	J1129 29	FO3902
KH011D4	*J01	12	FO2000	J1101 38	FO2000	J1110 52	FO3702
	J1112	52	FO3701	J1113 20	FO3702	J1113 53	FO3702
	J1113	54	FO3702	J1114 62	FO3703	J1115 62	FO3704
	J1126	03	FO3802	J1127 03	FO3802	J1129 30	FO3902
KH012D4	*J01	13	FO2000	J1101 23	FO2000	J1110 20	FO3702
	J1112	60	FO3701	J1113 18	FO3702	J1113 56	FO3702
	J1114	63	FO3703	J1115 63	FO3704	J1126 06	FO3802
	J1127	06	FO3802	J1129 74	FO3902		
KH013D4	*J01	14	FO2000	J1101 25	FO2000	J1112 62	FO3701
	J1113	27	FO3702	J1113 59	FO3702	J1114 65	FO3703
	J1115	65	FO3704	J1126 07	FO3802	J1127 07	FO3802
	J1129	71	FO3902				
KH014D4	*J01	15	FO2000	J1101 29	FO2000	J1110 23	FO3702
	J1112	64	FO3701	J1123 33	FO4001	J1126 25	FO3802
	J1129	68	FO3902				
KH015D4	*J01	16	FO2000	J1101 42	FO2000	J1112 66	FO3701
	J1123	34	FO4001	J1129 70	FO3902		
KLV1D0	*J01	31	FO2000	J1129 37	FO3902	J1129 79	FO3902
KL000D4	*J01	19	FO2200	J1101 46	FO2200	J1112 80	FO3701
KL001D4	*J01	21	FO2200	J1101 35	FO2200	J1112 79	FO3701
KL002D4	*J01	25	FO2200	J1101 37	FO2200	J1112 68	FO3701
KL003D4	*J01	27	FO2200	J1101 39	FO2200	J1101 52	FO2200
	P01	15	FO4002				
KL004D4	*J01	28	FO2200	J1101 41	FO2200	J1112 71	FO3701
KL005D4	*J01	30	FO2200	J1101 53	FO2200	J1110 80	FO3702

Table 5-7. Center Section Key Signal Lookup - Continued

Signal	Distribution						
KL007D4	*J01	33	FO2200	J1101 47	FO2200	J1124 70	FO3803
	J1126	37	FO3802	J1126 57	FO3802		
KL008D4	*J01	34	FO2200	J1101 45	FO2200	J1101 55	FO2200
	J1126	51	FO3802				
KL009D4	*J01	36	FO2200	J1101 51	FO2200	J111270	FO3701
LDRST0	*J02	72	FO5002				
	J1107	01	FO5002				
LESC10	*J02	01	FO5203	J1114 48	FO5203	J1115 48	FO5204
	J1123	18	FO5203	J1126 77	FO5203		
LESC20	*J02	02	FO5203	J1114 50	FO5203	J1115 50	FO5203
	J1123	27	FO5203	J1126 75	FO5203		
LESC40	*J02	03	FO5203	J1114 52	FO5203	J1115 52	FO5203
	J1123	25	FO5203	J1126 71	FO5203		
LFSTVS	*J01	50	FO4501	J1109 61	FO4501		
LMDSTAV	*J02	76	FO5002				
	J1107	08	FO5002				
LWDDE0T	*J02	08	FO5203	J1114 59	FO5203		
LWDDE1T	*J02	09	FO5203	J1114 60	FO5203		
LWDDE2T	*J02	06	FO5203	J1126 79	FO5203		
LWDDE3T	*J02	07	FO5203	J1126 80	FO5203		
LWDDE4T	*J02	10	FO5203	J1115 59	FO5203		
LWDDE5T	*J02	11	FO5203	J1115 60	FO5203		
LWDDE6T	*J02	04	FO5203	J1123 20	FO5203		
LWDDE7T	*J02	05	FO5203	J1123 30	FO5203		
RCPXAA	J01	45	FO4501	*J1109 19	FO4501		
RCPYAA	J01	51	FO4501	*J1109 63	FO4501		
RDNDX0	J01	43	FO4501	*J1109 13	FO4501		
RDNDY0	J01	48	FO4501	*J1109 49	FO4501		
RSFRUS	*J01	62	FO3902	J1129 52	FO3902		
RSHOOK	*J01	68	FO3902	J1129 63	FO3902		
RSMAP1	*J01	64	FO3902	J1129 50	FO3902		
RSMAP2	*J01	65	FO3902	J1129 56	FO3902		
RSPRLN	*J01	63	FO3902	J1129 49	FO3902		
RSSWVD	*J01	69	FO3902	J1129 64	FO3902		
RSTRKS	*J01	61	FO3902	J1129 42	FO3902		
RSOTHR	*J01	66	FO3902	J1129 54	FO3902		

Table 5-7. Center Section Key Signal Lookup - Continued

Signal			Distribution					
RUPDX0	J01	44	FO4501	*J1109	15	FO4501		
RUPDY0	J01	49	FO4501	*J1109	55	FO4501		
RVAR00	J01	17	FO4501	TB1	01	FO4501	*R2 G0	FO4501
RVAR10	J01	18	FO4501	TB1	02	FO4501	*R2 G1	FO4501
RVAR20	J01	19	FO4501	TB1	03	FO4501	*R2 G2	FO4501
RVAR30	J01	20	FO4501	TBI	04	FO4501	*R2 G3	FO4501
RVAR40	J01	21	FO4501	TBI	05	FO4501	*R2 G4	FO4501
RVAR50	J01	22	FO4501	TB1	06	FO4501	*R2 G5	FO4501
RVAR60	J01	23	FO4501	TB1	07	FO4501	*R2 G6	FO4501
RVAR70	J01	24	FO4501	TB1	08	FO4501	*R2 G7	FO4501
SWPC0MP	*J1127	66	FO3701	J1129	41	FO3902		
VRLVT0	*J01	55	FO3701	J1112	18	FO3701	J1113 40	FO3702
VOD2100L	*J01	57	FO3902	J1101	61	FO3902	J1129 03	FO3902
VOD220L	*J01	58	FO3902	J1101	72	FO3902	J1129 10	FO3902
VOD230L	*J01	60	FO3902	J1101	78	FO3902	J1129 13	FO3902

Table 5-8. Right Hand Assembly Key Signal Lookup

Signal				Distribution								
AALR131A	*J03	03		FO3001	J1120	78	38A	FO3001				
AALR132A	*J03	04		FO3001	J1120	72	35A	FO3001				
AALR133A	*J03	05		FO3001	J1120	77	36B	FO3001				
AALR134A	*J03	06		FO3001	J1120	71	33B	FO3001				
AALR231A	*J03	07		FO3001	J1119	64	30A	FO3001				
AALR232A	*J03	08		FO3001	J1119	56	28B	FO3001				
AALR233A	*J03	09		FO3001	J1119	59	30B	FO3001				
AALR234A	*J03	10		FO3001	J1119	53	26B	FO3001				
AALR331A	*J03	11		FO3001	J1119	78	38A	FO3001				
AALR332A	*J03	12		FO3001	J1119	72	35A	FO3001				
AALR333A	*J03	13		FO3001	J1119	77	36B	FO3001				
AALR334A	*J03	14		FO3001	J1119	71	33B	FO3001				
AALR432A	*J03	16		FO3001	J1118	72	35A	FO3001				
AALR433A	*J03	17		FO3001	J1118	77	36B	FO3001				
AALR434A	*J03	15		FO3001	J1118	71	33B	FO3001				
AH0RDA	*J03	01		FO0000	J1230	22	14A	FO2800				
AH0RD0V	*J1230	24	13A	FO2800	J1220	21	11B	FO2800				
AH0150V	*J03	18		FO3001	J1118	78	38A	FO3001				
ALCMDD	*J03	19		FO4200	J1127	23	11B	FO4200	J1131	42		FO4200
	J1133	06	05A	FO4200	J1134	08	06A	FO4200				
ALENAD	*J03	21		FO4200	J1131	29		FO4200	J1133	22	14A	FO4200
ALINDB4	*J1232	69	35A	FO4200	J03	43		FO4200				
ALI00B	*J1132	69	35A	FO4600	J03	23		FO0500	J1133	76	37A	FO4600
ALI01B	*J1132	38	18A	FO4600	J03	24		FO0500	J1133	74	35A	FO4600
ALI02B	*J1132	30	15A	FO4600	J03	25		FO0500	J1133	69	35B	FO4600
ALI03B	*J1132	33	16B	FO4600	J03	26		FO0500	J1133	73	37B	FO4600
ALI04B	*J1132	39	19B	FO4600	J03	27		FO0500	J1133	79	39B	FO4600
ALI05B	*J1132	52	24A	FO4600	J03	28		FO0500	J1133	65	33B	FO4600
ALI06B	*J1132	46	21A	FO4600	J03	29		FO0500	J1133	59	31B	FO4600
ALI07B	*J1132	45	24B	FO4600	J03	30		FO0500	J1133	55	29B	FO4600
ALI08B	*J1132	51	27B	FO4600	J03	31		FO0500	J1133	62	29A	FO4600
ALI09B	*J1132	66	31A	FO4600	J03	32		FO0500	J1133	61	31A	FO4600
ALI10B	*J1132	60	28A	FO4600	J03	33		FO0500	J1133	64	33A	FO4600
ALI11B	*J1132	57	30B	FO4600	J03	34		FO0500	J1130	30	15A	FO4102
	J1133	51	27B	FO4600								
ALI12B	*J1132	63	33B	FO4600	J03	35		00500	J1130	34	16A	FO4102

Table 5-8. Right Hand Assembly Key Signal Lookup - Continued

Signal	Distribution									
	J1133 45	25B	FO4600							
ALI13B	*J1132 75	37B	FO4600	J03 36			FO0500	J1129 40	19A	FO4102
	J1133 41	23B	FO4600							
ALI14B	*J1132 72	34A	FO4600	J03 37			FO0500	J1133 50	22A	FO4600
ALI15B	*J1132 80	39A	FO4600	J03 38			FO0500	J1133 75	39A	FO4600
AMRSTAV	*J05 60		FO5300	J1230 73		37B	FO5300			
A5SQF0	*J03 39		FO5403	J1225 59		31B	FO5403	J1230 55	29B	FO5403
A5SQT0	*J03 41		FO5403	J1212 53		26A	FO5403	J1212 60	29A	FO5403
	J1225 79	39B	FO5403	J1229 29		14B	FO2800			
CCCHEA4	*J02 23		FO2501	J1217 69		34B	FO2501			
CLLNAA4	*J02 18		FO2501	J1217 70		34A	FO2501			
CLSACA4	*J02 17		FO2501	J1217 72		35A	FO2501			
CLSC1A4	*J02 59		FO5403	J1224 41		22B	FO5403	J1228 68	32A	FO5403
	J1231 45		FO5403							
CLTCCA	*J02 66		FO5403	J1106 11		05B	FO3601	J1112 17	08B	FO5403
	J1222 36	17A	FO5403	J1222 37		18B	FO3601	J1222 50	23A	FO5403
KACLD0	*J1224 09	04B	FO2601	J1319 06			FO1602	J1320 06		FO1602
	J1321 06		FO1603	J1322 06			FO1604			
KAC12AV	*J1230 57	30B	FO1604	J1223 48		22A	FO1604			
KAC13AV	*J1230 49	23A	FO1604	J1223 43		23B	FO1604	J1223 68	32A	FO2602
KADUX0	*J1102 69	35A	FO2400	J1225 07		03A	FO2400			
KADVCA	*J1225 09	04B	FO2400	J1128 49		26B	FO2400	J1228 11	05B	FO2400
	J1233 56	26A	FO1901							
KADVC0	*J1228 15	07B	FO2400	J1128 41		22B	FO1902	J1130 78	38A	FO2300
	J1217 14	06A	FO1902	J1217 26		13A	FO1902	J1217 40	19A	FO1902
	J1217 54	25A	FO1902	J1218 14		09A	FO2400	J1218 24	13A	FO2400
	J1220 45	24B	FO2300	J1220 54		25A	FO2300	J1220 59	30B	FO2300
	J1220 66	32A	FO2300							
KAFCIO	J1117 35		FO1601	J1118 43		22B	FO5203	*J1317 05		FO1601
	J1319 70		FO1602	J1320 70			FO1602	J1321 70		FO1603
	J1322 70		FO1604							
KAFCOA	J1118 45	23B	FO5203	*J1317 03			FO1601	J1317 20		FO1604
	J1319 69		FO1602							
KAFSOA	J1117 37		FO1601	J1118 35		16B	FO5203	*J1317 14		FO1601
	J1319 56		FO1602	J1320 56			FO1602	J1321 56		FO1603
	J1322 56		FO1604							

Table 5-8. Right Hand Assembly Key Signal Lookup - Continued

Signal	Distribution								
KAFS1A	J1118 37	17B	FO5203	*J1317 04		FO1601	J1319 66		FO1602
	J1320 66		FO1602	J1321 66		FO1603	J1322 66		FO1604
KAFS2A	J1118 39	18B	FO5203	*J1317 02		FO1601	J1319 65		FO1602
	J1320 65		FO1602	J1321 65		FO1603	J1322 65		FO1604
KAFS3A	J1118 41	19B	FO5203	*J1317 01		FO1601	J1319 68		FO1602
	J1320 68		FO1602	J1321 68		FO1603	J1322 68		FO1604
KAFT1A	*J1233 76	37A	FO2602	J1102 71	36A	FO2400			
KAF1C0	*J1111 76	37A	FO2601	J1233 72	34A	FO2602			
KAF2UA	*J1224 38	18A	FO2400	J1102 73	36B	FO2400			
KALR101A	*J1319 01		FO1602						
KALR102A	*J1319 03		FO1602						
KALR103A	*J1319 17		FO1602						
KALR104A	*J1319 20		FO1602	J1320 02		FO1602			
KALR111A	*J1319 21		FO1801	J1214 45	23B	FO1901	J1314 62	29A	FO2200
	J1318 56		FO1701	J1329 33		FO1702	J1330 33		FO1702
KALR112A	*J1319 36		FO1801	J1214 43	22B	FO1901	J1314 54	26A	FO2200
	J1318 53		FO1701	J1329 34		FO1702	J1330 34		FO1702
KALR113A	*J1319 45		FO1801	J1214 41	19B	FO1901	J1314 57	29B	FO2200
	J1318 64		FO1701	J1329 32		FO1702	J1330 32		FO1702
KALR114A	*J1319 37		FO1801	J1214 39	18B	FO1901	J1314 51	25B	FO2200
	J1318 47		FO1701	J1329 25		FO1702	J1330 25		FO1702
KALR121A	*J1319 32		FO1602						
KALR122A	*J1319 31		FO1602						
KALR123A	*J1319 48		FO1602						
KALR124A	*J1319 47		FO1602	J1320 39		FO1602			
KALR131A	*J1319 40		FO2000	J1234 20	10A	FO2000			
KALR132A	*J1319 38		FO2000	J1234 23	12A	FO2000			
KALR133A	*J1319 22		FO2000	J1234 22	14A	FO2000			
KALR134A	*J1319 19		FO2000	J1234 15	07B	FO2000			
KALR141A	*J1319 55		FO1602	J1129 41	22B	FO1602			
KALR143A	*J1319 77		FO1602	J1317 66		FO1604			
KALR144A	*J1319 76		FO1602	J1317 65		FO1604			
KALR145A	J1319 75		FO1602						
KALR146A	*J1319 73		FO1602	J1317 55		FO1604	J1323 78		FO1602
KALR147A	*J1319 67		FO1601	J1227 10	07A	FO1604			
KALR201A	*J1320 01		FO1602						

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution							
KALR202A	*J1320 03	FO1602						
KALR203A	*J1320 17	FO1602						
KALR204A	*J1320 20	FO1602	J1321 02		FO1603			
KALR211A	*J1320 21	FO1802	J1213 59	30B	FO1901	J1318 39		FO1701
	J1329 43	FO1702	J1330 43		FO1702			
KALR212A	*J1320 36	FO1802	J1213 57	29B	FO1901	J1314 75	35B	FO220
	J1318 62	FO1701	J1329 39		FO1702	J1330 39		FO1702
KALR213A	*J1320 45	FO1802	J1213 55	27B	FO1901	J1318 30		FO1701
	J1329 42	FO1702	J1330 42		FO1702			
KALR214A	*J1320 37	FO1802	J1213 53	26B	FO1901	J1314 69	32A	FO2200
	J1318 29	FO1701	J1329 38		FO1702	J1330 38		FO1702
KALR221A	*J1320 32	FO1602						
KALR222A	*J1320 31	FO1602						
KALR223A	*J1320 48	FO1602						
KALR224A	*J1320 47	FO1602	J1321 39		FO1603			
KALR231A	*J1320 40	FO2000	J1234 38	20A	FO2000			
KALR232A	*J1320 38	FO2000	J1234 27	13B	FO2000			
KALR233A	*J1320 22	FO2000	J1234 21	11B	FO2000			
KALR234A	*J1320 19	FO2000	J1234 17	09B	FO2000			
KALR241A	*J1320 55	FO1602	J1129 43	23B	FO1602			
KALR243A	*J1320 77	FO1602	J1317 64		FO1604			
KALR244A	*J1320 76	FO1602	J1317 63		FO1604			
KALR245A	J1320 75	FO1602						
KALR246A	*J1320 73	FO1602	J1317 59		FO1604	J1323 76		FO1602
KALR247A	*J1320 67	FO1602	J1319 72		FO1602			
KALR301A	*J1321 01	FO1603						
KALR302A	*J1321 03	FO1603						
KALR303A	*J1321 17	FO1603						
KALR304A	*J1321 20	FO1603	J1322 02		FO1604			
KALR311A	*J1321 21	FO1802	J1214 77	36B	FO1901	J1329 53		FO1702
	J1330 53	FO1702						
KALR312A	*J1321 36	FO1802	J1214 75	35B	FO1901	J1329 52		FO1702
	J1330 52	FO1702						
KALR313A	*J1321 45	FO1802	J1214 73	34B	FO1901	J1230 23	12A	FO2200
	J1329 51	FO1702	J1330 51		FO1702			
KALR314A	*J1321 37	FO1802	J1214 71	33B	FO1901	J1314 70	34A	FO5220

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution							
	J1329 46	FO1702	J1330 46		FO1702			
KALR321A	*J1321 32	FO1603						
KALR322A	*J1321 31	FO1603						
KALR323A	*J1321 48	FO1603						
KALR324A	*J1321 47	FO1603	J1322 39		FO1604			
KALR331A	*J1321 40	FO2000	J1234 33	17B	FO2000			
KALR332A	*J1321 38	FO2000	J1234 29	15B	FO2000			
KALR333A	*J1321 22	FO2000	J1234 36	16A	FO2000			
KALR334A	*J1321 19	FO2000	J1234 35	18A	FO2000			
KALR341A	*J1321 55	FO1603	J1129 48	22A	FO1604			
KALR343A	*J1321 77	FO1603	J1317 76		FO1604			
KALR344A	*J1321 76	FO1603	J1317 78		FO1604			
KALR345A	J1321 75	FO1603						
KALR346A	*J1321 73	FO1603	J1317 60		FO1604	J1323 75		FO1603
KALR347A	*J1321 67	FO1603	J1320 72		FO1602			
KALR401A	*J1322 01	FO1604	J1230 59	31B	FO1604			
KALR402A	*J1322 03	FO1604	J1230 47	24A	FO1604			
KALR403A	*J1322 17	FO1604						
KALR404A	*J1322 20	FO1604	J1225 05		FO1602	J1225 64	30A	FO1604
	J1325 37							
KALR411A	*J1322 21	FO1800	J1329 63		FO1702	J1330 63		FO1702
KALR412A	*J1322 36	FO1800	J1329 60		FO1702	J1330 60		FO1702
KALR413A	*J1322 45	FO1800	J1329 61		FO1702	J1330 61		FO1702
KALR414A	*J1322 37	FO1800	J1329 55		FO1702	J1330 55		FO 1702
KALR421A	*J1322 32	FO1604	J1230 75	39A	FO1604			
KALR422A	*J1322 31	FO1604	J1230 51	27B	FO1604			
KALR423A	*J1322 48	FO1604						
KALR424A	*J1322 47	FO1604	J1226 76	37A	FO1601	J1228 26	14A	FO1602
	J1317 38	FO1601	J1325 41					
KALR431A	*J1322 40	FO2000	J1320 62	29A	FO2000			
KALR432A	*J1322 38	FO2000	J1230 61	31A	FO2000			
KALR433A	*J1322 22	FO2000	J1230 64	33A	FO2000	J1233 60	28A	FO2000
KALR434A	*J1322 19	FO2000	J1234 39	19B	FO2000			
KALR441A	*J1322 55	FO1604	J1129 50	23A	FO1604			
KALR443A	*J1322 77	FO1604	J1317 68		FO1604			
KALR444A	*J1322 76	FO1604	J1317 67		FO1604			

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution								
KALR445A	J1322 75		FO1604						
KALR446A	*J1322 73		FO1604	J1317 57		FO1604	J1323 73		FO1604
KALR447A	*J1322 67		FO1604	J1321 72		FO1603			
KALSHA	*J1227 31	15B	FO1602	J1226 11	07A	FO1602			
KALSHOV	*J1226 13	06A	FO1602	J1319 04		FO1602	J1320 04		FO1602
	J1321 04		FO1603	J1322 04		FO1604			
KALSIA	*J1225 01	02B	FO1602	J1226 06	05A	FO1602			
KALSI0V	*J1226 08	04A	FO1602	J1319 02		FO1602			
KALISA	J1127 34	16A	FO2602	*J1317 50		FO1604			
KAMAIA	*J1225 60	28A	FO1604	J1229 68	32A	FO1604			
KAMEIA	*J1227 04	04A	FO1604	J1229 70	33A	FO1604			
KAOPC0	*J1225 14	09A	FO2601	J1223 40	19A	FO2601			
KAPRTA	*J1228 63	33B	FO2601	J1223 42	20A	FO2601			
KARSHA	*J1227 07	03A	FO1602	J1226 27	13B	FO1602			
KARSH0V	*J1226 26	12B	FO1602	J1319 71		FO1602	J1320 71		FO1602
	J1321 71		FO1603	J1322 71		FO1604			
KARSIO	*J1229 66	31A	FO1604	J1322 72		FO1604			
KAT1LA	*J1225 39	19B	FO2601	J1224 03	02A	FO2601			
KAT2LA	*J1223 35	17B	FO2601	J1224 07	03A	FO2601			
KAU2CA	*J1317 70		FO1604	J1320 69		FO1602			
KAU3CA	*J1317 69		FO1604	J1321 69		FO1604			
KAU4CA	*J1317 72		FO1604	J1322 69		FO1604			
KBBHL0	*J1129 45	24B	FO1602	J1314 09	05B	FO5203	J1314 21	10B	FO5203
KBBHM0	*J1129 46	21A	FO1604	J1314 07	04B	FO5203	J1314 19	09B	FO5203
KBIS0A	J1117 36		FO2700	J1211 78	38A	FO2700	*J1317 10		FO2700
KBIS1A	J1211 72	35A	FO2700	*J1317 06		FO2700			
KBIS2A	J1211 77	36B	FO2700	*J1317 11		FO2700			
KBM010	J1314 29	13B	FO5203	*J1318 71		FO1701			
KBM020	J1314 23	11B	FO5203	*J1317 77		FO1604			
KBM030	J1314 25	12B	FO5203	*J1317 80		FO1604			
KBM061X	*J1209 04	02A	FO5202	J1314 50	24A	FO5203			
KBM071X	*J1209 20	10A	FO5202	J1314 47	23A	FO5203			
KBM081X	*J1209 36	17A	FO5202	J1314 45	23B	FO5203			
KBM091X	*J1210 04	02A	FO5202	J1314 43	22B	FO5203			
KBM101X	*J1210 20	100A	FO5203	J1314 41	19B	FO5203			
KBM111X	*J1210 36	17A	FO5203	J1314 39	18B	FO5203			

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution								
KBM121X	*J1211 04	02A	FO5203	J1314 37	17B	FO5203			
KBM131X	*J1211 20	10A	FO5203	J1314 35	16B	FO5203			
KBM141X	*J1211 36	17A	FO5203	J1314 17	08B	FO5203			
KBM151X	*J1118 20	10A	FO5203	J1314 18	09A	FO5203			
KBM161X	*J1118 36	17A	FO5203	J1314 31	14B	FO5203			
KBSMXTB	*J1211 79	37B	FO2700	J1118 34	15B	FO5203	J1319 16		FO1801
	J1320 16		FO1802	J1321 16		FO1802	J1322 16		FO1802
KBSMXTC	*J1211 74	36A	FO2700	J1118 31	14B	FO5203	J1319 15		FO1801
	J1320 15		FO1802	J1321 15		FO1802	J1322 15		FO1802
KBSMXTD	*J1211 80	38B	FO2700	J1118 29	13B	FO5203	J1319 18		FO1801
	J1320 18		FO1802	J1321 18		FO1802	J1322 18		FO1802
KBSYBD4	*J1132 15	07B	FO2200						
KBSYDAV	*J1133 34	15A	FO2200	J1129 55	29B	FO2200	J1130 59	30B	FO2200
KBSYDJ	*J1134 74	35B	FO2200	J1132 11	05B	FO2200			
KBSYDK	*J1134 69	35A	FO2200	J1130 66	32A	FO2200	J1234 45	25B	FO2200
	J1234 50	22A	FO2200						
KBSYD0V	*J1234 43	24B	FO2200	J1134 30	15A	FO2200	J1134 34	16A	FO2200
KBSYD2E	*J1130 68	33A	FO2200	J1129 53	28B	FO2200			
KBSYD3E	*J1130 64	31A	FO2200	J1133 36	16A	FO2200			
KBSYE0V	*J1234 48	21A	FO2200	J1134 29	14B	FO2200			
KBSYNK	*J1134 33	16B	FO2200	J1130 62	30A	FO2200			
KBSYTA	*J1129 57	30B	FO2200	J1133 52	26A	FO2200			
KBSYT0V	*J1133 54	25A	FO2200	J1134 72	34A	FO2200			
KBS09AV	*J1230 25	11A	FO2200	J1314 76	37A	FO2200			
KCCBEA	*J1223 76	37A	FO2300	J1317 52		FO2700			
KCC10JQ	*J1220 56	26A	FO2300	J1111 64	30A	FO2300	J1214 04	02A	FO2601
	J1214 20	100A	FO2601	J1215 04	02A	FO2601	J1215 20	10A	FO2601
KCC10KQ	*J1220 51	27B	FO2300	J1223 64	30A	FO2300	J1230 65	33B	FO2300
	J1233 07	03A	FO2300						
KCC11JQ	*J1220 68	33A	FO2300	J1111 62	29A	FO2300	J1214 06	03A	FO2601
	J1214 22	11A	FO2601	J1215 06	03A	FO2601	J1215 22	11A	FO2601
	J1223 62	29A	FO2300						
KCC11KQ	*J1220 65	33B	FO2300	J1230 79	39B	FO2300	J1233 06	05A	FO2300
KCD8D0T	*J1216 08	04A	FO2601	J1111 74	35B	FO2601	J1211 66	32B	FO2700
	J1214 05	03B	FO2601	J1223 22	12A	FO2601			
KCD8D1T	*J1216 10	05A	FO2601	J1111 75	37B	FO2601	J1214 21	10B	FO2601

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution								
	J1234 55	29B	FO2601						
KCD8D2T	*J1216 14	06A	FO2601	J1215 05	03B	FO2601	J1225 18	10A	FO2601
	J1126 38	20A	FO2601						
KCD8D3T	*J1216 13	07A	FO2601	J1215 21	10B	FO2601	J1227 41	22B	FO2601
KCD800T	*J1214 08	04A	FO2601	J1234 62	29A	FO2601			
KCD801T	*J1214 10	05A	FO2601	J1234 69	35B	FO2601			
KCD802T	*J1214 14	06A	FO2601	J1228 79	39B	FO2601			
KCD803T	*J1214 13	07A	FO2601	J1224 34	16A	FO2601			
KCD804T	*J1214 17	08B	FO2601	J1227 17	08B	FO2601			
KCD805T	*J1214 07	04B	FO2601	J1228 18	10A	FO2601			
KCD807T	*J1214 11	06B	FO2601	J1225 24	13A	FO2601			
KCD811T	*J1214 26	13A	FO2601	J1317 09		FO2700			
KCD812T	*J1214 27	14A	FO2601	J1317 17		FO2700			
KCD813T	*J1214 30	15A	FO2601	J1224 29	14B	FO2601	J1317 08		FO2700
KCD814T	*J1214 33	16A	FO2601	J1227 18	10A	FO2601	J1317 25		FO1601
KCD815T	*J1214 23	11B	FO2601	J1228 20	11A	FO2601			
KCD817T	*J1214 29	13B	FO2601	J1225 26	14A	FO2601			
KCD820T	*J1215 08	04A	FO2601	J1317 07		FO1601			
KCD821T	*J1215 10	05A	FO2601	J1317 34		FO1601			
KCD822T	*J1215 14	06A	FO2601	J1317 19		FO1601			
KCD823T	*J1215 13	07A	FO2601	J1225 17	08B	FO2601	J1317 27		FO1601
	J1317 27		FO2602						
KCD824T	*J1215 17	08B	FO2601	J1317 49		FO1601			
KCD825T	*J1215 07	04B	FO2601	J1317 31		FO1601			
KCD826T	*J1215 09	05B	FO2601	J1128 65	34B	FO2601	J1225 19	09B	FO2601
KCD827T	*J1215 11	06B	FO2601	J1223 25	12B	FO2601	J1234 41	23B	FO2601
	J1317 32		FO1601	J1317 40		FO2700			
KCD830T	*J1215 24	12A	FO2601	J1227 70	33A	FO1901	J1233 38	18A	FO2602
KCD831T	*J1215 26	13A	FO2601	J1226 04	02A	FO1602	J1317 33		FO1601
KCD832T	*J1215 27	14A	FO2601	J1223 19	09B	FO2602	J1225 20	11A	FO2601
	J1234 76	37A	FO2601	J1317 46		FO1601			
KCD833T	*J1215 30	15A	FO2601	J1111 72	34A	FO3601	J1224 36	17A	FO2601
	J1233 37	18B	FO2602						
KCD834T	*J1215 33	16A	FO2601	J1317 35		FO1601	J1317 35		FO2602
KCD835T	*J1215 23	11B	FO2601	J1111 73	36B	FO2601	11127 69	35A	FO2602
	J1226 23	12A	FO2602						

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution								
KCD836T	*J1215 25	12B	FO2601	J1223 26	14A	FO2601	J1227 66	31A	FO1901
KCFGPA	*J1227 27	13B	FO1902	J1233 36	17A	FO2602			
KCIM1TA	*J1209 55	27B	FO1902	J1217 48	22A	FO1902			
KCIM1TB	*J1209 61	31B	FO1901	J1217 46	21A	FO1902			
KCIM1TC	*J1209 60	28A	FO1902	J1217 41	22B	FO1902			
KCIM1TD	*J1209 63	31A	FO1902	J1217 43	23B	FO1902			
KCIM2TA	*J1209 73	34B	FO1902	J1217 34	16A	FO1902			
KCIM2TB	*J1209 79	37B	FO1902	J1217 30	15A	FO1902			
KCIM2TC	*J1209 74	36A	FO1902	J1217 29	14B	FO1902			
KCIM2TD	*J1209 80	38B	FO1902	J1217 31	15B	FO1902			
KCIM3TA	*J1210 55	27B	FO1902	J1217 20	10A	FO1902	J1220 61	31B	FO2300
	J1229 54	25A	FO2300						
KCIM3TB	*J1210 61	31B	FO1902	J1217 18	09A	FO1902	J1220 47	25B	FO2300
	J1229 40	19A	FO2300						
KCIM3TC	*J1210 60	28A	FO1902	J1217 15	08B	FO1902			
KCIM3TD	*J1210 63	31A	FO1902	J1217 17	09B	FO1902			
KCIM4TA	*J1210 73	34B	FO1902	J1217 06	03A	FO1902			
KCIM4TB	*J1210 79	37B	FO1902	J1130 70	34A	FO2300	J1217 04	02A	FO1902
KCIM4TC	*J1210 74	36A	FO1902	J1130 69	34B	FO2300	J1217 01	02B	FO1902
KCIM4TD	*J1210 80	38B	FO1902	J1130 71	35B	FO2300	J1217 03	03B	FO1902
KCI10A	*J1229 38	18A	FO2300	J1220 52	24A	FO2300			
KCI11A	*J1229 52	24A	FO2300	J1220 64	31A	FO2300			
KC00BAY	J1234 57		FO1902	J1209 68		FO1902	J1209 52		FO1902
	J1210 68		FO1902	J1210 52		FO1902			
KCRQ10E	*J1217 47	25B	FO1902	J1103 59	31B	FO2601	J1211 03	02B	FO5203
	J1226 35	18A	FO1902	J1229 64	30A	FO2601	J1314 53	26B	FO2200
	J1318 74		FO1701	J1319 54		FO1801			
KCRQ11E	*J1217 51	27B	FO1902	J1221 05	03B	FO5203	J1226 36	16A	FO1902
	J1314 59	30B	FO2200	J1318 78		FO1701	J1319 33		FO1801
KCRQ12E	*J1217 56	26A	FO1902	J1211 07	04B	FO5203	J1226 29	15B	FO1902
	J1314 56	28B	FO2200	J1318 76		FO1701	J1319 26		FO1801
KCRQ13E	*J1217 52	24A	FO1902	J1211 09	05B	FO5203	J1226 33	17B	FO1902
	J1314 64	30A	FO2200	J1318 73		FO1701	J1319 11		FO1801
KCRQ20E	*J1217 35	17B	FO1902	J1211 11	06B	FO5203	J1226 39	19B	FO1902
	J1227 05	03B	FO1602	J1314 71	33B	FO2200	J1318 70		FO1702
	J1320 54		FO1802						

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution								
KCRQ21E	*J1217 39	19B	FO1902	J1124 69	34B	FO2200	J1211 15	07B	FO5203
	J1226 52	26A	FO1902	J1227 30	15A	FO1602	J1318 80		FO1702
	J1320 33		FO1802						
KCRQ22E	*J1217 42	20A	FO1902	J1211 18	09A	FO5203	J1226 50	22A	FO1902
	J1227 60	28A	FO1602	J1314 77	36B	FO2200	J1318 79		FO1702
	J1320 26		FO1802						
KCRQ23E	*J1217 38	18A	FO1902	J1124 72	35A	FO2200	J1211 17	08B	FO5203
	J1224 54	25A	FO1902	J1233 18	10A	FO1902	J1318 77		FO1702
	J1320 11		FO1802						
KCRQ30E	*J1217 21	11B	FO1902	J1129 49	26B	FO2602	J1211 19	09B	FO5203
	J1225 53	28B	FO1902	J1233 19	09B	FO1902	J1314 72	35A	FO2200
	J1321 54		FO1802						
KCRQ31E	*J1217 27	13B	FO1902	J1211 21	10B	FO5203	J1228 62	29A	FO1902
	J1318 26		FO1701	J1321 33		FO1802			
KCRQ32E	*J1217 25	14A	FO1902	J1211 23	11B	FO5203	J1228 19	09B	FO1902
KCRQ33E	*J1217 24	12A	FO1902	J1211 25	12B	FO5203	J1223 75	37B	FO2300
	J1228 17	08B	FO1902						
KCRQ40E	*J1217 07	05B	FO1902	J1211 29	13B	FO5203	J1214 19	09B	FO2601
	J1215 03	02B	FO2601	J1215 19	09B	FO2601	J1225 71	36A	FO1902
	J1227 25	12B	FO1902						
KCRQ41E	*J1217 11	07B	FO1902	J1211 31	14B	FO5203	J1216 04	02A	FO2601
	J1225 65	34B	FO1902	J1227 23	11B	FO1902	J1322 33		FO1802
KCRQ42E	*J1217 13	07A	FO1902	J1211 34	15B	FO5203	J1216 06	03A	FO2601
	J1225 76	37A	FO1902	J1317 36		FO1601	J1322 26		FO1802
KCRQ43E	*J1217 10	05A	FO1902	J1128 43	23B	FO1902	J1211 33	16A	FO5203
	J1216 03	02B	FO2601	J1322 11		FO1802			
KCR00AV	*J1226 37	17A	FO1902	J1211 64	30A	FO2400	J1229 20	11A	FO2601
	J1313 22		FO2502						
KCR01AV	*J1226 34	15A	FO1902	J1211 56	28B	FO2400	J1313 56		FO2502
KCR02AV	*J1226 30	14B	FO1902	J1211 59	30B	FO2400	J1313 71		FO2502
KCR03AV	*J1226 31	16B	FO1902	J1211 53	26B	FO2400	J1313 62		FO2502
KCR04AV	*J1226 42	18B	FO1902	J1228 59	31B	FO2601	J1313 60		FO2502
KCR05AV	*J1226 54	25A	FO1902	J1313 34		FO2502	J1317 26		FO1601
KCR06AV	*J1226 48	21A	FO1902	J1313 35		FO2502			
KCR07A	*J1224 52	24A	FO1902	J1211 76	37A	FO2700	J1225 04	04A	FO1602
	J1226 41	23B	FO1604	J1227 08	06A	FO1604	J1228 24	13A	FO1602

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution								
	J1313 24		FO2502						
KCR070V	*J1226 46	22B	FO1604	J1225 62	29A	FO1604			
KCR08A	*J1225 57	30B	FO1902	J1211 70	34A	FO2700	J1226 45	25B	FO2700
	J1313 25		FO2502						
KCR080V	*J1226 43	24B	FO2700	J1317 53		FO2700			
KCR09A	*J1228 60	28A	FO1902	J1211 75	35B	FO2700	J1225 11	05B	FO2300
	J1233 20	11A	FO1902	J1313 23		FO2502	J1314 78	38A	FO2200
KCR100V	*J1230 68	32B	FO2300	J1321 26		FO1802			
KCR110V	*J1230 80	38B	FO2300	J1321 11		FO1802			
KCR12A	*J1225 72	34A	FO1902	J1224 48	22A	FO1902	J1227 33	16B	FO2601
	J1227 52	24A	FO1902	J1313 47		FO2502	J1314 49	24B	FO2200
	J1314 66	32B	FO2200	J1317 15		FO2700			
KCR120	*J1227 50	23A	FO1902	J1214 03	02B	FO2601	J1233 05	03B	FO2300
	J1317 42		FO2700	J1322 54		FO1802			
KCR13A	*J1225 69	35A	FO1902	J1233 04	04A	FO2300	J1233 22	12A	FO1902
KCR14A	*J1225 80	39A	FO1902	J1223 55	29B	FO2300	J1227 21	10B	FO1902
	J1233 01	02B	FO2300	J1233 24	13A	FO1902			
KCSDFB	*J1132 15	07B	FO2200	J02 24		FO2501	J1217 71	35B	FO2501
	J1231 19		FO2200						
KCSFB10E	*J1217 75	37B	FO2501	J1223 74	35B	FO2501	J1313 48		FO2501
KCSFB11E	*J1217 79	39B	FO2501	J1223 73	36B	FO2501	J1227 13	06B	FO2501
KCSFB12E	*J1217 80	39A	FO2501	J1223 72	34A	FO2501	J1227 09	05B	FO2501
KCSFB13E	*J1217 76	37A	FO2501	J1223 71	36A	FO2501	J1226 51	27B	FO2501
	J1227 11	04B	FO2501						
KCTRKA	*J1225 75	37B	FO5403	J1213 51	25B	FO1901	J1214 37	17B	FO1901
	J1214 69	32A	FO1901	J1215 37	17B	FO2400	J1318 60		FO1701
KDBACAV	*J1230 03	03A	FO2800	J1233 36	17A	FO2602			
KDBAC0	*J1229 27	13B	FO2800	J1230 04	02A	FO2800	J1318 50		FO2800
KDBAKAV	*J1226 19	10B	FO2800	J04 35		FO2800			
KDBAKJ	*J1219 61	32B	FO2800	J1213 79	37B	FO2900	J1214 61	31B	FO2900
	J1215 79	37B	FO2900	J1226 21	11B	FO2800	J1229 34	16A	FO2800
	J1318 09		FO2800	J1318 17		FO2800			
KDBAKK	*J1219 59	31B	FO2800	J1228 50	23A	FO2800			
KDBC80	*J1318 01		FO2800	J1318 18		FO2800			
KDBC90	*J1318 02		FO2800	J1318 15		FO2800			

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution								
KDBEMA	J1226 20	10A	FO2800	*J1318 13		FO2800			
KDBEMOV	*J1226 18	09A	FO2800	J1228 23	11B	FO2800			
KDBFLA	J1230 52	26A	FO2800	*J1318 14		FO2800			
KDBMATA	*J1121 55	27B	FO2900	J1311 63		FO3002	J1312 63		FO3002
KDBMATB	*J1121 61	31B	FO2900	J1311 62		FO3002	J1312 62		FO3002
KDBMATC	*J1121 60	28A	FO2900	J1311 60		FO3002	J1312 60		FO3002
KDBMATD	*J1121 63	31A	FO2900	J1311 29		FO3002	J1312 29		FO3002
KDBMBTA	*J1121 73	34B	FO2900	J1311 32		FO3002	J1312 32		FO3002
KDBMBTBA	*J1121 79	378	FO2900	J1311 41		FO3002	J1312 41		FO3002
KDBMBTC	*J1121 74	36A	FO2900	J1311 48		FO3002	J1312 48		FO3002
KDBMBTD	*J1121 80	38B	FO2900	J1311 45		FO3002	J1312 45		FO3002
KDBMCTA	*J1120 55	27B	FO2900	J1311 43		FO3002	J1312 43		FO3002
KDBMCTB	*J1120 61	31B	FO2900	J1311 46		FO3002	J1312 46		FO3002
KDBMDTA	*J1120 73	34B	FO3001	J1312 55		FO3002			
KDBMDTB	*J1120 79	37B	FO3001	J1312 26		FO3002			
KDBMDTC	*J1120 74	36A	FO3001	J1312 27		FO3002			
KDBMDTD	*J1120 80	38B	FO3001	J1312 31		FO3002			
KDBMETA	*J1119 55	27B	FO3001	J1312 25		FO3002			
KDBMETB	*J1119 61	31B	FO3001	J1312 51		FO3002			
KDBMETC	*J1119 60	28A	FO3001	J1312 30		FO3002			
KDBMETD	*J1119 63	31A	FO3001	J1312 34		FO3002			
KDBMFTA	*J1119 73	34B	FO3001	J1311 55		FO3002			
KDBMFTB	*J1119 79	37B	FO3001	J1311 26		FO3002			
KDBMFTC	*J1119 74	36A	FO3001	J1311 27		FO3002			
KDBMFTD	*J1119 80	38B	FO3001	J1311 31		FO3002			
KDBMGTA	*J1118 73	34B	FO3001	J1311 25		FO3002			
KDBMGTB	*J1118 79	37B	FO3001	J1311 51		FO3002			
KDBMGTC	*J1118 74	36A	FO3001	J1311 30		FO3002			
KDBMGTD	*J1118 80	38B	FO3001	J1311 34		FO3002			
KDBMTK	*J1219 47	25B	FO2800	J1228 54	25A	FO2800			
KDBRAJQ	*J1220 42	20A	FO2800	J1215 61	31B	FO2900	J1216 61	31B	FO2900
	J1216 79	37B	FO2900	J1219 46	21A	FO2800	J1226 47	24A	FO2800
	J1229 31	15B	FO2800						
KDBRAKQ	*J1220 39	19B	FO2800	J1229 25	12B	FO2800			
KDBRAIU	*J1216 54	26A	FO2900	J1121 53	26B	FO2900			
KDBRA2U	*J1216 56	28B	FO2900	J1121 59	30B	FO2900			

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution								
KDBRA3U	*J1216 60	28A	FO2900	J1121 56	28B	FO2900			
KDBRA4U	*J1216 62	29A	FO2900	J1121 64	30A	FO2900			
KDBRA5U	*J1216 52	25A	FO2900	J1215 64	30A	FO2900			
KDBRB1U	*J1215 54	26A	FO2900	J1121 71	33B	FO2900			
KDBRB2U	*J1215 56	28B	FO2900	J1121 77	36B	FO2900			
KDBRB3U	*J1215 60	28A	FO2900	J1121 72	35A	FO2900			
KDBRB4U	*J1215 62	29A	FO2900	J1121 78	38A	FO2900			
KDBRB5U	*J1215 52	25A	FO2900	J1216 78	38A	FO2900			
KDBRC1U	*J1216 70	34A	FO2900	J1120 53	26B	FO2900			
KDBRC2U	*J1216 72	35A	FL2900	J1120 59	30B	FO2900			
KDBRFJ	*J1134 78	38A	FO2800	J1313 20		FO2502			
KDBRFK	*J1134 76	37A	FO2800	J1127 59	31B	FO2602	J1129 62	29A	FO2800
	J1220 37	18B	FO2800						
KDBRIA	*J1228 52	24A	FO2800	J1129 64	30A	FO2800	J1220 33	16B	FO2800
KDBRJAV	*J1226 49	23A	FO2800	J1220 23	12B	FO2800			
KDBRN0	*J1129 60	28A	FO2800	J1223 30	15A	FO2602			
KDBRP0V	*J1226 57	30B	FO3002	J1311 33	ETP		J1311 37		FO3002
	J1312 33	ETP		J1312 37		FO3002			
KDBRRA	*J1228 01	02B	FO2601	J1230 29	15B	FO2601			
KDBRR0V	*J1230 30	14B	FO2601	J1134 79	39B	FO2800	J1313 04		FO2502
KDBSC0V	*J1230 54	25A	FO2800	J1219 48	22A	FO2800			
KDBSFA	*J1229 33	16B	FO2800	J1230 45	25B	FO2800	J1311 73		FO3002
	J1311 77		FO3002	J1312 73		FO3002	J1312 77		FO3002
KDBSF0V	*J1230 43	24B	FO2800	J1134 77	38B	FO2800	J1220 38	18A	FL2800
	J1228 25	12B	FO2800						
KDBSMA	*J1228 27	13B	FO2800	J1230 39	19B	FO2800			
KDBSWAV	*J1226 68	32B	FO2800	J1120 49	24B	FO2900	J1121 49	24B	FO2900
	J1121 66	32B	FO2900	J1229 23	11B	FO2800			
KDBSW0	*J1228 46	21A	FO2800	J1226 65	33B	FO2800			
KDBT20	J1318 16		FO2800	*J1318 23		FO2800			
KDBT30	J1219 56	26A	FO2800	*J1318 07		FO2800			
KDBWAJQ	*J1220 25	14A	FO2800	J1219 54	25A	FO2800	J1219 68	32A	FO2800
	J1226 75	39A	FO2800	J1229 36	17A	FO2800			
KDBWAKQ	*J1220 27	13B	FO2800	J1219 70	33A	FO2800	J1228 48	22A	FO2800
KDBWA1U	*J1215 70	34A	FO2900	J1121 51	25B	FO2900			

ETP = EXTRA TIE POINT

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution								
KDBWA2U	*J1215 72	35A	FO2900	J1121 57	29B	FO2900			
KDBWA3U	*J1215 74	36A	FO2900	J1121 54	26A	FO2900			
KDBWA4U	*J1215 76	37A	FO2900	J1121 62	29A	FO2900			
KDBWA5U	*J1215 68	33A	FO2900	J1214 64	30A	FO2900			
KDBWB1U	*J1214 54	26A	FO2900	J1121 69	32A	FO2900			
KDBWB2U	*J1214 56	28B	FO2900	J1121 75	35B	FO2900			
KDBWB3U	*J1214 60	28A	FO2900	J1121 70	34A	FO2900			
KDBWB4U	*J1214 62	29A	FO2900	J1121 76	37A	FO2900			
KDBWB5U	*J1214 52	25A	FO2900	J1213 78	38A	FO2900			
KDBWC1U	*J1213 70	34A	FO2900	J1120 51	25B	FO2900			
KDBWC2U	*J1213 72	35A	FO2900	J1120 57	29B	FO2900			
KDBWJAV	*J1226 77	38A	FO2800	J1220 35	17B	FO2800			
KDBWPA	*J1229 30	15A	FO2800	J1311 38		FO3002	J1311 40		FO3002
	J1312 38		FO3002	J1312 40		FO3002			
KDB0FK	*J1219 45	24B	FO2800	J1220 19	10B	FO2800			
KDB010E	J1209 03	02B	FO5202	*J1312 72		FO3002	J1319 52		FO1801
KDB011E	J1209 05	03B	FO5202	*J1312 65		FO3002	J1319 29		FO1801
KDB012E	J1209 07	04B	FO5202	*J1312 78		FO3002	J1319 25		FO1801
KDB013E	J1209 09	05B	FO5202	*J1312 79		FO3002	J1319 10		FO1801
KDB020E	J1209 11	06B	FO5202	*J1312 68		FO3002	J1320 52		FO1802
KDB021E	J1209 15	07B	FO5202	*J1312 69		FO3002	J1320 29		FO1802
KDB022E	J1209 18	09A	FO5202	*J1312 76		FO3002	J1320 25		FO1802
KDB023E	J1209 17	08B	FO5202	*J1312 74		FO3002	J1320 10		FO1802
KDB030E	J1209 19	09B	FO5202	*J1311 72		FO3002	J1321 52		FO1802
KDB031E	J1209 21	10B	FO5202	*J1311 65		FO3002	J1321 29		FO1802
KDB032E	J1209 23	11B	FO5202	*J1311 78		FO3002	J1321 25		FO1802
KDB033E	J1209 25	12B	FO5202	*J1311 79		FO3002	J1321 10		FO1802
KDB040E	J1209 29	13B	FO5202	*J1311 68		FO3002	J1322 52		FO1802
KDB041E	J1209 31	14B	FO5202	*J1311 69		FO3002	J1322 29		FO1802
KDB042E	J1209 34	15B	FO5202	*J1311 76		FO3002	J1322 10		FO1802
	J1322 25		FO1802						
KDB043E	J1209 33	16A	FO5202	*J1311 74		FO3002	J1313 07		FO2502
KDB06KQ	*J1220 11	07B	FO2200	J1129 76	37A	FO2200			
KDCG0AV	*J1230 10	06B	FO2200	J1324 49	26B	FO2200			
KDCTBA	*J1128 45	24B	FO1902	J04 50		FO1902			
KDC0BAV	*J1234 57	30B	FO2400	J1209 52	25A	FO1901	J1209 68	33A	FO1901

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution								
	J1210 52	25A	FO1901	J1210 68	33A	FO1901	J1211 52	25A	FO2400
	J1216 05	03B	FO2601	J1216 21	10B	FO1901	J1234 57		FO1901
KDC0CAV	*J1234 68	32B	FO2400	J1211 57	29B	FO2400	J1211 68	33A	FO2700
	J1311 23		FO3002	J1311 24	ETP		J1311 66		FO3002
	J1311 71		FO3002	J1312 23		FO3002	J1312 24	ETP	
	J1312 66		FO3002	J1312 71		FO3002	J1319 49		FO1801
	*J1234 68		FO3002	J1234 68		FO 1801			
KDC0DAV	*J1234 80	38B	FO2400	J1130 74	36A	FO2300	J1211 54	26A	FO2400
	J1217 08	04A	FO1902	J1217 22	11A	FO1902	J1217 36	17A	FO1902
	J1217 50	23A	FO1902	J1311 75		FO3002	J1311 80		FO3002
	J1312 75		FO3002	J1312 80		FO3002	*J1234 80		FO3002
	J1234 80		FO1902						
KDC0EAV	*J1234 71	36B	FO2400	J1119 13	07A	FO5202	J1119 30	15A	FO5202
	J1124 62	30A	FO2200	J1124 74	36A	FO2200	J1211 62	29A	FO2400
	J1217 74	36A	FO2501	J1319 57		FO1801	*J1234 71		XTOP00
	J1234 71		FO1801	J1234 71		FO2501			
KDC0FAV	*J1116 68	32B	FO2100	J1122 14	06A	FO2100	J1122 22	11A	FO2100
	J1122 40	19A	FO2100	J1122 50	23A	FO2100	J1122 66	32A	FO2100
	J1122 74	36A	FO2100	J1123 08	04A	FO2100	J1123 26	13A	FO2100
	J1123 36	17A	FO2100	J1123 54	25A	FO2100	J1123 62	30A	FO2100
	J1123 78	38A	FO2100						
KDC0GAV	*J1116 80		FO2200	*J1116 80	38B	FO2900	*J1116 80		FO3001
	J1101 09	02A	FO2100	J1101 46	25B	FO2100	J1101 54	30B	FO2100
	J1118 68	33A	FO3001	J1119 52	25A	FO1902	J1119 68	33A	FO3001
	J1120 52	25A	FO2900	J1120 68	33A	FO3001	J1121 52	25A	FO2900
	J1121 68	33A	FO2900	J1314 52	25A	FO2200	J1314 68	33A	FO2200
KDC0HAV	*J1230 37	17A	FO5202	J1118 30	15A	FO5203	J1118 48	22A	FO5203
	J1209 13	07A	FO5202	J1209 30	15A	FO5202	J1209 48	22A	FO5202
	J1210 13	07A	FO5202	J1210 30	15A	FO5203	J1210 48	22A	FO5203
	J1211 13	07A	FO5203	J1211 30	15A	FO5203	J1211 48	22A	FO5203
KD1G20	*J1224 46	21A	FO1902	J1233 26	14A	FO1902			
KD7R3A	*J1228 21	10B	FO1902	J1224 50	23A	FO1902			
KD8D10V	*J1234 56	28B	FO2601	J1227 37	18B	FO2601	J1317 39	FO27	00
KD8D20V	*J1226 40	19A	FO2601	J1317 43		FO2700			
KD8D30	*J1227 43	23B	FO2601	J1317 16		FO2700			

ETP = EXTRA TIE POINT

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution							
KEBTHAV	*J1226 01	02B	FO2601	J1223 37	18B	FO2601		
KEBTH0	*J1225 21	10B	FO2601	J1226 05	03B	FO2601		
KESCPA	*J1225 51	27B	FO2400	J1228 13	06B	FO2400		
KFA000	*J1318 57		FO1701	J1328 08		FO1702	J1328 38	FO1702
	J1328 60		FO1702	J1329 74		FO1702	J1330 74	FO1701
KFA010	*J1318 55		FO1701	J1328 09		FO1702	J1328 35	FO1702
	J1328 61		FO1702	J1329 73		FO1702	J1330 73	FO1701
KFA020	*J1318 54		FO1701	J1328 10		FO1702	J1328 39	FO1702
	J1328 62		FO1702	J1329 77		FO1702	J1330 77	FO1701
KFA030	*J1318 75		FO1701	J1328 18		FO1702	J1328 36	FO1702
	J1328 64		FO1702	J1329 72		FO1702	J1330 72	FO1701
KFA040	*J1318 49		FO1701	J1328 23		FO1702	J1328 40	FO1702
	J1328 70		FO1702					
KFA050	*J1318 52		FO1701	J1328 24		FO1702	J1328 37	FO1702
	J1328 72		FO1702					
KFBS0A	*J1318 41		FO1701	J1329 05		FO1702		
KFBS1A	*J1318 45		FO1701	J1329 80		FO1702		
KFBS2A	*J1318 46		FO1701	J1330 05		FO1702		
KFBS3A	*J1318 48		FO1701	J1330 80		FO1702		
KFCB00	*J1318 24		FO1701	J1328 27		FO1702	J1328 29	FO1702
KFCB10	*J1318 37		FO1701	J1328 31		FO1702	J1328 48	FO1702
KFCB20	*J1318 34		FO1701	J1328 63		FO1702	J1328 80	FO1702
KFCB30	*J1318 38		FO1701	J1328 17		FO1702	J1328 43	FO1702
KFCM100B	*J1328 59		FO1702	J1327 10	07A	FO1702		
KFCM101B	*J1328 57		FO1702	J1327 05	03B	FO1702		
KFCM102B	*J1328 56		FO1702	J1327 13	06B	FO1702		
KFCM103B	*J1328 55		FO1702	J1327 26	14A	FO1702		
KFCM104B	*J1328 65		FO1702	J1327 18	10A	FO1702		
KFCM105B	*J1328 66		FO1702	J1327 25	12B	FO1702		
KFCM106B	*J1328 68		FO1702	J1327 42	20A	FO1702		
KFCM107B	*J1328 69		FO1702	J1327 34	16A	FO1702		
KFCM140B	*J1328 13		FO1702					
KFCM141B	*J1328 11		FO1702					
KFCM142B	*J1328 15		FO1702					
KFCM143B	*J1328 14		FO1702					
KFCM144B	*J1328 22		FO1702					

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution						
KFCM145B	*J1328 19	FO1702					
KFCM146B	*J1328 21	FO1702					
KFCM147B	*J1328 20	FO1702					
KFCM150B	*J1328 46	FO1702					
KFCM151B	*J1328 47	FO1702					
KFCM152B	*J1328 74	FO1702					
KFCM153B	*J1328 75	FO1702					
KFCM154B	*J1328 76	FO1702					
KFCM155B	*J1328 77	FO1702					
KFCM156B	*J1328 78	FO1702					
KFCM157B	*J1328 79	FO1702					
KFCM160B	*J1328 49	FO1702					
KFCM161B	*J1328 50	FO1702					
KFCM162B	*J1328 51	FO1702					
KFCM163B	*J1328 52	FO1702					
KFCM164B	*J1328 53	FO1702					
KFCM165B	*J1328 54	FO1702					
KFCM166B	*J1328 71	FO1702					
KFCM167B	*J1328 73	FO1702					
KFCM170B	*J1328 01	FO1702					
KFCM171B	*J1328 03	FO1702					
KFCM172B	*J1328 04	FO1702					
KFCM173B	*J1328 05	FO1702					
KFCM174B	*J1328 06	FO1702					
KFCM175B	*J1328 07	FO1702					
KFCM176B	*J1328 25	FO1702					
KFCM177B	*J1328 26	FO1702					
KFC08B	*J1328 01	FO1702	*J1328 13		FO1702	*J1328 46	FO1702
	*J1328 49	FO1702	J1327 37	18B	FO1702		
KFC09B	*J1328 03	FO1702	*J1328 11		FO1702	*J1328 47	FO1702
	*J1328 50	FO1702	J1327 56	26A	FO1702		
KFC10B	*J1328 04	FO1702	*J1328 15		FO1702	*J1328 51	FO1702
	*J1328 74	FO1702	J1327 48	22A	FO1702		
KFC11B	*J1328 05	FO1702	*J1328 14		FO1702	*J1328 52	FO1702
	*J1328 75	FO1702	J1327 49	26B	FO1702		
KFC12B	*J1328 06	FO1702	*J1328 22		FO1702	*J1328 53	FO1702

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution							
	*J1328 76		FO1702	*J1327 70	33A	FO1702		
KFC13B	*J1328 07		FO1702	*J1328 19		FO1702	*J1328 54	FO1702
	*J1328 77		FO1702	JP327 62	29A	FO1702		
KFC14B	*J1328 21		FO1702	*J1328 25		FO1702	*J1328 71	FO1702
	*J1328 78		FO1702	J1327 61	32B	FO1702		
KFC15B	*J1328 20		FO1702	*J1328 26		FO1702	*J1328 73	FO1702
	*J1328 79		FO1702	J1327 79	39B	FO1702		
KFD000	*J1327 04	04A	FO1702	J1209 35	16B	FO5202	J1319 53	FO1801
	J1319 53		FO1602					
KFD010	*J1327 07	03A	FO1702	J1209 37	17B	FO5202	J1319 35	FO1801
	J1319 35		FO1602					
KFD020	*J1327 15	07B	FO1702	J1209 39	18B	FO5202	J1319 74	FO1801
	J1319 74		FO1602					
KFD030	*J1327 20	11A	FO1702	J1209 41	19B	FO5202	J1319 09	FO1801
	J1319 09		FO1602					
KFD040	*J1327 19	09B	FO1702	J1209 43	22B	FO5202	J1320 53	FO1802
	J1320 53		FO1602					
KFD050	*J1327 27	13B	FO1702	J1209 45	23B	FO5202	J1320 35	FO1802
	J1320 35		FO1602					
KFD060	*J1327 36	17A	FO1702	J1209 47	23A	FO5202	J1320 74	FO1802
	J1320 74		FO1602					
KFD070	*J1327 31	15B	FO1702	J1209 50	24A	FO5202	J1320 09	FO1802
	J1320 09		FO1602					
KFD080	*J1327 39	19B	FO1702	J1210 03	02B	FO5202	J1321 53	FO1802
	J1321 53		FO1603					
KFD090	*J1327 50	23A	FO1702	J121005	03B	FO5202	J1321 35	FO1802
	J1321 35		FO1603					
KFD100	*J1327 43	23B	FO1702	J1210 07	04B	FO5202	J1321 74	FO1802
	J1321 74		FO1603					
KFD110	*J1327 51	27B	FO1702	J1210 09	05B	FO5202	J1321 09	FO1802
	J1321 09		FO1603					
KFD120	*J1327 64	30A	FO1702	J1210 11	06B	FO5202	J1322 53	FO1802
	J1322 53		FO1604					
KFD130	*J1327 55	29B	FO1702	J1210 15	07B	FO5202	J1322 35	FO1802
	J1322 35		FO1604					
KFD140	*J1327 63	33B	FO1702	J1210 18	09A	FO5202	J1322 74	FO1802

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution							
	J1322 74		FO1604					
KFD150	*J1327 73	36B	FO1702	J1210 17	08B	FO5202	J1322 09	FO1802
	J1322 09		FO1604					
KFRW100C	*J1329 27		FO1702	J1327 06	05A	FO1702		
KFRW101C	*J1329 31		FO1702	J1327 01	02B	FO1702		
KFRW102C	*J1329 36		FO1702	J1327 09	04B	FO1702		
KFRW103C	*J1329 35		FO1702	J1327 22	12A	FO1702		
KFRW104C	*J1329 37		FO1702	J1327 14	09A	FO1702		
KFRW105C	*J1329 40		FO1702	J1327 21	10B	FO1702		
KFRW106C	*J1329 41		FO1702	J1327 38	18A	FO1702		
KFRW107C	*J1329 45		FO1702	J1327 29	14B	FO1702		
KFRW108C	*J1329 49		FO1702	J1327 33	16B	FO1702		
KFRW109C	*J1329 50		FO1702	J1327 52	24A	FO1702		
KFRW110C	*J1329 54		FO1702	J1327 41	22B	FO1702		
KFRW111C	*J1329 56		FO1702	J1327 45	24B	FO1702		
KFRW112C	*J1329 57		FO1702	J1327 66	31A	FO1702		
KFRW113C	*J1329 59		FO1702	J1327 53	28B	FO1702		
KFRW114C	*J1329 62		FO1702	J1327 57	30B	FO1702		
KFRW115C	*J1329 65		FO1702	J1327 75	37B	FO1702		
KFRW200C	*J1330 27		FO1702	J1327 08	06A	FO1702		
KFRW201C	*J1330 31		FO1702	J1327 03	02A	FO1702		
KFRW202C	*J1330 36		FO1702	J1327 11	05B	FO1702		
KFRW203C	*J1330 35		FO1702	J1327 24	13A	FO1702		
KFRW204C	*J1330 37		FO1702	J1327 17	08B	FO1702		
KFRW205C	*J1330 40		FO1702	J1327 23	11B	FO1702		
KFRW206C	*J1330 41		FO1702	J1327 40	19A	FO1702		
KFRW207C	*J1330 45		FO1702	J1327 30	15A	FO1702		
KFRW208C	*J1330 49		FO1702	J1327 35	17B	FO1702		
KFRW209C	*J1330 50		FO1702	J1327 54	25A	FO1702		
KFRW210C	*J1330 54		FO1702	J1327 46	21A	FO1702		
KFRW211C	*J1330 56		FO1702	J1327 47	25B	FO1702		
KFRW212C	*J1330 57		FO1702	J1327 68	32A	FO1702		
KFRW213C	*J1330 59		FO1702	J1327 60	28A	FO1702		
KFRW214C	*J1330 62		FO1702	J1327 59	31B	FO1702		
KFRW215C	*J1330 65		FO1702	J1327 77	38B	FO1702		
KFWBSA	*J1228 38	18A	FO2601	J1127 77	38B	FO2601		

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution								
KFWDRA	*J1228 30	15A	FO2601	J1127 79	39B	FO2601			
KFWEN0	*J1127 73	36B	FO2601	J1329 03		FO1702	J1330 03		FO1702
KFWSCA	*J1227 39	19B	FO2601	J1127 75	37B	FO2601	J1223 24	13A	FO2601
KGRSWA	*J1225 06	05A	FO2601	J1313 42		FO2502			
KGSSWA	*J1228 80	39A	FO2601	J1313 70		FO2502			
KHC1B0	*J1128 22	12A	FO5202	J1118 27	14A	FO5203	J1118 46	21A	FO5203
	J1209 14	06A	FO5202	J1209 27	14A	FO5202	J1209 46	21A	FO5202
	J1210 14	06A	FO5202	J1210 27	14A	FO5203	J1210 46	21A	FO5203
	J1211 14	06A	FO5203	J1211 27	14A	FO5203	J1211 46	21A	FO5203
KHC1C0	*J1128 21	10B	FO5202	J1118 14	06A	FO3500	J1119 14	06A	FO5202
	J1119 27	14A	FO5202	J1317 73		FO1604	J1318 65		FO1701
	J1319 59		FO1602	J1320 59		FO1602	J1321 59		FO1603
	J1322 59		FO1604						
KHC2B0	*J1128 33	16B	FO5202	J1118 26	13A	FO5203	J1118 42	20A	FO5203
	J1209 10	05A	FO5202	J1209 26	13A	FO5202	J1209 42	20A	FO5202
	J1210 10	05A	FO5202	J1210 26	13A	FO5203	J1210 42	20A	FO5203
	J1211 10	05A	FO5203	J1211 26	13A	FO5203	J1211 42	20A	FO5203
KHC2C0	*J1128 27	13B	FO5202	J1118 10	05A	FO3500	J1119 10	05A	FO5202
	J1119 26	13A	FO5202	J1317 74		FO1602	J1318 66		FO1701
	J1319 62		FO1602	J1320 62		FO1602	J1321 62		FO1603
	J1322 62		FO1604						
KHC3B0	*J1128 39	19B	FO5202	J1118 24	12A	FO5203	J1118 40	19A	FO5203
	J1209 08	04A	FO5202	J1209 24	12A	FO5202	J1209 40	19A	FO5202
	J1210 08	04A	FO5202	J1210 24	12A	FO5203	J1210 40	19A	FO5203
	J1211 08	04A	FO5203	J1211 24	12A	FO5203	J1211 40	19A	FO5203
KHC3C0	*J1128 38	18A	FO5202	J1118 08	04A	FO3500	J1119 08	04A	FO5202
	J1119 24	12A	FO5202	J1317 71		FO1604	J1318 69		FO1701
	J1319 60		FO1602	J1321 60		FO1603			
KHRLDA	*J1127 51	27B	FO2602	J1230 06	05A	FO2000			
KHRLD0V	*J1230 08	04A	FO2000	J1319 80		FO2000	J1320 80		FO2000
	J1321 80		FO2000	J1322 80		FO2000			
KHVEQA	*J1223 09	04B	FO2200	J1232 26	14A	FO2000			
KH000AV	*J1234 10	06B	FO2000	J1232 24	13A	FO2000			
KH000D4	*J1232 22	12A	FO2000	J02 01		FO2000			
KH001AV	*J1234 24	13A	FO2000	J1232 18	10A	FO2000			
KH001D4	*J1232 14	09A	FO2000	J02 02		FO2000			

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution									
KH002D4	*J1232	21	10B	FO2000	J02	03		FO2000			
KH003AV	*J1234	18	09A	FO2000	J1232	23	11B	FO2000			
KH003D4	*J1232	27	13B	FO2000	J02	04		FO2000			
KH004AV	*J1234	14	08B	FO2000	J1232	40	19A	FO2000			
KH004D4	*J1232	38	18A	FO2000	J02	05		FO2000			
KH005AV	*J1234	19	10B	FO2000	J1232	34	16A	FO2000			
KH005D4	*J1232	30	15A	FO2000	J02	06		FO2000			
KH006AV	*J1234	26	12B	FO2000	J1232	29	14B	FO2000			
KH006D4	*J1232	33	16B	FO2000	J02	07		FO2000			
KH007AV	*J1234	40	19A	FO2000	J1232	35	17B	FO2000			
KH007D4	*J1232	39	19B	FO2000	J02	08		FO2000			
KH008AV	*J1234	37	17A	FO2000	J1232	54	25A	FO2000	J1233	70	33A	FO2000
KH008D4	*J1232	52	24A	FO2000	J02	09		FO2000			
KH009AV	*J1234	34	15A	FO2000	J1232	48	22A	FO2000	J1233	68	32A	FO2000
KH009D4	*J1232	46	21A	FO2000	J02	10		FO2000			
KH010AV	*J1234	30	14B	FO2000	J1232	41	22B	FO2000	J1233	66	31A	FO2000
KH010D4	*J1232	45	24B	FO2000	J02	11		FO2000			
KH011AV	*J1234	31	16B	FO2000	J1232	47	25B	FO2000	J1233	62	29A	FO2000
KH011D4	*J1232	51	27B	FO2000	J02	12		FO2000			
KH012AV	*J1234	42	18B	FO2000	J1232	68	32A	FO2000	J1233	61	32B	FO2000
KH012D4	*J1232	66	31A	FO2000	J02	13		FO2000			
KH013AV	*J1230	66	32A	FO2000	J1232	62	29A	FO2000			
KH013D4	*J1232	60	28A	FO2000	J02	14		FO2000			
KH014AV	*J1230	63	30A	FO2000	J1232	53	28B	FO2000	J1233	55	29B	FO2000
KH014D4	*J1232	57	30B	FO2000	J02	15		FO2000			
KH015AV	*J1230	60	28A	FO2000	J1232	59	31B	FO2000			
KH015D4	*J1232	63	33B	FO2000	J02	16		FO2000			
KICENA	*J1229	01	02B	FO2602	J1129	77	38B	FO2602			
KICEN0	*J1129	75	37B	FO2602	J1318	59		FO1701			
KICLDA	*J1229	15	07B	FO2601	J1318	61		FO1701			
KICNMA	*J1223	59	31B	FO2602	J1129	31	15B	FO2602	J1129	79	39B	FO2602
KICTCA	J1234	47	24A	FO2602	*J1318	27		FO1701			
KICTC0V	*J1234	49	23A	FO2602	J1127	60	28A	FO2602			
KLBZ52X	*J1314	22	11A	FO5203	J04	30		FO5202			
KLBZ62X	*J1314	38	18A	FO5203	J04	31		FO5202			
KLBZ72X	*J1314	06	03A	FO5203	J04	29		FO5202			

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution								
KLEFFA	*J1224 15	07B	FO2200	J1226 69	35B	FO2200			
KLEFF0	*J1226 70	34B	FO2200	J1324 56	26A	FO2200			
KLENC0	*J1228 72	34A	FO2200	J1124 66	32A	FO2200	J1324 31	15B	FO2200
	J1324 36	17A	FO2200	J1324 42	20A	FO2200			
KLENFJ	*J1218 13	06B	FO2200	J1220 14	06A	FO2200	J1224 11	05B	FO2200
	J1324 37	18B	FO2200	J1324 50	23A	FO2200	J1324 64	30A	FO2200
	J1324 70	33A	FO2200						
KLENFK	*J1218 11	05B	FO2200	J1225 34	16A	FO2200	J1228 73	36B	FO2200
	J1229 35	17B	FO2200	J1229 41	22B	FO2200	J1229 48	22A	FO2200
	J1327 72	34A	FO2602						
KLGSTJ	*J1218 43	23B	FO2200	J1230 17	09B	FO2200			
KLSBA2X	*J1119 06	03A	FO5202	J1314 33	16A	FO5203			
KLSBB2X	*J1119 22	11A	FO5202	J1314 34	15B	FO5203			
KLSDLTA	*J1314 55	27B	FO2200	J1229 37	18B	FO2200			
KLSDLTB	*J1314 61	31B	FO2200	J1229 50	23A	FO2200			
KLSDLTC	*J1314 60	28A	FO2200	J1229 43	23B	FO2200			
KLSDLTD	*J1314 63	31A	FO2200	J1225 36	17A	FO2200			
KLSDMTA	*J1314 73	34B	FO2200	J1124 71	35B	FO2200			
KLSDMTB	*J1314 79	37B	FO2200	J1220 07	05B	FO2200			
KLSDMTC	*J1314 74	36A	FO2200	J1227 75	37B	FO2200			
KLSDMTD	*J1314 80	38B	FO2200	J1218 46	21A	FO2200			
KLSSPA	*J1233 59	31B	FO2000	J1227 77	38B	FO2200			
KLST0A	*J1229 39	19B	FO2200	J1124 55	29B	FO2200	J1228 41	22B	FO2200
KLST1A	*J1229 46	21A	FO2200	J1124 53	28B	FO2200	J1228 08	06A	FO2200
KLST2A	*J1229 45	24B	FO2200	J1124 57	28A	FO2200	J1228 53	28B	FO2200
KLST3A	*J1225 30	15A	FO2200	J1226 15	07B	FO2200			
KLST30V	*J1226 10	06B	FO2200	J1124 60	29A	FO2200			
KLST8A	*J1227 73	36B	FO2200	J1230 20	10A	FO2200			
KLST80V	*J1230 18	09A	FO2200	J1218 34	16A	FO2200			
KLST90V	*J1230 14	08B	FO2200	J1324 62	29A	FO2200			
KLS0CJ	*J1218 31	15B	FO2200	J1324 68	32A	FO2200			
KLV1D0	*J1129 80	39A	FO2200	J02 31		FO2200	J1119 18	09A	FO5202
KL0A00	*J1228 45	24B	FO2200	J1223 04	04A	FO2200	J1324 40	19A	FO2200
KL0A10	*J1228 06	05A	FO2200	J1324 34	16A	FO2200			
KL0A20	*J1228 57	30B	FO2200	J1223 07	03A	FO2200	J1324 29	14B	FO2200
KL0FFJ	*J1219 37	18B	FO2200	J1220 78	38A	FO2200			

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution								
KL0FFJQ	*J1220 80	39A	FO2200	J1224 13	06B	FO2200	J1224 20	11A	FO2200
	J1228 71	36A	FO2200						
KL0FFKQ	*J1220 79	39B	FO2200	J1124 78	38A	FO2200	J1218 08	06A	FO2200
	J1218 41	22B	FO2200	J1227 79	39B	FO2200			
KL0NNA	*J1224 14	09A	FO2200	J1220 05	04B	FO2200			
KL0X01E	*J1124 61	31B	FO2200	J1228 43	23B	FO2200			
KL0X11E	*J1124 65	33B	FO2200	J1228 10	07A	FO2200			
KL0X12E	*J1124 68	33A	FO2200	J1228 55	29B	FO2200			
KL0X13E	*J1124 64	31A	FO2200	J1134 71	36A	FO2200	J1324 35	17B	FO2200
KL0X20E	*J1124 75	37B	FO2200	J1324 54	25A	FO2200			
KL0X21E	*J1124 79	39B	FO2200	J1324 48	22A	FO2200			
KL0X23E	*J1124 76	37A	FO2200	J1324 47	25B	FO2200			
KL000D4	*J1324 38	18A	FO2200	J02 19		FO2200	J1119 03	02B	FO5202
KL001D4	*J1324 30	15A	FO2200	J02 21		FO2200	J1119 05	03B	FO5202
	J1223 05	03B							
KL002D4	*J1324 33	16B	FO2200	J02 25		FO2200	J1119 07	04B	FO5202
KL003D4	*J1324 39	19B	FO2200	J02 27		FO2200	J1119 09	05B	FO5202
KL004D4	*J1324 52	24A	FO2200	J02 28		FO2200	J1119 11	06B	FO5202
KL005D4	*J1324 46	21A	FO2200	J02 30		FO2200	J1119 15	07B	FO5202
KL007D4	*J1324 51	27B	FO2200	J02 33		FO2200	J1119 17	08B	FO5202
KL008D4	*J1324 66	31A	FO2200	J02 34		FO2200	J1119 19	09B	FO5202
KL009D4	*J1324 60	28A	FO2200	J02 36		FO2200	J1119 21	01B	FO5202
KMRESD4	*J1232 80	39A	FO5300						
KMRSTB4	*J1232 72	34A	FO5300	*J1232 80	39A	FO5300	J1102 72	34A	FO2400
	J1103 21	10B	FO3500	J1103 33	16B	FO3601	J1128 73	36B	FO4401
	J1134 73	36B	FO2800	J1213 49	24B	FO1901	J1213 66	32B	FO2900
	J1214 35	16B	FO1901	J1214 49	24B	FO2900	J1214 66	32B	FO1901
	J1215 49	24B	FO2900	J1215 66	32B	FO2900	J1216 49	24B	FO2900
	J1216 66	32B	FO2900	J1218 04	04A	FO2200	J1219 50	23A	FO2800
	J1219 64	30A	FO2800	J1220 17	09B	FO2800	J1220 31	15B	FO2800
	J1220 70	34A	FO2200	J1231 48		FO5300	J1318 33		FO2800
KMRSTD4	*J1232 72	34A	FO5300						
KMWRK0	*J1228 66	31A	FO5403	J1329 01		FO1702	J1330 01		FO1702
KNORMA	*J1129 51	27B	FO2602	J1128 20	11A	FO2602	J1234 11	07A	FO2602
KNORM0V	*J1234 13	06A	FO2602	J1223 61	32B	FO2602	J1229 47	25B	FO2400
KORLDA	*J1229 22	12A	FO2601	J1230 38	20A	FO1602			

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution								
KORLD0V	*J1230 40	19A	FO1602	J1319 79		FO1602	J1320 79		FO1602
	J1321 79		FO1603	J1322 79		FO1604			
KORSB0V	*J1226 03	03A	FO1602	J1319 63		FO1602	J1320 63		FO1602
	J1321 63		FO1603	J1322 63		FO1604			
KORSHA	*J1227 55	29B	FO1602	J1226 17	09B	FO1602			
KORSH0V	*J1226 14	08B	FO1602	J1319 78		FO1602	J1320 78		FO1602
	J1321 78		FO1603	J1322 78		FO1604			
KORSIA	*J1228 22	12A	FO1602	J1230 27	13B	FO1602			
KORSI0V	*J1230 26	12B	FO1602	J1319 39		FO1602			
KPACB0	*J1227 64	30A	FO1901	J1229 03	02A	FO1901			
KPACC0	*J1233 47	25B	FO1901	J1213 61	31B	FO1901	J1214 47	23A	FO1901
	J1214 79	37B	FO1901						
KPACLA	*J1229 09	04B	FO1901	J1213 63	31A	FO1901	J1214 50	24A	FO1901
	J1214 80	38B	FO1901						
KPAC11U	*J1214 38	18A	FO1901	J1211 35	16B	FO5203	J1229 53	28B	FO1901
	J1319 51		FO1801						
KPAC12U	*J1214 40	19A	FO1901	J1211 37	17B	FO5203	J1229 59	31B	FO1901
	J1319 34		FO1801						
KPAC13U	*J1214 42	20A	FO1901	J1211 39	18B	FO5203	J1229 77	38B	FO1901
	J1319 46		FO1801						
KPAC14U	*J1214 46	21A	FO1901	J1211 41	19B	FO5203	J1229 71	36A	FO1901
	J1319 14		FO1801						
KPAC15U	*J1214 36	17A	FO1901	J1213 64	30A	FO1901			
KPAC21U	*J1213 54	26A	FO1901	J1211 43	22B	FO5203	J1229 65	34B	FO1901
	J1320 51		FO1802						
KPAC22U	*J1213 56	28B	FO1901	J1211 45	23B	FO5203	J1229 76	37A	FO1901
	J1320 34		FO1802						
KPAC23U	*J1213 60	28A	FO1901	J1211 47	23A	FO5203	J1216 20	10A	FO1901
	J1320 46		FO1802						
KPAC24U	*J1213 62	29A	FO1901	J1211 50	24A	FO5203	J1216 22	11A	FO1901
	J1320 14		FO1802						
KPAC25U	*J1213 52	25A	FO1901	J1214 78	38A	FO1901			
KPAC31U	*J1214 70	34A	FO1901	J1118 19	09B	FO5203	J1216 19	09B	FO1901
	J1321 51		FO1802						
KPAC32U	*J1214 72	35A	FO1901	J1118 21	10B	FO5203	J1321 34		FO1802
KPADC0T	*J1216 24	12A	FO1901	J1224 68	32A	FO1901			

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution							
KPADC1T	*J1216 26	13A	FO1901	J1224 62	29A	FO1901		
KPADC2T	*J1216 27	14A	FO1901	J1224 53	28B	FO1901		
KPADC3T	*J1216 30	15A	FO1901	J1224 59	31B	FO1901		
KPADC4T	*J1216 33	16A	FO1901	J1224 77	38B	FO1901		
KPADC5T	*J1216 23	11B	FO1901	J1224 71	36A	FO1901		
KPADC6T	*J1216 25	12B	FO1901	J1224 65	34B	FO1901		
KPADC7T	*J1216 29	13B	FO1901	J1224 76	37A	FO1901		
KPAD00	*J1224 66	31A	FO1901	J1315 29		FO1901	J1316 29	FO1902
KPAD10	*J1224 60	28A	FO1901	J1315 31		FO1901	J1316 31	FO1902
KPAD20	*J1224 57	30B	FO1901	J1315 80		FO1901	J1316 80	FO1902
KPAD30	*J1224 63	33B	FO1901	J1315 43		FO1901	J1316 43	FO1902
KPAD40	*J1224 75	37B	FO1901	J1315 27		FO1901	J1316 27	FO1902
KPAD50	*J1224 72	34A	FO1901	J1315 48		FO1901	J1316 48	FO1902
KPAD60	*J1224 60	35A	FO1901	J1315 63		FO1901	J1316 63	FO1902
KPAD70	*J1224 80	39A	FO1901	J1315 17		FO1901	J1316 17	FO1902
KPA0BA	*J1229 57	30B	FO1901	J1315 08		FO1901	J1315 38	FO1901
	J1315 60		FO1901	J1316 08		FO1902	J1316 38	FO1902
	J1316 60		FO1902					
KPA1BA	*J1229 63	33B	FO1901	J1315 09		FO1901	J1315 35	FO1901
	J1315 61		FO1901	J1316 09		FO1902	J1316 35	FO1902
	J1316 61		FO1902					
KPA2BA	*J1229 75	37B	FO1901	J1315 10		FO1901	J1315 39	FO1901
	J1315 62		FO1901	J1316 10		FO1902	J1316 39	FO1902
	J1316 62		FO1902					
KPA3BA	*J1229 72	34A	FO1901	J1315 18		FO1901	J1315 36	FO1901
	J1315 64		FO1901	J1316 18		FO1902	J1316 36	FO1902
	J1316 64		FO1902					
KPA4BA	*J1229 69	35A	FO1901	J1315 23		FO1901	J1315 40	FO1901
	J1315 70		FO1901	J1316 23		FO1902	J1316 40	FO1902
	J1316 70		FO1902					
KPA5BA	*J1229 80	39A	FO1901	J1315 24		FO1901	J1315 37	FO1901
	J1315 72		FO1901	J1316 24		FO1902	J1316 37	FO1902
	J1316 72		FO1902					
KPML100B	*J1315 59		FO1901					
KPML101B	*J1315 57		FO1901					
KPML102B	*J1315 56		FO1901					

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal		Distribution
KPML103B	*J1315 55	FO1901
KPML104B	*J1315 65	FO1901
KPML105B	*J1315 66	FO1901
KPML106B	*J1315 68	FO1901
KPML107B	*J1315 69	FO1901
KPML140B	*J1315 13	FO1901
KPML141B	*J1315 11	FO1901
KPML142B	*J1315 15	FO1901
KPML143B	*J1315 14	FO1901
KPML144B	*J1315 22	FO1901
KPML145B	*J1315 19	FO1901
KPML146B	*J1315 21	FO1901
KPML147B	*J1315 20	FO1901
KPML150B	*J1315 46	FO1901
KPML151B	*J1315 47	FO1901
KPML152B	*J1315 74	FO1901
KPML153B	*J1315 75	FO1901
KPML154B	*J1315 76	FO1901
KPML155B	*J1315 77	FO1901
KPML156B	*J1315 78	FO1901
KPML157B	*J1315 79	FO1901
KPML160B	*J1315 49	FO1901
KPML161B	*J1315 50	FO1901
KPML162B	*J1315 51	FO1901
KPML163B	*J1315 52	FO1901
KPML164B	*J1316 53	FO1901
KPML165B	*J1315 54	FO1901
KPML166B	*J1315 71	FO1901
KPML167B	*J1315 73	FO1901
KPML170B	*J1315 01	FO1901
KPML171B	*J1315 03	FO1901
KPML172B	*J1315 04	FO1901
KPML173B	*J1315 05	FO1901
KPML174B	*J1315 06	FO1901
KPML175B	*J1315 07	FO1901
KPML176B	*J1315 25	FO1901

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal		Distribution
KPML177B	*J1315 26	FO1901
KPMM100B	*J1316 59	FO1902
KPMM101B	*J1316 57	FO1902
KPMM102B	*J1316 56	FO1902
KPMM103B	*J1316 55	FO1902
KPMM104B	*J1316 65	FO1902
KPMM105B	*J1316 66	FO1902
KPMM106B	*J1316 68	FO1902
KPMM107B	*J1316 69	FO1902
KPMM140B	*J1316 13	FO1902
KPMM141B	*J1316 11	FO1902
KPMM142B	*J1316 15	FO1902
KPMM143B	*J1316 14	FO1902
KPMM144B	*J1316 22	FO1902
KPMM145B	*J1316 19	FO1902
KPMM146B	*J1316 21	FO1902
KPMM147B	*J1316 20	FO1902
KPMM150B	*J1316 46	FO1902
KPMM151B	*J1316 47	FO1902
KPMM152B	*J1316 74	FO1902
KPMM153B	*J1316 75	FO1902
KPMM154B	*J1316 76	FO1902
KPMM155B	*J1316 77	FO1902
KPMM156B	*J1316 78	FO1902
KPMM157B	*J1316 79	FO1902
KPMM160B	*J1316 49	FO1902
KPMM161B	*J1316 50	FO1902
KPMM162B	*J1316 51	FO1902
KPMM163B	*J1316 52	FO1902
KPMM164B	*J1316 53	FO1902
KPMM165B	*J1316 54	FO1902
KPMM166B	*J1316 71	FO1902
KPMM167B	*J1316 73	FO1902
KPMM170B	*J1316 01	FO1902
KPMM171B	*J1316 03	FO1902
KPMM172B	*J1316 04	FO1902

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution							
KPMM173B	*J1316 05		FO1902					
KPMM174B	*J1316 06		FO1902					
KPMM175B	*J1316 07		FO1902					
KPMM176B	*J1316 25		FO1902					
KPMM177B	*J1316 26		FO1902					
KP100B	*J1315 01		FO1901	*J1315 13	FO1901	*J1315 46		FO1901
	*J1315 49		FO1901	*J1315 59	FO1901	J1209 62	29A	FO1902
	J1210 19	09B	FO5203					
KP101B	*J1315 03		FO1901	*J1315 11	FO1901	*J1315 47		FO1901
	*J1315 50		FO1901	*J1315 57	FO1901	J1209 54	26A	FO1902
	J1210 21	10B	FO5203					
KP102B	*J1315 04		FO1901	*J1315 15	FO1901	*J1315 51		FO1901
	*J1315 56		FO1901	*J1315 74	FO1901	J1209 57	29B	FO1902
	J1210 23	11B	FO5203					
KP103B	*J1315 05		FO1901	*J1315 14	FO1901	*J1315 52		FO1901
	*J1315 55		FO1901	*J1315 75	FO1901	*J1209 51	25B	FO1902
	J1210 25	12B	FO5203					
KP104B	*J1315 06		FO1901	*J1315 22	FO1901	*J1315 53		FO1901
	*J1315 65		FO1901	*J1315 76	FO1901	J1209 76	37A	FO1902
	J1210 29	13B	FO5203					
KP105B	*J1315 07		FO1901	*J1315 19	FO1901	*J1315 54		FO1901
	*J1315 66		FO1901	*J1315 77	FO1901	J1209 70	34A	FO1902
	J1210 31	14B	FO5203					
KP106B	*J1315 21		FO1901	*J1315 25	FO1901	*J1315 68		FO1901
	*J1315 71		FO1901	*J1315 78	FO1901	J1209 75	35B	FO1902
	J1210 34	15B	FO5203					
KP107B	*J1315 20		FO1901	*J1315 26	FO1901	*J1315 69		FO1901
	*J1315 73		FO1901	*J1315 79	FO1901	J1209 69	32A	FO1902
	J1210 33	16A	FO5203					
KP108B	*J1316 01		FO1902	*J1316 13	FO1902	*J1316 46		FO1902
	*J1316 49		FO1902	*J1316 59	FO1902	J1210 35	16B	FO5203
	J1210 62	29A	FO1902					
KP109B	*J1316 03		FO1902	*J1316 11	FO1902	*J1316 47		FO1902
	*J1316 50		FO1902	*J1316 57	FO1902	J1210 37	17B	FO5203
	J1210 54	26A	FO1902					
KP110B	*J1316 04		FO1902	*J1316 15	FO1902	*J1316 51		FO1902

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution								
	*J1316 56		FO1902	*J1316 74		FO 1902	J1210 39	18B	FO5203
	J1210 57	29B	FO1902						
KP111B	*J1316 05		FO1902	*J1316 14		FO1902	*J1316 52		FO1902
	*J1316 55		FO1902	*J1316 75		FO1902	J1210 41	19B	FO2203
	J1210 51	25B	FO1902						
KP112B	*J1316 06		FO1902	*J1316 22		FO1902	*J1316 53		FO1902
	*J1316 65		FO1902	*J1316 76		FO1902	J1210 43	22B	FO2203
	J1210 76	37A	FO1902						
KP113B	*J1316 07		FO1902	*J1316 19		FO1902	*J1316 54		FO1902
	*J1316 66		FO1902	*J1316 77		FO1902	J1210 45	23B	FO2203
	J1210 70	34A	FO1902						
KP114B	*J1316 21		FO1902	*J1316 25		FO1902	*J1316 68		FO1902
	*J1316 71		FO1902	*J1316 78		FO1902	J1210 47	23A	FO2203
	J1210 75	35B	FO1902						
KP115B	*J1316 20		FO1902	*J1316 26		FO1902	*J1316 69		FO1902
	*J1316 73		FO1902	*J1316 79		FO1902	J1210 50	24A	FO2203
	J1210 69	32A	FO1902						
KRBSEA	*J1223 33	16B	FO2602	J04 37		FO2602			
KRRDYAV	*J1230 34	15A	FO2502	J1313 14		FO2502			
KSDATHA	J1101 15	05B	FO2100	*J01 71		FO2100			
KSDATHC	*J1101 35	19B	FO2100	J1230 69	35B	FO2100	J1231 71		FO2100
KSDAT0V	*J1230 70	34B	FO2100	J1122 05	04B	FO2100			
KSDCA0V	*J1230 48	21A	FO2100	J1122 09	06B	FO2100	J1122 37	18B	FO2100
	J1122 63	32B	FO2100	J1123 23	12B	FO2100	J1123 49	26B	FO2100
	J1123 77	38B	FO2100						
KSDCB0V	*J1230 46	22B	FO2100	J1122 23	12B	FO2100	J1122 49	26B	FO2100
	J1122 77	38B	FO2100	J1123 09	06B	FO2100	J1123 37	18B	FO2100
	J1123 63	32B	FO2100						
KSDCPHA	J1101 48	31B	FO2100	*J01 70		FO2100			
KSDCPHB	*J1101 74	33A	FO2100	J1230 41	23B	FO2100	J1230 50	22A	FO2100
KSDP10E	*J1123 07	05B	FO2100	J1319 07		FO1801			
KSDP11E	*J1123 11	07B	FO2100	J1320 49		FO1802			
KSDP12E	*J1123 13	07A	FO2100	J1320 50		FO1802			
KSDP13E	*J1123 10	05A	FO2100	J132027		FO1802			
KSDP20E	*J1122 21	11B	FO2100	J1320 07		FO1802			
KSDP21E	*J1122 27	13B	FO2100	J1321 49		FO1802			

Table 5-8. Right Hand Assembly Key Signal Lookup --Continued

Signal	Distribution								
KSDP22E	*J1122 25	14A	FO2100	J1321 50		FO1802			
KSDP23E	*J1122 24	12A	FO2100	J1321 27		FO1802			
KSDP30E	*J1123 35	17B	FO2100	J1321 07		FO1802			
KSDP31E	*J1123 39	19B	FO2100	J1322 49		FO1802			
KSDP32E	*J1123 42	20A	FO2100	J1322 50		FO1802			
KSDP33E	*J1123 38	18A	FO2100	J1322 27		FO1802			
KSDP40E	*J1122 47	25B	FO2100	J1319 13		FO1801			
KSDP41E	*J1122 51	27B	FO2100	J1320 57		FO1802			
KSDP42E	*J1122 56	26A	FO2100	J1320 43		FO1802			
KSDP43E	*J1122 52	24A	FO2100	J1320 30		FO1802			
KSDP50E	*J1123 61	31B	FO2100	J1320 13		FO1802			
KSDP51E	*J1123 65	33B	FO2100	J1321 57		FO1802			
KSDP52E	*J1123 68	33A	FO2100	J1321 43		FO1802			
KSDP53E	*J1123 64	31A	FO2100	J1321 30		FO1802			
KSDP60E	*J1122 75	37B	FO2100	J1321 13		FO1802			
KSDP61E	*J1122 79	39B	FO2100	J1322 57		FO1802			
KSDP62E	*J1122 80	39A	FO2100	J1322 43		FO1802			
KSDP63E	*J1122 76	37A	FO2100	J1322 30		FO1802			
KSDS10E	*J1122 07	05B	FO2100	J1123 03	03B	FO2100			
KSDS11E	*J1122 11	07B	FO2100	J1123 01	02B	FO2100			
KSDS12E	*J1122 13	07A	FO2100	J1123 04	02A	FO2100			
KSDS13E	*J1122 10	05A	FO2100	J1123 06	03A	FO2100	J1123 19	10B	FO2100
KSDS20E	*J1123 21	11B	FO2100	J1122 17	09B	FO2100			
KSDS21E	*J1123 27	13B	FO2100	J1122 15	08B	FO2100			
KSDS22E	*J1123 25	14A	FO2100	J1122 18	09A	FO2100			
KSDS23E	*J1123 24	12A	FO2100	J1122 20	10A	FO2100	J1122 33	16B	FO2100
KSDS30E	*J1122 35	17B	FO2100	J1123 31	15B	FO2100			
KSDS31E	*J1122 39	19B	FO2100	J1123 29	14B	FO2100			
KSDS32E	*J1122 42	20A	FO2100	J1123 30	15A	FO2100			
KSDS33E	*J1122 38	18A	FO2100	J1123 34	16A	FO2100	J1123 45	24B	FO2100
KSDS40E	*J1123 47	25B	FO2100	J1122 43	23B	FO2100			
KSDS41E	*J1123 51	27B	FO2100	J1122 41	22B	FO2100			
KSDS42E	*J1123 56	26A	FO2100	J1122 46	21A	FO2100			
KSDS43E	*J1123 52	24A	FO2100	J1122 48	22A	FO2100	J1122 59	30B	FO2100
KSDS50E	*J1122 61	31B	FO2100	J1123 55	29B	FO2100			
KSDS51E	*J1122 65	33B	FO2100	J1123 53	28B	FO2100			

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution								
KSDS52E	*J1122 68	33A	FO2100	J1123 57	28A	FO2100			
KSDS53E	*J1122 64	31A	FO2100	J1123 60	29A	FO2100	J1123 73	36B	FO2100
KSDS60E	*J1123 75	37B	FO2100	J1122 71	35B	FO2100			
KSDS61E	*J1123 79	39B	FO2100	J1122 69	34B	FO2100			
KSDS62E	*J1123 80	39A	FO2100	J1122 70	34A	FO2100			
KSDS63E	*J1123 76	37A	FO2100	J1122 72	35A	FO2100			
KSKBWA	*J1127 31	15B	FO2602	J1223 18	10A	FO2602	J1233 50	23A	FO1901
KSKDFA	J1233 48	22A	FO1901	*J1317 62		FO1604			
KSKDIA	*J1127 55	29B	FO2602	J1233 31	15B	FO2602	J1233 46	21A	FO1901
KSKMCA	J1223 14	09A	FO2602	J1233 49	26B	FO1901	*J1317 45		FO2602
KSKTSA	*J1127 64	30A	FO2601	J1233 30	15A	FO2602	J1233 43	23B	FO1901
KSLSTB4	*J1324 75	37B	FO2502	J05 01		FO3500	J1103 37	18B	FO3601
	J1106 18	10A	FO3500	J1131 48		FO2502			
KSLSTD4	*J1324 75	37B	FO2502						
KSPCSJ	*J1219 78	38A	FO2100	J1322 07		FO1802	J1322 13		FO1802
KSTFL0	J1103 61	32B	FO2601	J1127 66	31A	FO2601	*J1313 80		FO2502
KSTRBHA	*J1101 40	31A	FO2100	J01 68		FO2100			
KSTRBHC	*J1101 79	39A	FO2100	J1116 75	39A	FO2100	J1219 79	39B	FO2100
	J1323 05		FO2100						
KSTRB0V	*J1116 77	38A	FO2100	J1122 26	13A	FO2100	J1122 54	25A	FO2100
	J1122 78	38A	FO2100	J1123 14	06A	FO2100	J1123 40	19A	FO2100
	J1123 66	32A	FO2100	J1219 77	38B	FO2100			
KSWAC0V	*J1226 53	26B	FO2501	J1102 66	31A	FO3402	J1104 07	03A	FO3602
	J1112 07	03A	FO3603						
KSWD7K	*J1109 69	35A	FO2502	J1324 77	38B	FO2502			
KSW06D4	*J1324 06	05A	FO2502	J04 32		FO2502			
KSW06K	*J1313 21		FO2502	J1324 08	06A	FO2502			
KSW07D4	*J1324 01	02B	FO2502	J04 33		FO2502			
KSW07J	J1109 71	36A	FO2502	*J1313 26		FO2502	J1324 79	39B	FO2502
KSW07K	J1106 79	39B	FO3601	J1109 72	34A	FO2502	*J1313 19		FO2502
	J1324 04	04A	FO2502						
KSW08D4	*J1324 09	04B	FO2502	J04 4		FO2502			
KSW08K	*J1313 11		FO2502	J1324 03	02A	FO2502			
KTCNMA	*J1229 51	27B	FO2400	J1129 56	26A	FO2400			
KTCSHAV	*J1226 71	36B	FO2400	J1129 54	25A	FO2400			
KTCSH0	*J1224 22	12A	FO2400	J1226 73	37B	FO2400			

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution								
KT1FFJ	*J1218 25	12B	FO2400	J1225 48	22A	FO2601	J1225 54	25A	FO2400
KT1FFK	*J1218 23	IB	FO2400	J1225 47	25B	FO2400			
KT1FNA	*J1225 46	21A	FO2601	J1228 07	03A	FO2601			
KT1G0A	*J1227 51	27B	FO2602	J1103 76	37A	FO2602	J1226 64	33A	FO2602
KT1G00V	*J1226 66	32A	FO2602	J1223 54	25A	FO2602	J1225 10	07A	FO2601
	J1227 35	17B	FO2601	J1228 40	19A	FO2601	J1228 78	38A	FO2601
	J1229 05	03B	FO2602						
KT1NBA	*J1225 52	24A	FO2400	J1226 61	31A	FO2400			
KT1NB0V	*J1226 63	30A	FO2400	J1103 69	35A	FO2602	J1227 45	24B	FO2602
	J1317 54		FO2700						
KT1NH0	*J1228 09	04B	FO2601	J1102 79	39B	FO2602	J1233 71	36A	FO2602
KT1VBA	*J1102 76	37A	FO2602	J1224 37	18B	FO2602			
KT1VB0	*J1224 39	19B	FO2602	J1128 47	25B	FO2400	J1225 35	17B	FO2601
	J1225 70	33A	FO2400	J1228 05	03B	FO2601	J1229 07	03B	FO1901
	J1229 11	05B	FO2601	J1229 26	14A	FO2601			
KT1WTA	*J1103 80	39A	FO2602	J1102 77	38B	FO2602	J1127 49	26B	FO2602
	J1226 09	05B	FO2602	J1233 73	36B	FO2602			
KT1WT0V	*J1226 07	04B	FO2602	J1223 34	16A	FO2602			
KT2FFJ	*J1218 19	09B	FO2400	J1127 30	15A	FO2602	J1128 18	10A	FO2602
	J1128 68	32A	FO2400	J1223 66	31A	FO2602	J1224 40	19A	FO2400
	J1225 41	22B	FO2400	J1227 01	02B	FO1602	J1227 22	12A	FO2400
	J1317 18		FO1604	J1317 18		FO2602			
KT2FFK	*J1218 21	10B	FO2400	J1225 49	26B	FO2400			
KT2FJA	*J1128 51	27B	FO2400	J1227 40	19A	FO2400			
KT2FJ0	*J1227 36	17A	FO2400	J1218 18	10A	FO2400	J1218 26	14A	FO2400
KT2NBA	*J1128 66	31A	FO2400	J1234 52	26A	FO2400			
KT2NB0V	*J1234 54	25A	FO2400	J1223 38	18A	FO2601			
KT2NMA	*J1128 14	09A	FO2602	J1129 29	14B	FO2602			
KT2SF0	*J1129 33	16B	FO2602	J1227 34	16A	FO1602	J1227 62	29A	FO1602
KT2XBA	*J1225 45	24B	FO2400	J1102 74	35B	FO2400	J1226 55	29B	FO2400
	J1317 24		FO2700						
KT2XB0V	*J1226 56	28B	FO2400	J1228 36	17A	FO2601			
KVTCSAV	*J1230 07	04B	FO2602	J1223 31	15B	FO2602			
KVTCS0	*J1327 74	35B	FO2602	J1230 09	05B	FO2602			
KWFNIA	*J1127 63	33B	FO2602	J1102 78	38A	FO2602	J1103 78	38A	FO2602
	J1227 49	26B	FO2602	J1233 75	37B	FO2602			

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution								
KWTXHA	*J1103 63	33B	FO2601	J1228 03	02A	FO2601			
KXBSTA	*J1111 59	31B	FO2300	J1225 13	06B	FO2300	J1227 68	32A	FO1901
	J1234 74	35A	FO2300	J1317 41		FO2700	J1318 68		FO1701
KXBST0V	*J1234 72	34A	FO2300	J1228 42	20A	FO2601			
KXBWT0	J1127 29	14B	FO2602	*J1317 13		FO2602			
KXCBAA	*J1233 11	05B	FO2300	J1225 40	19A	FO2300			
KXCBA0	*J1225 38	18A	FO2300	J1317 23		FO1601			
KXDFS0V	*J1234 78	36A	FO2601	J1228 34	16A	FO2601			
KXDIS0V	*J1226 25	11A	FO2602	J1127 62	29A	FO2602	J1229 04	04A	FO2602
KXFHB0	*J1224 33	16B	FO2601	J1127 57	30B	FO2602	J1228 04	04A	FO2601
KXFHRA	*J1233 23	11B	FO1902	J1224 31	15B	FO2601			
KXFTA0	*J1227 19	09B	FO2601	J1225 37	18B	FO2601			
KXFTH0	*J1225 22	12A	FO2601	J1127 47	25B	FO2602			
KXFT10	*J1224 30	15A	FO2601	J1229 13	06B	FO2601			
KXFT00	*J1228 14	09A	FO2601	J1229 24	13A	FO2601			
KXRSW0V	*J1234 70	34B	FO2601	J1225 08	06A	FO2601			
KXSHF0V	*J1234 46	22B	FO2601	J1129 47	25B	FO2602	J1211 49	24B	FO2400
	J1224 26	14A	FO2400	J1225 68	32A	FO2400	J1227 03	02A	FO1602
	J1227 06	05A	FO1604	J1227 29	14B	FO1602	J1227 53	28B	FO1602
	J1228 61	32B	FO2602						
KXSSW0V	*J1234 60	28A	FO2601	J1228 76	37A	FO2601			
KXS03AV	*J1230 01	02B	FO2602	J1327 65	34B	FO2602			
KXS030	*J1223 69	35A	FO2501	J1230 05	03B	FO2602	J1313 51		FO2502
KXS04AV	*J1226 72	34A	FO2501	J1313 49		FO2502			
KXS040	*J1227 15	07B	FO2501	J1226 74	35A	FO2501			
KXTCFAV	*J1234 77	38A	FO2400	J1215 47	23A	FO2400	J1224 24	13A	FO2400
KXTCF0	*J1129 52	24A	FO2400	J1224 42	20A	FO2400			
KXTCITA	*J1211 55	27B	FO2400	J1215 45	23B	FO2400			
KXTCITB	*J1211 61	31B	FO2400	J1215 43	22B	FO2400			
KXTCITC	*J1211 60	28A	FO2400	J1215 41	19B	FO2400			
KXTCITD	*J1211 63	31A	FO2400	J1215 39	18B	FO2400			
KXTCLA	*J1225 66	31A	FO2400	J1215 50	24A	FO2400			
KXTCT5U	*J1215 36	17A	FO2400	J1234 75	39A	FO2400			
KXTFFJ	*J1218 37	18B	FO2400	J1225 43	23B	FO2400			
KXTFFK	*J1218 35	17B	FO2400	J1128 70	33A	FO2400	J1225 56	26A	FO2400
	J1227 24	13A	FO2400						

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution								
KXTFJ0	*J1225 33	16B	FO2400	J1218 40	19A	FO2400			
KXTJ1A	*J1223 47	25B	FO2602	J1102 75	37B	FO2602	J1127 45	24B	FO2602
	J1225 29	14B	FO2400	J1233 74	35B	FO2602			
KXTJ2A	*J1227 20	11A	FO2400	J1225 03	02A	FO2400	J1225 31	15B	FO2400
KXTLSA	*J1223 57	30B	FO2300	J1219 40	19A	FO2000	J1230 76	37A	FO2200
	J1329 04		FO1702	J1330 04		FO1702			
KXTLS0V	*J1230 78	36A	FO2200	J1219 42	20A	FO2200	J1220 74	36A	FO2200
KXTSWAV	*J1226 24	13A	FO2602	J1127 76	37A	FO2602	J1225 25	12B	FO2602
KXTSW0	*J1228 75	37B	FO2601	J1127 70	33A	FO2601	J1226 22	14A	FO2602
KXTXHA	*J1229 60	28A	FO2601	J1225 50	23A	FO2601			
KXTXSA	*J1229 14	09A	FO2601	J1111 71	36A	FO2601	J1217 78	38A	FO2501
	J1228 77	38B	FO2601						
KXTXS0	*J1128 69	35A	FO2601	J1103 57	30B	FO2601	J1229 18	10A	FO2601
	J1229 62	29A	FO2601						
KX1BI0	*J1225 15	07B	FO2300	J1127 78	38A	FO2602	J1318 35		FO1701
KX1CGA	*J1223 23	11B	FO2601	J1225 23	11B	FO2602			
KX1CM0	*J1225 27	13B	FO2602	J1223 49	26B	FO2602			
KX1FIA	*J1127 80	39A	FO2602	J123334	16A	FO2602			
KX1NC0	*J1233 35	17B	FO2602	J1223 52	24A	FO2602			
KX2NC0	*J1223 21	10B	FO2602	J1227 26	14A	FO2400			
KZRQ40E	*J1130 75	37B	FO2300	J1111 61	32B	FO2300	J1223 79	39B	FO2300
KZRQ41E	*J1130 79	39B	FO2300	J1111 60	28A	FO2300	J1223 60	28A	FO2300
	J1223 78	38A	FO2300						
KZRQ42E	*J1130 80	39A	FO2300	J1111 55	29B	FO2300	J1223 77	38B	FO2300
K0P12AV	*J1230 77	38A	FO1604	J1223 50	23A	FO1604			
K0P13AV	*J1230 53	26B	FO1604	J1223 46	21A	FO1604	J1223 70	33A	FO2602
K0R1SAV	*J1226 78	36A	FO1601	J1317 37		FO1601			
K10MZ0	*J1224 45	24B	FO5403	J1212 51	25B	FO5403	J1212 62	30A	FO5403
	J1225 61	32B	FO5403	J1225 77	38B	FO5403			
K12130	*J1223 45	24B	FO1604	J1229 49	26B	FO2400			
K5MIDA	*J1225 63	33B	FO5403	J1222 13	06B	FO5403			
K5MID04	*J1222 11	05B	FO5403	J1220 20	10A	FO2800	J1220 72	35A	FO2200
	J1318 36		FO2800	J1323 07		FO5403	J1323 08		FO5403
K5MZA04	*J1222 09	04B	FO5403	J1106 65	34B	FO3601	J1114 66	31A	FO4502
	J1124 09	06B	FO4600	J1130 09	06B	FO4600	J1134 06	05A	FO4200
	J1218 06	05A	FO2200	J1219 38	18A	FO2200	J1220 06	03A	FO2200

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution								
	J1323 09		FO5403	J1323 10		FO5403	J1114 66	31A	FO4102
K5MZBAH	*J1212 61	31B	FO5403	J1213 69	32A	FO2900	J1214 51	25B	FO2900
	J1215 51	25B	FO2900	J1215 69	32A	FO2900	J1216 51	25B	FO2900
	J1313 36		FO2502	J1319 05		FO1602	J1320 05		FO1602
	J1321 05		FO1603	J1322 05		FO1604			
K5MZB04	*J1222 21	10B	FO5403	J1110 75	37B	FO3601	J1114 75	37B	FO4200
	J1124 23	12B	FO4600	J1130 23	12B	FO4600	J1134 22	12A	FO4102
	J1218 22	12A	FO2400	J1219 52	24A	FO4200	J1220 34	16A	FO2800
	J1323 17		FO5403	J1323 19		FO5403			
K5MZCAH	*J1212 64	31A	FO5403	J1216 69	32A	FO2900	J1222 04	04A	FO5403
	J1222 20	11A	FO5403	J1222 25	12B	FO5403	J1222 64	30A	FO5403
	J1224 23	11B	FO5403	J1228 29	14B	FO5403	J1228 70	33A	FO5403
	J1311 64		FO3002	J1312 64		FO3002			
K5MZC04	*J1222 23	11B	FO5403	J1124 49	26B	FO4300	J1124 63	32B	FO2200
	J1130 37	18B	FO4102	J1130 49	26B	FO3601	J1131 25		FO5403
	J1131 26		FO5403	J1134 38	18A	FO2200	J1218 38	18A	FO2200
	J1219 66	31A	FO2800						
K5MZD0	*J1224 27	13B	FO5403	J1130 63	32B	FO2200	J113077	38B	FO2300
	J1217 09	06B	FO1902	J1219 23	12B	FO1902	J1217 37	18B	FO1902
	J1217 49	26B	FO1902	J1220 48	22A	FO2300	J1220 60	29A	FO2300
K5MZE04	*J1222 57	30B	FO5403	J1124 77	38B	FO2200	J1129 65	34B	FO4502
	J1131 23		FO5403	J1131 24		FO5403	J1134 52	24A	FO4102
	J1217 63	32B	FO3601	J1217 77	38B	FO2501	J1218 52	24A	FO2200
	J1219 75	37B	FO2100						
K5MZGO	*J1228 33	16B	FO5403	J1134 66	31A	FO4200	J1134 75	37B	FO2800
	J1134 75		FO2200						
K5SQFAV	*J1230 56	28B	FO5403	J1329 06		FO1702	J1330 06		FO1702
LAD0B0E	*J05 21		FO3001	J1118 76	37A	FO3001	J1210 71	33B	FO1902
LAD0B1E	*J05 22		FO3001	J1118 70	34A	FO3001	J1210 77	36B	FO1902
LAD0B2E	*J05 23		FO3001	J1118 75	35B	FO3001	J1210 72	35A	FO1902
LAD0B3E	*J05 24		FO3001	J1118 69	32A	FO3001	J1210 78	38A	FO1902
LBD0B0E	*J05 25		FO3001	J1119 76	37A	FO3001	J1210 53	26B	FO1902
LBD0B1E	*J05 26		FO3001	J1119 70	34A	FO3001	J1210 59	30B	FO1902
LBD0B2E	*J05 27		FO3001	J1119 75	35B	FO3001	J1210 56	28B	FO1902
LBD0B3E	*J05 28		FO3001	J1119 69	32A	FO3001	J1210 64	30A	FO1902
LDBISA	*J05 58		FO3001	J1118 66	32B	FO3001	J1119 49	24B	FO3001

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution									
	J1119 66	32B	FO3001	J1120 66	32B	FO3001				
LDBLPAV	*J05 57		FO4900	J1228 56	26A	FO2800				
LDCG00	*J04 51		FO4900	J1127 53	28B	FO2602	J1127 61	32B	FO2602
	J1127 68	32A	FO2601	J1227 47	25B	FO2602	J1230 15	07B	FO2200
LDCRS0V	*J1230 71	36B	FO5300	J1132 05	03B	FO5300	J1232 71	36A	FO5300
	J1232 76	37A	FO5300	J1313 18		FO2502			
LENCB5T	*J03 46		FO5202	J1314 30	15A	FO5202	J1319 61		FO1602
	J1320 61		FO1602	J1321 61		FO1603	J1322 61		FO1604
LENCB6T	*J03 47		FO5202	J1314 48	22A	FO5202			
LENCB7T	*J03 45		FO5202	J1314 13	07A	FO5202			
LHCR1A	*J05 44		FO5202	J1128 17	08B	FO5202	J1128 24	13A	FO5202
LHCR2A	*J05 46		FO5202	J1128 23	11B	FO5202	J1128 29	14B	FO5202
LHCR3A	*J05 49		FO5202	J1128 35	17B	FO5202	J1128 40	19A	FO5202
	J1320 60		FO1602	J1322 60		FO 1604			
LHCR4A	*J03 48		FO5202	J1314 14	06A	FO5202	J1314 27	14A	FO5202
	J1314 46	21A	FO5202						
LRAVM1U	*J05 51		FO3500	J1102 14	09A	FO3500	J1213 04	02A	FO3500
LRAVM2U	*J05 52		FO3500	J1107 73	37B	FO3500	J1213 06	03A	FO3500
LRAVM3U	*J05 53		FO3500	J1107 69	35B	FO3500	J1213 03	02B	FO3500
LRAVM4U	*J05 54		FO3500	J1102 20	11A	FO3500	J1213 05	03B	FO3500
LRDSC0	*J05 37		FO1901	J1209 49	24B	FO1902	J1209 66	32B	FO1902
	J1210 49	24B	FO1902	J1210 66	32B	FO1902			
LTSB2AV	*J03 50		FO5202	J1314 08	04A	FO5202	J1314 24	12A	FO5202
	J1314 40	19A	FO5202						
LTSB3AV	*J03 49		FO5202	J1314 10	05A	FO5202	J1314 26	13A	FO5202
	J1314 42	20A	FO5202						
LTSEG0E	*J05 29		FO3001	J1119 62	29A	FO3001	J1209 71	33B	FO1902
LTSEG1E	*J05 30		FO3001	J1119 54	26A	FO3001	J1209 77	36B	FO1902
LTSEG2E	*J05 31		FO3001	J1119 57	29B	FO3001	J1209 72	35A	FO1902
LTSEG3E	*J05 32		FO3001	J1119 51	25B	FO3001	J1209 78	38A	FO1902
LTSFG0E	*J05 33		FO3001	J1120 76	37A	FO3001	J1209 53	26B	FO1902
LTSFG1E	*J05 34		FO3001	J1120 70	34A	FO3001	J1209 59	30B	FO1902
LTSFG2E	*J05 35		FO3001	J1120 75	35B	FO3001	J1209 56	28B	FO1902
LTSFG3E	*J05 36		FO3001	J1120 69	32A	FO3001	J1209 64	30A	FO1902
LVCTGD4	*J05 03		FO4900	J1103 49	26B	FO3402	J1105 41	22B	FO3500
	J1106 71	36A	FO3500	J1131 47		FO3500	J05 03		FO3402

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution								
RACAC0	*J1129 15	07B	FO4200	J1128 11	05B	FO4200			
RACUCA	*J1128 15	07B	FO4200	J1234 05	03B	FO4200			
RAMRM0	*AO3A 1		FO3100	J1302 07		FO3100			
RAMRM1	*A03A 2		FO3100	J1302 04		FO3100			
RAMRM2	*A03A 4		FO3100	J1302 10		FO3100			
RAMRM3	*A03A 8		FO3100	J1302 03		FO3100			
RAMUSJ	*J1134 61	32B	FO4200	J1129 13	06B	FO4200			
RAMUSK	*J1134 59	31B	FO4200	J1128 77	38B	FO4200			
RASB00E	*J1130 07	05B	FO4600	J1132 78	38A	FO4600			
RASB01E	*J1130 11	07B	FO4600	J1132 73	36B	FO4600			
RASB02E	*J1130 13	07A	FO4600	J1132 79	39B	FO4600			
RASB03E	*J1130 10	05A	FO4600	J1124 05	04B	FO4600	J1132 61	32B	FO4600
RASB10E	*J1124 07	05B	FO4600	J1132 55	29B	FO4600			
RASB11E	*J1124 11	07B	FO4600	J1132 64	30A	FO4600			
RASB12E	*J1124 13	07A	FO4600	J1132 70	33A	FO4600			
RASB13E	*J1124 10	05A	FO4600	J1130 19	10B	FO4600	J1132 49	26B	FO4600
RASB20E	*J1130 21	11B	FO4600	J1132 43	23B	FO4600			
RASB21E	*J1130 27	13B	FO4600	J1132 50	23A	FO4600			
RASB22E	*J1130 25	14A	FO4600	J1132 56	26A	FO4600			
RASB23E	*J1130 24	12A	FO4600	J1124 19	10B	FO4600	J113237	18B	FO4600
RASB30E	*J1124 21	11B	FO4600	J1132 31	15B	FO4600			
RASB31E	*J1124 27	13B	FO4600	J1132 36	17A	FO4600			
RASB32E	*J1124 25	14A	FO4600	J1132 42	20A	FO4600			
RASB33E	*J1124 24	12A	FO4600	J1132 74	35B	FO4600	J1133 39	19B	FO4600
	J1217 59	30B	FO3601						
RAS01D4	*J1132 28	18A	FO4600						
RAS02D4	*J1132 30	15A	FO4600						
RAS03D4	*J1132 33	16B	FO4600						
RAS04D4	*J1132 39	19B	FO4600						
RAS05D4	*J1132 52	24A	FO4600						
RAS06D4	*J1132 46	21A	FO4600						
RAS07D4	*J1132 45	24B	FO4600						
RAS08D4	*J1132 51	27B	FO4600						
RAS09D4	*J1132 66	31A	FO4600						
AS10D4	*J1132 60	28A	FO4600						
RAS11D4	*J1132 57	30B	FO4600						

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution										
RAS12D4	*J1132	63	33B	FO4600							
RAS13D4	*J1132	75	37B	FO4600							
RAS14D4	*J1132	72	34A	FO4600							
RAS33AV	*J1133	42	18B	FO4600	J1234	04	02A	FO4600			
RAS330V	*J1234	03	03A	FO4600	J04	09		FO4102	J1333	01	FO4101
RATELOV	*J1133	08	04A	FO4200	J1129	10	07A	FO4200	J1134	10	07A FO4200
RA401AF	J03	52		FO4102	*J1333	26		FO4101			
RA403AF	J03	53		FO4102	*J1333	13		FO4101			
RA411L	J03	54		FO4102	*J1333	25		FO4101			
RA412L	J03	55		FO4102	J04	55		FO4102	*J1333	15	FO4101
RBEGEK	*J1134	09	04B	FO4502	J04	43		FO4502	J1121	30	15A FO4502
RCEP1A	*J1127	43	23B	FO4502	J1125	47	23A	FO4502			
RCMDAA	*J1129	30	15A	FO4200	J1133	05	03B	FO4200			
RCMD1A	*J1129	39	19B	FO4200	J1128	59	31B	FO4502	J1133	20	10A FO4200
RCMSBA	*J1128	09	04B	FO4502	J1133	47	24A	FO4502			
RCMSWOV	*J1133	49	23A	FO4502	J1134	05	03B	FO4502			
RCPXAA	*J1101	41	26B	FO4501	J02	45		FO4501	J1131	08	FO4501
RCPX1A	*J1101	71	36B	FO4501	J1117	18		FO4502	J1125	37	17B FO4502
RCPYAA	*J1101	62	32A	FO4501	J02	50		FO4501	J1131	09	FO4501
RCPYBA	*J1101	73	38B	FO4501	J1117	39		FO4502	J1125	69	32A FO4502
RCRAA0V	*J1133	10	06B	FO4200	J1134	70	33A	FO4200			
RCRSTA	*J1129	38	18A	FO4102	J1134	20	11A	FO4102			
RCSETA	*J1129	01	02B	FO4102	J1134	17	08B	FO4102			
RCUETA	*J1129	69	35A	FO4502	J1126	69	32A	FO4502	J1333	19	FO4101
RDAMSK	*J1134	47	25B	FO4102	J1129	73	36B	FO4102			
RDEC00	*J1129	72	34A	FO4102	J1127	13	06B	FO4102	J1127	18	10A FO4102
	J1127	37	18B	FO4102	J1127	56	26A	FO4102			
RDNDX0	*J02	43		FO4501	J1117	19		FO4501	J1120	17	08B FO4502
RDNDY0	*J02	48		FO4501	J1117	40		FO4501	J1120	33	16A FO4502
RD405AF	J03	63		FO4102	*J1333	14		FO4101			
RD407AF	J03	56		FO4102	*J1333	09		FO4101			
RD407L	J03	57		FO4102	*J1333	07		FO4101			
RD408L	J03	58		FO4102	*J1333	08		FO4101			
RD409AF	J03	59		FO4102	*J1333	06		FO4101			
RD409L	J03	60		FO4102	*J1333	04		FO4101			
RD410L	J03	61		FO4102	*J1333	11		FO4101			

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution									
RD411AF	J03 62		FO4102	*J1333 02		FO4101				
REC1RA	*J1224 01	02B	FO4200	J1234 06	05A	FO4200				
REGNTA	*J1223 11	05B	FO4401	J1128 71	36A	FO4401				
REGNTAV	*J1133 26	12B	FO4401	J04 26		FO4401				
REGNT0	*J1128 72	34A	FO4401	J1133 27	13B	FO4401				
REG1S0E	*J1124 47	25B	FO4300	J1102 55	29B	FO4502	J1120 46	21A	FO4300	
	J1223 13	06B	FO4401							
REG1S1E	*J1124 51	27B	FO4300	J1102 60	28A	FO4502	J1120 42	20A	FO4300	
	J1223 10	07A	FO4401							
REG1S2E	*J1124 56	26A	FO4300	J1116 69	35B	FO4502	J1120 40	19A	FO4300	
	J1223 08	06A	FO4401							
RELIK0E	*J1130 35	17B	FO4102	J04 18		FO4102				
REL1K1E	*J1130 39	19B	FO4102	J04 19		FO4102				
REL1K2E	*J1130 42	20A	FO4102	J1127 09	04B	FO4102	J1127 14	09A	FO4102	
REL1K3E	*J1130 38	18A	FO4102	J04 21		FO4102	J1127 33	16B	FO4102	
	J1127 52	24A	FO4102							
REMANA	*J1128 06	05A	FO4200	J1133 15	07B	FO4200				
RENAD0V	*J1133 24	13A	FO4200	J1102 64	30A	FO4502	J1114 77	38B	FO4200	
	J1128 79	39B	FO4200	J1134 01	02B	FO4502	J1134 42	20A	FO4200	
	J1134 62	29A	FO4200	J1134 68	32A	FO4200	J1223 06	05A	FO4401	
	J1209 76		FO4402							
RENEWAV	*J1116 70	34B	FO4502	J1102 62	29A	FO4502				
REPLA0V	*J1234 08	04A	FO4200	J1114 70	33A	FO4102	J1118 49	24B	FO4300	
RFASTJ	*J1134 37	18B	FO4200	J1127 25	12B	FO4200				
RFASTK	*J1134 35	17B	FO4200	J1129 11	05B	FO4200				
RFLAKJ	*J1114 78	38A	FO4200	J1120 48	22A	FO4300	J1129 37	18B	FO4200	
RFLAKK	*J1114 76	37A	FO4200	J1128 76	37A	FO4200				
RFLAR0V	*J1133 07	04B	FO4200	J1114 79	39B	FO4200	J1128 78	38A	FO4200	
	J1129 35	17B	FO4200							
RFL1AA	*J1127 19	09B	FO4102	J04 61		FO4102				
RFL1BA	*J1127 39	19B	FO4102	J04 62		FO4102				
RFL1CA	*J1127 15	07B	FO4102	J04 20		FO4102				
RFL1DA	*J1127 50	23A	FO4102	J04 76		FO4102				
RFRCSA	*J1102 57	30B	FO4502	J1125 35	16B	FO4502	J1125 66	32B	FO4502	
	J1126 35	16B	FO4502	J1126 49	24B	FO4502				
RF0RGAV	*J1133 19	10B	FO4102	J1118 64	30A	FO4300	J1124 45	24B	FO4300	

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution									
	J1134 14	09A	FO4102							
RF402L	A04B B		FO4101	A04B C		FO4101	*J1333 79		FO4101
RF403L	*J1333 75		FO4101	A04A B		FO4102	A04A C		FO4102
	A04A D		FO4102	A04A E		FO4102			
RF404L	*J1333 73		FO4101	A04C B		FO4102	A04C C		FO4102
	A04C D		FO4102	A04C E		FO4102			
RF405L	*J1333 59		FO4101	A04D B		FO4102	A04D C		FO4102
	A04D D		FO4102	A04D E		FO4102			
RF406L	*J1333 60		FO4101	A04E B		FO4102	A04E C		FO4102
	A04E D		FO4102	A04E E		FO4102			
RF407L	*J1333 55		FO4101	A04F B		FO4102	A04F C		FO4102
	A04F D		FO4102	A04F E		FO4102			
RF409L	*J03 69		FO4101	A01B A		FO4101	A01B B		FO4101
	A01B C		FO4101	A01B D		FO4101			
RF410L	*J03 70		FO4101	A01C A		FO4101	A01C B		FO4101
	A01C C		FO4101	A01C D		FO4101			
RF411L	*J03 71		FO4101	A01D A		FO4101	A01D B		FO4101
	A01D C		FO4101	A01D D		FO4101			
RF421L	*J1333 80		FO4101	A04B D		FO4102	A04B E		FO4102
RGRUNAV	*J1234 07	04B	FO4401	J04 66		FO4401			
RGRUP0	*J1229 06	05A	FO4401	J1234 09	05B	FO4401			
RGSELJ	*J1134 19	09B	FO4102	J04 40		FO4102	J1127 17	08B	FO4102
	J1127 35	17B	FO4102						
RGSELK	*J1134 21	10B	FO4102	J04 41		FO4102	J1127 11	05B	FO4102
	J1127 54	25A	FO4102						
RGUSTA	*J1128 80	39A	FO4200	J1133 11	07A	FO4200			
RHOLYA	*J1127 36	17A	FO4502	J1125 79	37B	FO4502			
RJPEB0V	*J1133 13	06A	FO4200	J1134 40	19A	FO4200			
RKEYBA	*J1129 63	33B	FO4300	J1128 34	16A	FO4300			
RKYR0A	J1117 42		FO4502	J1121 19	09B	FO4502	*A06 8		FO4502
RKYR1A	J1117 46		FO4502	J1121 21	10B	FO4502	*A06 9		FO4502
RKYR2A	J1117 41		FO4502	J1121 23	11B	FO4502	*A06 10		FO4502
RKYR3A	J1117 45		FO4502	J1121 25	12B	FO4502	*A06 7		FO4502
RKYR4A	J1117 47		FO4502	J1121 29	13B	FO4502	*A06 6		FO4502
RKYR5A	J1117 48		FO4502	J1121 31	14B	FO4502	*A06 4		FO4502
RKYR6A	J1117 52		FO4502	J1121 34	15B	FO4502	*A06 5		FO4502

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution									
RKYR7A	J1117 54		FO4502	J1129 03	02A	FO4502	*A06 3		FO4502
RLADP0V	*J1230 19	10B	FO4200	J1124 14	06A	FO4600	J1124 26	13A	FO4600
	J1130 14	06A	FO4600	J1130 26	13A	FO4600	J1133 38	20A	FO4502
	J1134 54	25A	FO4102	J1232 65	34B	FO4200			
RLAST0V	*J1234 01	02B	FO4200	J1134 60	28A	FO4200			
RLDL33E	J03 60		FO4102	*J1333 21		FO4101			
RLDL40E	J04 57		FO4102	*J1333 22		FO4101			
RLDL41E	J04 59		FO4102	*J1333 43		FO4101			
RLGNDAV	*J1133 35		FO3601	*J1133 25	11A	FO4102	J1101 39	24B	FO4501
	J1118 52	25A	FO4300	J1120 35	16B	FO4300	J1124 50	23A	FO4300
	J1130 33	16B	FO4102	J1134 18	10A	FO4102	J1217 66	32A	FO3601
	J1333 64		FO4401	J1133 25		FO3601			
RLGRDAV	*J1133 30	14B	FO4102	J1101 52	29B	FO4501	J1118 53	26B	FO4300
	J1121 17	08B	FO4501	J1121 33	16A	FO4502	J1130 36	17A	FO4102
RLINDD	*J1232 69	35A	FO4200						
RLRHMJ	*J1114 61	32B	FO4102		J04 42	FO4102	J1129 71	36A	FO4102
	J1333 05		FO4101						
RLRQ1D4	*J1132 09	04B	FO4200	J03 44			J1131 46		FO4200
RLSB2D4	*J1132 69	35A	FO4600						
RLSD20V	*J1133 78	36A	FO4600	J1124 20	10A	FO4600			
RMAR1J	*J1114 55	29B	FO4502	J1124 08	04A	FO4600	J1124 22	11A	FO4600
	J1126 66	32B	FO4502	J1130 08	04A	FO4600	J1130 22	11A	FO4600
RMAR1K	*J1114 57	30B	FO4502	J1128 13	06B	FO4200			
RMRSTD4	*J1132 01	02B	FO5300	J1114 53	28B	FO4502	J1114 80	39A	FO4200
	J1131 19		FO5300	J1134 15	07B	FO4200	J1134 36	17A	FO4200
	J1134 50	23A	FO4102	J1134 53	28B	FO4200	J1134 63	33B	FO4200
RMSBE0V	*J1133 77	38A	FO4600	J1128 05	03B	FO4200	J1130 03	03B	FO4600
RMUX12X	*J1120 06	03A	FO4502	J1129 25	12B	FO4502			
RMUX22X	*J1120 22	11A	FO4502	J1129 23	11B	FO4502			
RMUX31X	*J1121 04	02A	FO4501	J1128 48	22A	FO4300			
RMUX41X	*J1121 20	01A	FO4502	J1129 59	31B	FO4300			
RMUX61X	*J1120 36	17A	FO4300	J1130 05	04B	FO4600			
RMXC1D4	*J1132 14	09A	FO4502	J05 65		FO4502			
RMXC2D4	*J1132 21	01B	FO4502	J05 67		FO4502			
RMXC3D4	*J1132 27	13B	FO4502	J05 69		FO4502			
RMXC51U	*J1126 70	34A	FO4502	J1120 14	06A	FO4502	J1120 27	14A	FO4502

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution								
	J1121 14	06A	FO4501	J1121 27		FO4502	J1127 06	05A	FO4502
	J1132 18	10A	FO4502						
RMXC52U	*J1126 72	35A	FO4502	J1120 10	05A	FO4502	J1120 26	13A	FO4502
	J1121 10	05A	FO4501	J1121 26	13A	FO4502	J1127 08	06A	FO4502
	J1132 17	08B	FO4502						
RMXC53U	*J1126 74	36A	FO4502	J1120 08	04A	FO4502	J1120 24	12A	FO4502
	J1121 08	04A	FO4501	J1121 24	12A	FO4502	J1132 23	11B	FO4502
RMXC54U	*J1126 76	37A	FO4501	J04 69		FO4502	J1120 13	07A	FO4502
	J1121 13	07A	FO4501	J1127 10	07A	FO4502	J1133 35	18A	FO4502
RMXC55U	**J1126 68	33A	FO4502	J1114 60	28A	FO4502			
RNANAAV	*J1133 37	17A	FO4502	J1120 30	15A	FO4502	J1128 50	23A	FO4300
	J1128 56	26A	FO4300						
RNORME	J1304 66		FO3100	*J1333 56		FO4101			
RNORM0	*A03H 1		FO3100	J1304 51		FO3100			
RNORM1	*A03H 2		FO3100	J1304 48		FO3100			
RNORM2	*A03H 4		FO3100	J1304 54		FO3100			
RNORM3	*A03H 8		FO3100	J1304 50		FO3100			
R0R01S	*A05A 2A		FO4401	J1333 70		FO4401			
R0R02S	*A04B 2A		FO4401	J1333 69		FO4401			
R0R03S	*A04A 2A		FO4401	J1333 72		FO4401			
R0R04S	*A04C 2A		FO4401	J1333 71		FO4401			
R0R05S	*A04D 2A		FO4401	J1333 66		FO4401			
R0R06S	*A04E 2A		FO4401	J1333 63		FO4401			
R0R07S	*A04F 2A		FO4401	J1333 62		FO4401			
R0W12S	*A05C 2A		FO4401	J03 64		FO4401			
R0W13S	*A05D 2A		FO4401	J03 65		FO4401			
R0W14S	*A05E 2A		FO4401	J03 66		FO4401			
R0W15S	*A05F 2A		FO4401	J03 67		FO4401			
R0216S	*A05B 2A		FO4401	J03 68		FO4401			
RPADRA	*J1128 75	37B	FO4200	J1230 21	11B	FO4200			
RPADRAV	*J1133 40	19A	FO4502	J1128 61	32B	FO4502			
RPATRA	*J1129 66	31A	FO4200	J1132 29	14B	FO4600	J1132 34	16A	FO4600
	J1132 35	17B	FO4600	J1132 40	19A	FO4600	J1132 41	22B	FO4600
	J1132 47	25B	FO4600	J1132 48	22A	FO4600	J1132 53	28B	FO4600
	J1132 54	25A	FO4600	J1132 59	31B	FO4600	J1132 62	29A	FO4600
	J1132 65	34B	FO4600	J1132 68	32A	FO4600	J1132 71	36A	FO4600

Table 5-8. Right Hand Assembly Key Signal Lookup
--Continued

Signal	Distribution								
	J1132 76	37A	FO4600	J1132 77	38B	FO4600			
RPATR0	*J1127 27	13B	FO4200	J1129 68	32A	FO4200			
RPGX11U	**J1125 38	18A	FO4502	J1120 03	02B	FO4502			
RPGX12U	*J1125 40	19A	FO4502	J1120 05	03B	FO4502			
RPGX13U	*J1125 42	20A	FO4502	J1120 07	04B	FO4502			
RPGX14U	*J1125 46	21A	FO4502	J1120 09	05B	FO4502			
RPGX15U	*J1125 36	17A	FO4502	J1126 51	25B	FO4502			
RPGX21U	*J1126 54	26A	FO4502	J1120 11	06B	FO4502	J1127 41	22B	FO4502
RPGX22U	*J1126 56	28B	FO4502	J1120 15	07B	FO4502	J1127 46	21A	FO4502
RPGX23U	*J1126 60	28A	FO4502	J1120 18	09A	FO4502	J1127 48	22A	FO4502
RPGY31U	*J1125 70	34A	FO4502	J1120 19	09B	FO4502			
RPGY32U	*J1125 72	35A	FO4502	J1120 21	10B	FO4502			
RPGY33U	*J1125 74	36A	FO4502	J1120 23	11B	FO4502			
RPGY34U	*J1125 76	37A	FO4502	J1120 25	12B	FO4502			
RPGY35U	*J1125 68	33A	FO4502	J1126 37	17B	FO4502			
RPGY41U	*J1126 38	18A	FO4502	J1120 29	13B	FO4502	J1127 40	19A	FO4502
RPGY42U	**J1126 40	19A	FO4502	J1120 31	14B	FO4502	J1127 42	20A	FO4502
RPGY43U	*J1126 42	20A	FO4502	J1120 34	15B	FO4502	J1127 38	18A	FO4502
RPR0CE	J1304 60		FO3100	*J1333 68		FO4101			
RPR0C0	*A03E 1		FO3100	J1304 7		FO3100			
RPR0C1	*A03E 2		FO3100	J1304 4		FO3100			
RPR0C2	*A03E 4		FO3100	J1304 10		FO3100			
RPR0C3	*A03E 8		FO3100	J1304 03		FO3100			
RREQJK	*J1134 57	30B	FO4200	J1127 21	10B	FO4200	J1132 03	02A	FO4200
RRTS10E	*J1217 61	31B	FO3601	J1130 43	23B	FO3601			
RRTS11E	*J1217 65	33B	FO3601	J1115 46	21A	FO3601	J1130 41	22B	FO3601
RRTS12E	*J1217 68	33A	FO3601	J1115 48	22A	FO3601	J1130 46	21A	FO3601
RRTS13E	*J1217 64	31A	FO3601	J1115 50	23A	FO3601	J1130 48	22A	FO3601
RRTS21E	*J1130 51	27B	FO3601	J1106 19	09B	FO3301	J1112 70	33A	FO3302
	J1115 41	22B	FO3601						
RRTS22E	*J1130 56	26A	FO3601	J1106 25	12B	FO3301	J1112 64	30A	FO3302
	J1115 43	23B	FO3601						
RRTS23E	*J1130 52	24A	FO3601	J1106 42	20A	FO3301	J1112 55	29B	FO3302
	J1115 45	24B	FO3601						
RSAR0	*J02 57		FO3900	A02B 8		FO3900			
RSCRUA	*J1128 01	02B	FO4200	J1133 09	05B	FO4200			

Table 5-8. Right Hand Assembly Key Signal Lookup -Continued

Signal	Distribution								
RSECAE	J1302 64		FO3100	*J1333 78		FO4101			
RSECBE	J1302 66		FO3100	*J1333 77		FO4101			
RSECT0	J1302 46		FO3100	J1302 51		FO3100	*A03D 1		FO3100
RSECT1	J1302 37		FO3100	J1302 48		FO3100	*A03D 2		FO3100
RSECT2	J1302 41		FO3100	J1302 54		FO3100	*A03D 4		FO3100
RSECT3	J1302 40		FO3100	J1302 50		FO3100	*A03D 8		FO3100
RSENAJQ	*J0423		FO4300	J1129 19	09B	FO4300			
RSENAKQ	*J0422		FO4300	J1129 07	03A	FO4502	J1129 61	32B	FO4300
RSFRUS	*J0252		FO3900	A02G 8		FO3900			
RSHFE0	*J1128 63	33B	FO4502	J1114 62	29A	FO4502			
RSH00K	*J02 61		FO3900	A02A 8		FO3900			
RSIFFE	J1304 62		FO3100	*J1333 65		FO4101			
RSIFF0	*A03F 1		FO3100	J1304 22		FO3100			
RSIFF1	*A03F 2		FO3100	J1304 14		FO3100			
RSIFF2	*A03F 4		FO3100	J1304 21		FO3100			
RSIFF3	*A03F 8		FO3100	J1304 15		FO3100			
RSMAP1	*J02 54		FO3900	A02E 8		FO3900			
RSMAP2	*J02 55		FO3900	A02D 8		FO3900			
RS0THR	*J02 56		FO3900	A02C 8		FO3900			
RSPCL0	*A0G3 I		FO3100	J1304 46		FO3100			
RSPCL1	*A03G 2		FO3100	J1304 37		FO3100			
RSPCL2	*A03G 4		FO3100	J1304 41		FO3100			
RSPCL3	*A03G 8		FO3100	J1304 40		FO3100			
RSPRLN	*J02 53		FO3900	A02F 8		FO3900			
RSPCLE	J1304 64		FO3100	*J1333 57		FO4101			
RSSWVD	*A03B 8		FO3900	J02 62		FO3900			
RSTRKS	*J02 51		FO3900	A02H 8		FO3900			
RSWST0	*J1129 09	04B	FO4502	J1128 07	03A	FO4502			
RSW1TA	*J1129 21	10B	FO4300	J1128 36	17A	FO4300			
RTA160V	*J04 47		FO4101	J1333 03		FO4101			
RTA170V	*J04 48		FO4101	J1333 29		FO4101			
RTA180V	*J04 49		FO4101	J1333 20		FO4101			
RTA190V	*J04 53		FO4102	J111077	38B	FO3601	J1116 17	09B	FO3601
	J1217 62	30A	FO3601						
RTESTE	J1302 62		FO3100	*J1333 76		FO4101			
RTEST0	*A03C 1		FO3100	J1302 22		FO3100			
RTEST1	*A03C 2		FO3100	J1302 14		FO3100			

Table 5-8. Right Hand Assembly Key Signal Lookup -Continued

Signal	Distribution								
RTEST2	*A03C 4		FO3100	J1302 21		FO3100			
RTEST3	*A03C 8		FO3100	J1302 15		FO3100			
RTTG1A	*J1128 52	24A	FO4300	J1120 43	22B	FO4300			
RUX5DD4	*J05 61		FO4502	J1128 54	25A	FO4300	J1131 52		FO4300
RVARXA	*J1128 46	21A	FO4300	J1120 39	18B	FO4300			
RVAR00	*J02 67		FO4501	J1117 05		FO4501	J1121 03	O2B	FO4501
RVAR10	*J02 68		FO4501	J1117 06		FO4501	J1121 05	O3B	FO4501
RVAR20	*J02 69		FO4501	J111707		FO4501	J1121 07	04B	FO4501
RVAR30	*J02 70		FO4501	J1117 08		FO4501	J1121 09	05B	FO4501
RVAR40	*J02 71		FO4501	J1117 09		FO4501	J1121 11	06B	FO4501
RVAR50	*J02 72		FO4501	J1117 10		FO4501	J1121 15	07B	FO4501
RVAR60	*J02 73		FO4501	J1117 17		FO4501	J1121 18	09A	FO4501
RVRGDD4	*J1232 75	37B	FO4501	J02 58		FO4501	J1231 73		FO4501
RWH1POV	*J1133 01	02B	FO4200	J1128 04	04A	FO4200	J1128 10	07A	FO4200
	J1129 04	04A	FO4102	J1129 42	20A	FO4102	J1130 40	19A	FO4102
RXSWDD4	*J05 63		FO4300	J1129 17	08B	FO4300	J1231 08		FO4300
RXYDA0	*J1129 27	13B	FO4502	J1120 41	19B	FO4300			
RX65R0	*J1128 30	15A	FO4300	J1120 50	24A	FO4300			
R0ACHAV	*J1133 31	16B	FO4300	J112047	23A	FO4300			
R0ACH0	*J05 71		FO4104	J1133 33	17B	FO4300			
R0MERTA	*J1118 55	27B	FO4300	J1124 43	23B	FO4300			
R0MERTB	*J111861	31B	FO4300	J112441	22B	FO4300			
R0MERTC	*J111860	28A	FO4300	J112446	21A	FO4300			
R0MERTD	*J1118 63	31A	FO4300	J1124 48	22A	FO4300			
R0NEGA	*J1129 06	05A	FO4200	J1133 04	02A	FO4200			
R0NERJ	*J 1134 13	06B	FO4200	J1129 08	06A	FO4200			
R0NE10V	*J 1133 03	03A	FO4200	J1129 34	16A	FO4200			
R0S020V	*J1133 48	21A	FO4600	J1128 08	06A	FO4200	J1130 01	02B	FO4600
R0S030V	*J113346	22B	FO4600	J112905	03B	FO4102	J113004	02A	FO4600
R0S040V	*J 1133 43	24B	FO4600	J1130 06	03A	FO4600			
R0S050V	*J1133 53	26B	FO4600	J1118 54	26A	FO4300	J112403	03B	FO4600
R0S060V	*J1133 66	32A	FO4600	J1118 57	29B	FO4300	J1124 01	02B	FO4600
	J1130 29	14B	FO4102						
R0S070V	*J1133 63	30A	FO4600	J1118 51	25B	FO4300	J1124 04	02A	FO4600
	J1130 31	15B	FO4102						
R0S080V	*J1133 60	28A	FO4600	J1124 06	03A	FO4600	J1224 04	04A	FO4200
R0S090V	*J 1133 56	28B	FO4600	J1130 17	09B	FO4600			

Table 5-8. Right Hand Assembly Key Signal Lookup -Continued

Signal	Distribution								
R0S100V	*J1133 57	30B	FO4600	J1130 15	08B	FO4600			
R0S110V	*J1133 68	32B	FO4600	J1130 18	09A	FO4600			
R0S120V	*J1133 80	38B	FO4600	J1130 20	10A	FO4600			
R0S130V	*J1133 71	36B	FO4600	J1124 17	09B	FO4600			
R0S140V	*J1133 70	34B	FO4600	J1124 15	08B	FO4600			
R0S150V	*J1133 72	34A	FO4600	J1124 18	09A	FO4600	J1129 36	17A	FO4200
R0UTSA	*J1127 04	04A	FO4502	J1133 17	09B	FO4502			
R0UTSOV	*J1133 14	08B	FO4502	J1114 68	32A	FO4102	J1134 56	26A	FO4102
R0WRGAV4	J1229 10	07A	FO4401	J1231 24		FO4401	*A05E 4A		FO4401
	*A05D 4A		FO4401	*A05C 4A		FO4401	*A05B 4A		FO4401
	*A05F 4A		FO4401						
R0WR1AV	J04 11		FO4401	*J1333 42		FO4401			
R0WR2AV	J04 12		FO4401	*J1333 40		FO4401			
R0WR3AV	J04 13		FO4401	*J1333 46		FO4401			
R0WR4AV	J04 14		FO4401	J1129 08	06A	FO4401	*J1333 45		FO4401
R1NVEOV	*J1133 18	09A	FO4200	J04 15		FO4200	J1124 54	25A	FO4300
	J1128 03	02A	FO4502	J1224 05	03B	FO4200			
SPI001	*J1117 56								
SPI002	*J1117 62								
SPI003	*J1117 64								
SPI004	*J1117 61								
SPI005	*J1117 63								
SPI006	*J1117 65								
SPI007	*J1117 66								
SPI008	*J1117 72								
SPI009	*J1117 74								
SPI010	*J1117 71								
SPI011	*J1117 73			J1115 73		FO5201			
SPI012	*J1117 75			J1123 47		FO5202	J1119 23		FO5202
SPI013	*J1117 76								
SPI014	*J1117 77			J1123 50		FO5202	J1119 25		FO5202
SPI015	*J1117 78			J1128 19		FO5202	J1128 25		FO5202
	J1128 42		FO5202	J1128 26		FO5202	J1128 37		FO5202
	J1128 31		FO5202						
SPI016	*J1131 41			J1118 23		FO5203	J1132 31		FO5201
	J1132 19		FO5201	J1132 37		FO5201	J1119 73		FO5201
	J1132 36		FO5201						

Table 5-8. Right Hand Assembly Key Signal Lookup -Continued

Signal	Distribution					
SPI017	J1131 62		J1118 33	FO5203	J1119 33	FO5202
	J1227 49	FO5201				
SPI018	*J1131 56		J1118 25	FO5203	J1119 31	FO5202
SPI019	*J1131 55		J1119 34	FO5202		
SPI020	*J1131 53		J1133 21	FO5201	J1134 75	FO5201
	J1133 34	FO5201	J1133 24	FO5201	J1133 25	FO5201
	J1133 35	FO5201	J1134 74	FO5201	J1134 75	FO5201
	J1227 35	FO5201	J1134 75	FO5201		
SPI021	*J1131 51					
SPI022	*J1131 72		J1119 29	FO5202		
SPI023	*J1131 66		J1233 27	FO5201		
SPI024	*J1131 65		J1218 05	FO5201		
SPI025	*J1131 63					
SPI026	*J1131 61					
SPI027	*J1131 78					
SPI028	*J1131 76					
SPI029	*J1131 75		J1327 17	FO5202		
SPI030	*J1131 73					
SPI031	*J1131 71		J1327 09	FO5202	J1327 34	FO5202
SPI032	*J1231 56		J1327 07	FO5202	J1327 33	FO5202
SPI033	*J1231 55					
SPI034	*J1231 53					
SPI035	*J1231 51					
SPI036	*J1231 72					
SPI037	*J1231 66		J1120 50	FO5201		
SPI038	*J1231 65					
SPI039	*J1231 63		J1230 35	FO5202	J1132 73	FO5201
SPI040	*J1231 61					
SPI041	*J1231 78		J1132 42	FO5201		
SPI042	*J1231 76		J1234 73	FO5202		
SPI043	*J1231 75					
SPI045	*J1131 05					
SPI046	*J1131 07					
SPI047	*J1131 35					
SPI048	*J1131 36					
SPI049	*J1131 37					
SPI050	*J1131 38					

Table 5-8. Right Hand Assembly Key Signal Lookup -Continued

Signal	Distribution								
SPI051	*J1131 39								
SPI052	*J1231 52								
SPI053	*J1231 42								
SPI054	*J1231 46								
SPI055	*J1231 35								
SPI056	*J1231 37								
SPI057	*J1231 38								
SPI058	*J1231 39								
SPI060	*J1231 10								
SPI061	*J1231 17								
SPI062	*J1231 20								
SPI063	*J1231 23								
SPI064	*J1231 25								
SPI065	*J1231 41								
VACENR	*J1104 52	24A	FO3602	J1103 56	26A	FO3602			
VACENS	*J1103 50	23A	FO3602	J1104 56	26A	FO3602	J1106 13	06B	FO3601
	J1109 36	17A	FO3602	J1110 36	17A	FO3603	J1222 42	20A	FO5403
VACLTA	*J1103 36	17A	FO3602	J1105 11	05B	FO3602	J1127 03	02A	FO3402
VACPAA	*J1103 73	36B	FO3602	J1106 08	06A	FO3602			
VACP1J	*J1110 37	18B	FO3602	J1102 22	12A	FO3603	J1109 40	19A	FO3602
VACP1K	*J1110 35	17B	FO3602	J1102 05	03B	FO3500	J1103 79	39B	FO3602
	J1109 30	15A	FO3602	J1109 42	20A	FO3602			
VACP2J	*J1109 37	18B	FO3602	J1103 77	38B	FO3602	J1105 24	13A	FO3603
VACP2K	*J1109 35	17B	FO3602	J1107 38	20A	FO3602			
VACP20V	*J1107 40	19A	FO3602	J1109 34	16A	FO3602			
VACP3J	*J1109 31	15B	FO3602	J1102 24	13A	FO3603	J11O 42	20A	FO3602
VACP3K	*J1109 33	16B	FO3602	J1110 40	19A	FO3602			
VACP60	*J1106 15	07B	FO5403	J1109 38	18A	FO3602			
VAC25J	*J1110 31	15B	FO3603	J1104 26	14A	FO3603			
VAC25K	*J1110 33	16B	FO3603	J1105 64	30A	FO3603			
VAC5004	*J1222 35	17B	FO5403	J1104 13	06B	FO3603	J1104 79	39B	FO3603
	J1109 06	05A	FO3603	J1110 38		FO3602	J1110 38	18A	FO3500
	J1111 38	18A	FO3500	J1323 35		FO5403	J1323 37		FO5403
VAD01A	*J1104 14	09A	FO3200	J1105 20	11A	FO3301			
VAD02A	*J1104 21	10B	FO3200	J1105 19	09B	FO3301			
VAD03A	*J1104 27	13B	FO3200	J1105 25	12B	FO3301			

Table 5-8. Right Hand Assembly Key Signal Lookup -Continued

Signal	Distribution								
VAD110	*J1105 14	09A	FO33U1	J1305 06		FO3301	J1306 06		FO3302
	J1307 06		FO3302						
VAD120	*J1105 21	10B	FO3301	J1305 20		FO3301	J1306 20		FO3302
	J1307 20		FO3302						
VAD130	*J1105 27	13B	FO3301	J1305 54		FO3301	J1306 54		FO3302
	J1307 54		FO3302						
VAIENA	*J1103 31	15B	FO3602	J1105 49	26B	FO3301	J1107 27	13B	FO3602
VAIEN0V	*J1107 26	12B	FO3602	J1104 17	08B	FO3200	J1104 18	10A	FO3200
	J1104 23	11B	FO3200						
VAINHA	*J1106 63	33B	FO3500	J1305 34		FO3301	J1305 38		FO3301
	J1305 70		FO3301	J1305 78		FO3301	J1306 34		FO3302
	J1306 38		FO3302	J1306 70		FO3302	J1306 78		FO3302
VALBI0	*J1105 51	27B	FO3301	J1305 56		FO3301	J1306 56		FO3302
	J1307 56		FO3302						
VALDEA	*J1104 66	31A	FO3602	J1224 08	06A	FO3602			
VALENA	*J110501	02B	FO3602	J110354	25A	FO3602	J110408	06A	FO3602
VALENR	*J1105 06	05A	FO3602	J1104 10	07A	FO3602	J1106 03	02A	FO3602
VALENS	*J1104 06	05A	FO3602	J1102 25	12B	FO3603	J1103 34	16A	FO3602
	J1105 10	07A	FO3602						
VALTDJ	*J1110 49	26B	FO3602	J1104 71	36A	FO3602			
VAM11A	J1108 10	05A	FO3500	*J130540		FO3301	J1306 04		FO3302
VAM12A	J1108 08	04A	FO3500	*J1305 36		FO3301	J1306 18		FO3302
VAM13A	J1108 06	03A	FO3500	*J1305 72		FO3301	J1306 48		FO3302
VAM14A	J1108 04	02A	FO3500	*J1305 80		FO3301	J1306 46		FO3302
VAM21A	J1108 24	12A	FO3500	*J 1306 40		FO3302	J1307 04		FO3302
VAM22A	J1108 22	11A	FO3500	*J1306 36		FO3302	J1307 18		FO3302
VAM23A	J1108 20	10A	FO3500	*J1306 72		FO3302	J1307 48		FO3302
VAM24A	J1108 18	09A	FO3500	*J1306 80		FO3302	J1307 46		FO3302
VAM3CA	*J1112 63	33B	FO3602	J1103 75	37B	FO3602			
VAM31A	J1103 09	04B	FO3200	J1108 38	18A	FO3500	*J1307 40		FO3200
	*J1307 40		FO3302						
VAM32A	J1103 22	12A	FO3200	J1108 36	17A	FO3500	*J1307 36		FO3200
	*J1307 36		FO3302						
VAM33A	J1103 14	09A	FO3200	J1108 34	16A	FO3500	*J1307 72		FO3200
	*J1307 72		FO3302						
VAM34A	J1105 77	38B	FO3602	J1107 21	11 B	FO3602	J1108 30	15A	FO3500
	J1110 51	27B	FO3602	*J1307 80		FO3302			

Table 5-8. Right Hand Assembly Key Signal Lookup -Continued

Signal	Distribution								
VAM340V	*J1107 19	O1B	FO3602	J1104 03	02A	FO3602	J110404	04A	FO3602
	J1104 70	33A	FO3602	J1112 59	31B	FO3602			
VAPARA	*J1104 15	07B	FO3603	J1109 15	07B	FO3603			
VAPBRA	*J1104 75	37B	FO3603	J1109 03	02A	FO3603			
VAPCAA	*J1104 22	12A	FO3603	J1107 06	05A	FO3603			
VAPCAJ	*J1109 13	06B	FO3603	J1305 14		FO3301	J1305 66		FO3301
	J1306 14		FO3302	J1306 66		FO3302	J1307 14		FO3302
	J1307 66		FO3302						
VAPCAK	*J1109 11	05B	FO3603	J1104 11	05B	FO3603			
VAPCA0V	*J1107 08	04A	FO3603	J1109 10	07A	FO3603			
VAPCBA	*J1105 60	28A	FO3603	J1107 04	02A	FO3603			
VAPCBJ	*J1109 07	03A	FO3603	J1305 10		FO3301	J1305 60		FO3301
	J1306 10		FO3302	J1306 60		FO3302	J1307 10		FO3302
	J1307 60		FO3302						
VAPCBK	*J1109 09	04B	FO3603	J1104 77	38B	FO3603			
VAPCB0V	*J1107 03	03A	FO3603	J1109 01	02B	FO3603			
VAPHC0	*J1106 06	05A	FO3603	J1104 24	13A	FO3603	J1105 59	31B	FO3603
	J1105 62	29A	FO3603	J111030	15A	FO3603	J1110 34	16A	FO3603
VARMCA	*J1105 22	12A	FO3603	J1106 34	16A	FO3402			
VARME0	*J1106 09	04B	FO3603	J1105 26	14A	FO3603	J1105 61	32B	FO3603
VARMSA	*J1105 63	33B	FO3603	J1106 29	14B	FO3402			
VARS30	*J1106 21	O1B	FO3301	J1307 25		FO3302			
VARS60	*J1106 27	13B	FO3301	J1306 25		FO3302			
VARS90	*J1106 38	18A	FO3301	J1305 25		FO3301			
VASHFA	*J1105 72	34A	FO3603	J1106 54	25A	FO3603			
VASHFR	*J1105 75	37B	FO3602	J1102 38	18A	FO3602	J1104 73	36B	FO3602
VASHFS	*J1104 72	34A	FO3602	J1105 79	39B	FO3602			
VASMPA	*J1102 23	11B	FO3601	J1105 68	32A	FO3200	J1222 61	32B	FO3200
VATB1AV	*J1107 37	17A	FO3500	J1108 07	05B	FO3500	J1108 21	11B	FO3500
	J1108 35	17B	FO3500						
VATB2AV	*J1107 34	15A	FO3500	J1108 05	04B	FO3500	J1108 19	10B	FO3500
	J1108 33	16B	FO3500						
VATB3AV	*J1107 30	14B	FO3500	J1108 03	03B	FO3500	J1108 17	09B	FO3500
	J1108 31	15B	FO3500						
VATB4AV	*J1107 31	16B	FO3500	J1108 01	02B	FO3500	J1108 15	08B	FO3500
	J1108 29	14B	FO3500						

Table 5-8. Right Hand Assembly Key Signal Lookup -Continued

Signal	Distribution								
VATDS0V	*J1107 42	18B	FO3500	J1104 29	14B	FO3500	J1104 40	19A	FO3500
	J1105 54	25A	FO3500						
VATENAV	*J1107 01	02B	FO3500	J1102 37	18B	FO3602	J1102 70	33A	FO3402
	J1105 13	06B	FO3602	J1106 17	08B	FO3301	J110623	11B	FO3301
	J1106 40	19A	FO3301	J1111 05	03B	FO3402			
VAT1C0	*J1104 46	21A	FO3500	J1105 56	26A	FO3500			
VAT1FA	*J1105 52	24A	FO3500	J1104 41	22B	FO3500			
VAT1FR	*J1105 46	21A	FO3500	J1104 43	23B	FO3500			
VAT1FS	*J1104 45	24B	FO3500	J1105 50	23A	FO3500	J1118 03	02B	FO3500
VAT1M1C	*J1108 11	07B	FO3500	J1104 48	22A	FO3500			
VAT1M2C	*J1108 14	06A	FO3500	J1104 50	23A	FO3500			
VAT2C0	*J1105 38	18A	FO3500	J1104 42	20A	FO3500			
VAT2FA	*J1104 38	18A	FO3500	J1105 34	16A	FO3500			
VAT2FR	*J1104 30	15A	FO3500	J1105 36	17A	FO3500			
VAT2FS	*J1105 30	15A	FO3500	J1104 36	17A	FO3500	J1118 05	03B	FO3500
VAT2M1C	*J1108 27	13B	FO3500	J1105 40	19A	FO3500			
VAT2M2C	*J1108 26	13A	FO3500	J1105 42	20A	FO3500			
VAT3C0	*J1105 33	16B	FO3500	J1104 34	15B	FO3500			
VAT3FA	*J1104 33	16B	FO3500	J1105 35	17B	FO3500			
VAT3FR	*J1104 39	19B	FO3500	J1105 37	18B	FO3500			
VAT3FS	*J1105 39	19B	FO3500	J1104 37	18B	FO3500	J1118 07	04B	FO3500
VAT3M1C	*J1108 39	19B	FO3500	J1105 29	14B	FO3500			
VAT3M2C	*J1108 40	19A	FO3500	J1105 31	15B	FO3500			
VAUNLA	*J1104 09	04B	FO3602	J1105 03	02A	FO3602			
VAUNLR	*J1104 01	02B	FO3602	J1102 40	19A	FO3602	J1105 07	03A	FO3602
VAUNLS	*J1105 09	04B	FO3602	J1103 38	18A	FO3602	J110405	03B	FO3602
VA0EN0	*J1105 15	07B	FO3602	J1307 34		FO3302	J1307 38		FO3302
	J1307 70		FO3302						
VA25EAV	*J1107 25	11A	FO3602	J1109 56	26A	FO3602			
VA25EK	*J1109 47	25B	FO3602	J1106 10	07A	FO3602			
VA25E0	*J1102 35	17B	FO3602	J1107 23	12A	FO3602	J1109 54	25A	FO3602
VBCENR	*J1106 52	24A	FO3603	J1103 48	22A	FO3603			
VBCENS	*J1103 43	23B	FO3603	J1106 56	26A	FO3603	J111064	30A	FO3603
	J1112 19	09B	FO5403	J1114 50	23A	FO3603	J1222 34	16A	FO5403
VBCLTA	*J1103 55	29B	FO3603	J1113 55	29B	FO3603	J1127 05	03B	FO3402
VBCPAA	*J1103 74	35B	FO3603	J1106 04	04A	FO3603			
VPCP1J	*J1114 49	26B	FO3603	J1102 43	23B	FO3603	J111068	32A	FO3603

Table 5-8. Right Hand Assembly Key Signal Lookup -Continued

Signal	Distribution								
VBCP1K	*J1114 47	25B	FO3603	J1103 72	34A	FO3603	J1110 60	28A	FO3603
	J1110 70	33A	FO3603						
VBCP2J	*J1110 61	32B	FO3603	J1103 71	36A	FO3603	J1113 17	08B	FO3603
VBCP2K	*J1110 59	31B	FO3603	J1116 21	11B	FO3603			
VBCP20V	*J1116 19	01B	FO3603	J1110 62	29A	FO3603			
VBCP3J	*J1110 55	29B	FO3603	J1102 46	21A	FO3603	J1114 56	26A	FO3603
VBCP3K	*J1110 57	30B	FO3603	J1114 54	25A	FO3603			
VBC25J	*J1114 43	23B	FO3603	J1112 20	11A	FO3603			
VBC25K	*J1114 45	24B	FO3603	J1 1 13 49	26B	FO3603			
VBC5004	*J1222 33	16B	FO5403	J1102 50	23A	FO3603	J1110 66	31A	FO3603
	J1113 70	33A	FO3603	J1113 74	35B	FO3603	J1114 06	05A	FO3603
	J1323 39		FO5403	J1323 41		FO5403			
VBD01A	*J1112 52	24A	FO3200	J1113 56	26A	FO3302			
VBD02A	*J111246	21A	FO3200	J1113 50	23A	FO3302			
VBD03A	*J111245	24B	FO3200	J1113 43	23B	FO3302			
VBD110	*J1113 52	24A	FO3302	J1308 06		FO3302	J1309 06		FO3302
	J1310 06		FO3303						
VBD120	*J1113 46	21A	FO3302	J1308 20		FO3302	J1309 20		FO3302
	J1310 20		FO3303						
VBD130	*J1113 45	24B	FO3302	J1308 54		FO3302	J1309 54		FO3302
	J1310 54		FO3303						
VBGP60	*J1112 21	01B	FO5403	J1114 52	24A	FO3603			
VBIENA	*J1103 64	30A	FO3603	J1106 35	17B	FO3302	J1116 27	13B	FO3603
VBIEN0V	*J1116 26	12B	FO3603	J111241	22B	FO3200	J1112 48	22A	FO3200
	J1112 54	25A	FO3200						
VBINHA	*J1106 80	39A	FO3500	J1308 34		FO3302	J1308 38		FO3302
	J1308 70		FO3302	J1308 78		FO3302	J1309 34		FO3303
	J1309 38		FO3303	J1309 70		FO3303	J1309 78		FO3303
VBLBI0	*J1106 39	19B	FO3302	J1308 56		FO3302	J1309 56		FO3302
	J1310 56		FO3302						
VBLDEA	*J1112 69	35A	FO3602	J1224 10	07A	FO3602			
VBLENA	*J1113 01	02B	FO3603	J1103 46	21A	FO3603	J1112 08	06A	FO3603
VBLENR	*J1113 06	05A	FO3603	J1112 10	07A	FO3603			
VBLENS	*J1112 06	05A	FO3603	J1102 48	22A	FO3603	J1103 70	33A	FO3603
	J1106 24	13A	FO3603	J1113 10	07A	FO3603			
VBLTDJ	*J1110 43	23B	FO3603	J1112 24	13A	FO3603			
VBM11A	J1115 10	05A	FO3500	*J 1308 40		FO3302	J1309 04		FO3303

Table 5-8. Right Hand Assembly Key Signal Lookup -Continued

Signal	Distribution								
VBM12A	J1115 08	04A	FO3500	*J1308 36		FO3302	J1309 18		FO3303
VBM13A	J1115 06	03A	FO3500	*J1308 72		FO3302	J1309 48		FO3303
VBM14A	J1115 04	02A	FO3500	*J1308 80		FO3302	J1309 46		FO3303
VBM21A	J1115 24	12A	FO3500	*J1309 40		FO3303	J1310 04		FO3303
VBM22A	J1115 22	11 A	FO3500	*J1309 36		FO3303	J1310 18		FO3303
VBM23A	J1115 20	10A	FO3500	*J1309 72		FO3303	J1310 48		FO3302
VBM24A	J1115 18	09A	FO3500	J1309 80		FO3303	J1310 46		FO3303
VBM3CA	*J1113 63	33B	FO3603	J1103 65	34B	FO3603			
VBM31A	J1103 11	05 B	FO3200	J1115 38	18A	FO3500	*J1310 40		FO3200
	*J1310 40		FO3303						
VBM32A	J1103 24	13A	FO3200	J1115 36	17A	FO3500	*J1310 36		FO3200
	*J1310 36		FO3303						
VBM33A	J1103 17	08B	FO3200	J1115 34	16A	FO3500	*J1310 72		FO3200
	*J1310 72		FO3302						
VBM34A	J1105 53	28B	FO3603	J1110 41	22B	FO3603	J1113 24	13A	FO3603
	J1115 30	15A	FO3500	*J1310 80		FO3303			
VBM340	*J1105 57	30B	FO3603	J1112 03	02A	FO3603	J1112 04	04A	FO3603
	J1112 74	35B	FO3602	J1113 59	31B	FO3603			
VBPARA	*J1113 66	31A	FO3603	J1114 15	07B	FO3603			
VBPBRA	*J1113 69	35A	FO3603	J1114 03	02A	FO3603			
VBPCAA	*J1112 14	09A	FO3603	J111606	05A	FO3603			
VBPCAJ	*J1114 13	06B	FO3603	J1308 14		FO3302	J1308 66		FO3302
	J1309 14		FO3303	J1309 66		FO3303	J1310 14		FO3303
	J1310 66		FO3303						
VBPCAK	*J1114 11	05B	FO3603	J1113 68	32A	FO3603			
VBPCA0V	*J111608	04A	FO3603	J1114 10	07A	FO3603			
VBPCBA	*J1113 51	27B	FO3603	J1116 04	02A	FO3603			
VBPCBJ	*J1114 07	03A	FO3603	J1308 10		FO3302	J1308 60		FO3302
	J1309 10		FO3303	J1309 60		FO3303	J1310 10		FO3303
	J1310 60		FO3303						
VBPCBK	*J1114 09	04B	FO3603	J1113 65	34B	FO3603			
VBPCB0V	*J1116 03	03A	FO3603	J1114 01	02B	FO3603			
VBPHC0	*J110601	02B	FO3603	J1112 18	10A	FO3603	J1113 23	11B	FO3603
	J1113 47	25B	FO3603	J1114 46	21A	FO3603	J1114 48	22A	FO3603
VBRMCA	*J1113 21	10B	FO3603	J1106 36	17A	FO3402			
VBRMEA	*J1106 22	12A	FO3603	J1116 50	22A	FO3603			
VBRME0V	*J111648	21A	FO3603	J1113 19	O9B	FO3603	J111325	12B	FO3603

Table 5-8. Right Hand Assembly Key Signal Lookup -Continued

Signal	Distribution								
VBRMSA	*J1113 27	13B	FO3603	J1106 31	15B	FO3402			
VBRS30	*J1112 66	31A	FO3302	J1310 25		FO3303			
VBRS60	*J1112 60	28A	FO3302	J1309 25		FO3303			
VBRS90	*J1112 57	30B	FO3302	J1308 25		FO3302			
VBSHFA	*J1113 14	09A	FO3602	J1104 54	25A	FO3602			
VBSHFR	*J1113 22	12A	FO3603	J1102 34	16A	FO3603	J1112 26	14A	FO3603
VBSHFS	*J1112 22	12A	FO3603	J1113 26	14A	FO3603			
VBSMPA	*J1102 45	24B	FO3603	J1105 70	33A	FO3200	J1222 70	33A	FO3200
VBTB1AV	*J1116 07	04B	FO3500	J1115 07	05B	FO3500	J1115 21	11B	FO3500
	J1115 35	17B	FO3500						
VBTB2AV	*J1116 10	06B	FO3500	J1115 05	04B	FO3500	J1115 19	01B	FO3500
	J1115 33	16B	FO3500						
VBTB3AV	*J1116 24	13A	FO3500	J1115 03	03B	FO3500	J1115 17	09B	FO3500
	J1115 31	15B	FO3500						
VBTB4AV	*J1116 25	11A	FO3500	J1115 01	02B	FO3500	J1115 15	08B	FO3500
	J1115 29	14B	FO3500						
VBTDS0V	*J1116 18	09A	FO3500	J1112 31	15B	FO3500	J1112 42	20A	FO3500
	J1113 73	36B	FO3500						
VBTENAV	*J1116 01	02B	FO3500	J1102 36	17A	FO3603	J1111 22	12A	FO3402
	J1112 53	28B	FO3302	J111262	29A	FO3302	J1112 68	32A	FO3302
	J1113 53	28B	FO3603						
VBT1C0	*J1112 72	34A	FO3500	J111371	36A	FO3500			
VBT1FA	*J1113 72	34A	FO3500	J1112 77	38B	FO3500			
VBT1FR	*J1113 75	37B	FO3500	J1112 79	39B	FO3500			
VBT1FS	*J1112 75	37B	FO3500	J1113 79	39B	FO3500	J1118 09	05B	FO3500
VBT1M1C	*J1115 11	07B	FO3500	J111271	36A	FO3500			
VBT1M2C	*J1115 14	06A	FO3500	J111273	36B	FO3500			
VBT2C0	*J1113 38	18A	FO3500	J111240	19A	FO3500			
VBT2FA	*J1112 38	18A	FO3500	J1113 34	16A	FO3500			
VBT2FR	*J1112 30	15A	FO3500	J1113 36	17A	FO3500			
VBT2FS	*J1113 30	15A	FO3500	J1112 36	17A	FO3500	J1118 11	06B	FO3500
VBT2M1C	*J1115 27	13B	FO3500	J1113 40	19A	FO3500			
VBT2M2C	*J1115 26	13A	FO3500	J111342	20A	FO3500			
VBT3C0	*J1113 33	16B	FO3500	J1112 29	14B	FO3500			
VBT3FA	*J1112 33	16B	FO3500	J1113 35	17B	FO3500			
VBT3FR	*J1112 39	19B	FO3500	J1113 37	18B	FO3500			
VBT3FS	*J1113 39	19B	FO3500	J1112 37	18B	FO3500	J1118 15	07B	FO3500

Table 5-8. Right Hand Assembly Key Signal Lookup -Continued

Signal	Distribution								
VBT3M1C	*J1115 39	19B	FO3500	J1113 29	14B	FO3500			
VBT3M2C	*J1115 40	19A	FO3500	J1113 31	15B	FO3500			
VBUNLA	*J1112 09	04B	FO3603	J1113 03	02A	FO3603			
VBUNLR	*J1112 01	02B	FO3603	J110231	15B	FO3603	J111307	03A	FO3603
VBUNLS	*J1113 09	04B	FO3603	J1103 60	28A	FO3603	J1112 05	03B	FO3603
VB0EN0	*J1113 57	30B	FO3603	J1310 34		FO3303	J1310 38		FO3303
	J1310 70		FO3303						
VB25EAV	*J1116 13	06A	FO3603	J1109 46	21A	FO3603			
VB25EK	*J1109 45	24B	FO3603	J1106 05	03B	FO3503			
VB25E0	*J1102 33	16B	FO3603	J110948	22A	FO3603	J1116 11	07A	FO3603
VCLK504	*J1222 45	24B	FO5403	J1102 07	03A	FO3500	J1102 26	14A	FO3602
	J1102 54	25A	FO3500	J1109 52	24A	FO3602	J1124 37	18B	FO3200
	J1323 45		FO5403	J1323 46		FO5403	J1109 52	24A	FO3603
	J1102 50		FO3603						
VCMSL0	*J1106 75	37B	FO3601	J1116 64	33A	FO3601			
VCSEIAV	*J1107 63	30A	FO3602	J1110 56	26A	FO3602			
VCSELJ	*J1110 19	09B	FO3602	J1105 71	36A	FO3603	J1107 62	29A	FO3603
	J1113 05	03B	FO3603						
VCSELK	*J1110 21	10B	FO3602	J1105 05	03B	FO3602	J1107 61	31A	FO3602
	J1113 18	10A	FO3602						
VCSENAY	*J1107 60	28A	FO3603	J1110 46	21A	FO3603			
VC0MPAV	*J1116 78	36A	FO3601	J1106 77	38B	FO3601			
VGND1AV	*J1107 54		FO3500	*J1107 54	25A	FO3601	J1108 13	07A	FO3500
	J1108 25	14A	FO3500	J1108 42	20A	FO3500	J1109 08	06A	FO3603
	J1115 56	26A	FO3601	J1130 50	23A	FO3601	J1107 54	25A	FO3603
VGND2AV	*J1107 43	24B	FO3200	*J1107 43		FO3500	*J1107 43		FO3603
	J1101 05	04A	FO3602	J110905	03B	FO3603	J1114 05	03B	FO3603
	J1115 13	07A	FO3500	J1115 25	14A	FO3500	J1114 42	20A	FO3500
	J1212 30	15A	FO3200						
VGND3AV	*J1116 71		FO3500	*J1116 71	36B	FO3603	J1108 56	26A	FO3500
	J1108 68	33A	FO3500	J1114 08	06A	FO3603	J1118 13	07A	FO3500
VKILM0	*J05 14		FO3401	J1102 06	05A	FO3402	J1103 05	03B	FO3402
	J1111 19	09B	FO3402						
VMFL10	*J1127 74	35B	FO3500	J1118 18	09A	FO3500			
VMFL20	*J1127 20	11A	FO3500	J1118 17	08B	FO3500			
VMILE0	*J05 13		FO3401	J1103 06	05A	FO3402	J1111 01	02B	FO3402
VMRDEA	*J1104 80	39A	FO3601	J1105 74	35B	FO3601			

Table 5-8. Right Hand Assembly Key Signal Lookup -Continued

Signal	Distribution								
VMRRTK	*J1110 23	11B	FO3601	J1104 78	38A	FO3601			
VMRSBAV	*J1107 14	08B	FO3601	J1104 47	25B	FO3402	J110468	32A	FO3602
	J1112 65	34B	FO3602						
VMRSCAV	*J1107 80	38B	FO3601	J1102 30	15A	FO3603	J1102 42	20A	FO3602
	J1103 30	15A	FO3602	J1103 41	22B	FO3603	J1103 42	20A	FO3602
	J1103 52	24A	FO3602	J1103 62	29A	FO3603	J1103 68	32A	FO3603
	J1110 17	08B	FO3602	J1113 04		FO3603			
VMRSTAV	*J1107 13	06A	FO3601	J1104 65	34B	FO3601			
VMRSTR	*J1105 69	35A	FO3601	J1104 74	35B	FO3601			
VMRSTS	*J1104 69	35A	FO3601	J1105 65	34B	FO3601	J1107 17	09B	FO3601
	J1107 79	39B	FO3601	J1110 27	13B	FO3601	J1212 29	13B	FO3200
VMRST0	*J1103 39	19B	FO3601	J1107 11	07A	FO3601			
VRAT1AV	*J1116 63	30A	FO3500	J1108 47	25B	FO3500	J1108 61	31B	FO3500
VRAT10	*J1102 21	10B	FO3500	J1116 55	29B	FO3500	J1116 59	31B	FO3500
	J1116 61	31A	FO3500	J111662	29A	FO3500			
VRAT2AV	*J1116 60	28A	FO3500	J1108 45	24B	FO3500	J1108 59	30B	FO3500
VRAT3AV	*J1116 56	28B	FO3500	J1108 43	23B	FO3500	J1108 55	29B	FO3500
VRAT4AV	*J1116 57	30B	FO3500	J1108 41	22B	FO3500	J1108 53	28B	FO3500
VRAV2AV	*J1107 71	36B	FO3500	J1102 18	10A	FO3500			
VRAV3AV	*J1107 70	34B	FO3500	J1102 19	09B	FO3500			
VRAZHE	*J05 15		FO3401	J1101 28	13B	FO3401			
VRAZHHA	J1101 18	08B	FO3401	*J01 78		FO3401			
VRAZHHB1	*JO11I 22	12B		J1117 20					
VRAZHHC1	*J1101 34	14B	FO3401	J1106 49	26B	FO3402	J1117 24		FO3401
VRDECNA	*J1212 33	16A	FO3200	J1107 74	35A	FO3200			
VRDECNB	*J1212 34	15B	FO3200	J1107 76	37A	FO3200			
VRDECNC	*J1212 31	14B	FO3200	J1107 75	39A	FO3200			
VRD010V	*J1107 72	34A	FO3200	J1104 20	11A	FO3200	J1106 70	33A	FO3200
	J1112 56	26A	FO3200						
VRD020V	*J1107 78	36A	FO3200	J1104 19	09B	FO3200	J1106 64	30A	FO3200
	J1112 50	23A	FO3200						
VRD030V	*J1107 77	38A	FO3200	J1104 25	12B	FO3200	J1106 55	29B	FO3200
	J1112 43	23B	FO3200						
VRENDA	*J1104 51	27B	FO3402	J1103 47	25B	FO3402			
VRENDHA	*J1101 07	06B	FO3401	*J01 75		FO3401			

Table 5-8. Right Hand Assembly Key Signal Lookup -Continued

Signal	Distribution								
VRENDHB1	*J1101 17	17A	FO3401	J1104 49	26B	FO3402	J1105 73	36B	FO3603
	J1106 50	23A	FO3402	J1112 11	05B	FO3402	J1113 20	11A	FO3602
	J1117 25		FO3402	J1222 74	35B	FO3402			
VRENDHC1	*J1101 20	15A		J1117 29					
VRENDHN4	*J1222 69	35A	FO3402	J1102 61	32B	FO3402	J1105 08	06A	FO3602
	J1109 20	11A	FO3402	J1110 52		FO3601	J1110 52	24A	FO3602
	J1113 08	06A	FO3603	J1323 53		FO3402	J1323 55		FO3402
	J1110 52		FO3603						
VREND0	*11112 15	07B	FO3402	J1110 04	04A	FO3402			
VRLDEA	*J1106 46	21A	FO3402	J1105 55	29B	FO3603			
VRLVT0	*J1127 07	03A	FO3402	J02 37		FO3701			
VRMAZAV	*J1107 68	32B	FO3402	J1302 17		FO3402			
VRMAZ0	*J1106 51	27B	FO3402	J1107 65	33B	FO3402			
VRMB1J	*J1110 13	06B	FO3402	J1103 08	06A	FO3402			
VRMB1K	*J1110 11	05B	FO3402	J1102 08	06A	FO3402	J1107 55	29B	FO3402
VRMB10V	*J1107 56	28B	FO3402	J1103 03	02A	FO3402	J1110 01	02B	FO3402
	J1110 05	03B	FO3402						
VRMB2J	*J1110 07	03A	FO3402	J1103 01	02B	FO3402	J1103 10	07A	FO3402
VRMB2K	*J1110 09	04B	FO3402	J1102 10	07A	FO3402			
VRMB3J	*J1109 25	12B	FO3402	J1102 13	06B	FO3402			
VRMB3K	*J110923	11B	FO3402	J1110 08	06A	FO3402	J1110 10	07A	FO3402
VRMCA1U	*J1213 38	18A	FO3402	J1111 14	09A	FO3402	J1111 40	19A	FO3500
VRMCA2U	*J1213 40	19A	FO3402	J1111 34	16A	FO3500			
VRMCA3U	*J1213 42	20A	FO3402	J1111 18	10A	FO3402			
VRMCA4U	*J1213 46	21A	FO3402	J1111 06	05A	FO3402			
VRMCA5U	*J1213 36	17A	FO3402	J1125 64	30A	FO3500	J1216 47	23A	FO3402
VRMCBA	*J1113 15	07B	FO3500	J1107 51	27B	FO3500			
VRMCB0V	*J1107 53	26B	FO3500	J1125 61	31B	FO3500			
VRMCB1U	*J1216 38	18A	FO3402	J1111 07	03A	FO3402	J1111 20	11A	FO3402
	J1111 31	15B	FO3500						
VRMCB2U	*J121640	19A	FO3402	J1111 08	06A	FO3402	J1111 30	15A	FO3500
VRMCB3U	*J1216 42	20A	FO3402	J1111 04	04A	FO3402			
VRMCB4U	*J1216 46	21A	FO3402	J1111 24	13A	FO3402			
VRMCB5U	*J1216 36	17A	FO3402	J1113 13	05B	FO3500			
VRMC00	*J1106 30	15A	FO3402	J1125 51	25B	FO3500	J1213 37	17B	FO3402
	J1216 37	17B	FO3402						
VRMINA	*J1104 63	33B	FO3402	J1302 39		FO3402			

Table 5-8. Right Hand Assembly Key Signal Lookup -Continued

Signal	Distribution								
VRMI1A	*J1102 11	05B	FO3402	J1106 41	22B	FO3402			
VRM12A	*J1103 04	04A	FO3402	J1106 43	23B	FO3402			
VRM130	*J1106 45	24B	FO3402	J1104 59	31B	FO3402			
VRMKBA	*J1103 07	03A	FO3402	J1107 59	31B	FO3402			
VRMKB0V	*J1107 57	30B	FO3402	J1109 24	13A	FO3402			
VRMKMA	*J1111 23	11B	FO3402	J1105 78	38A	FO3402			
VRMMLA	*J1111 11	05B	FO3402	J1105 76	37A	FO3402			
VRMRMAV	*J1107 63	09A	FO3402	J1106 47	25B	FO3402			
VRMRM0	*J1105 80	39A	FO3402	J1104 53	28B	FO3402	J1104 61	32B	FO3402
	J1107 20	10A	FO3402						
VRMR1A	*J1104 60	28A	FO3402	J1103 45	24B	FO3402			
VRMR2AV	*J1107 66	32A	FO3402	J1125 49	24B	FO3502	J1213 35	16B	FO3402
	J1216 35	16B	FO3402						
VRMR20	*J1103 51	27B	FO3402	J1107 26	33A	FO3402			
VRMSTA	*J1104 57	30B	FO3402	J1222 49	26B	FO3402			
VRMST04	*J1222 47	25B	FO3402	J1104 64	30A	FO3402	J1109 22	12A	FO3402
	J1110 06	05A	FO3402	J1323 56		FO3402	J1323 61		FO3402
VRMS00	*J1106 33	16B	FO3402	J1104 55	29B	FO3402	J1104 62	29A	FO3402
VRRCP0	*J1112 80	39A	FO3601	J1113 76	37A	FO3601			
VRRCP1C	*J1115 51	27B	FO3601	J111276	37A	FO3601			
VRRCP2C	*J1115 54	25A	FO3601	J1112 78	38A	FO3601			
VRRDY0	*J1224 06	05A	FO3601	J1230 36	16A	FO2500			
VRRG0HA	J1101 06	04B	FO3601	*J01 74		FO3601			
VRRG0HB1	*J1101 38	20A	FO3601	J1117 23		FO3601			
VRRG0HC1	*J1101 30	18A	FO3601	J1117 26		FO3601	J1222 78	38A	FO3601
VRRG0HN4	*J1222 76	37A	FO3601	J1104 76	37A	FO3601	J1105 04	04A	FO3602
	J1110 22	12A	FO3601	J1113 04	04A	FO3602	J1323 51		FO3601
	J1323 52		FO3601	J1110 22	12A	FO3602			
VRRMRA	*J1106 69	35A	FO3601	J1103 35	17B	FO3601			
VRRSFA	*J1113 80	39A	FO3601	J1116 45	25B	FO3601			
VRRSF0V	*J1116 43	24B	FO3601	J1106 74	35B	FO3601	J1130 54	25A	FO3601
VRR18A	*J1113 60	28A	FO3601	J1116 41	23B	FO3601			
VRR180	*J1116 46	22B	FO3601	J1113 78	38A	FO3601			
VRR19AV	*J1116 14	08B	FO3601	J1110 79	39B	FO3601	J1113 64	30A	FO3601
VRR19J	*J1110 78	38A	FO3601	J1113 62	29A	FO3601			
VRSMP0	*J1105 66	31A	FO3200	J110966	31A	FO3200	J111422	12A	FO3200

Table 5-8. Right Hand Assembly Key Signal Lookup -Continued

Signal	Distribution								
VRSMP04	*J1222 59	31B	FO3200	J1109 75	37B	FO3200	J1114 38	18A	FO3200
	J1323 47		FO3200	J1323 48		FO3200	J1109 75	37B	FO2502
VRVMCN	J1302 69		FO3100	J1304 70		FO3100			
VRVMDN	*J1302 01		FO3100	*J1304 01		FO3100			
VRVMRA	J1302 06		FO3100	*J1302 25		FO3402			
VRVM1A	J1108 52	24A	FO3500	J1114 26	14A	FO3200	J1116 38	20A	FO3200
	*J1304 80		FO3100						
VRVM1K	*J1114 23	11B	FO3200	J1212 27	14A	FO3200			
VRVM10V	*J1116 40	19A	FO3200	J1114 24	13A	FO3200			
VRVM2A	J1108 50	23A	FO3500	J1114 14	09A	FO3200	J1116 35	18A	FO3200
	*J1304 72		FO3100						
VRVM2K	*J1114 21	10B	FO3200	J1212 26	13A	FO3200			
VRVM20V	*J1116 37	17A	FO3200	J1114 18	10A	FO3200			
VRVM3A	J1108 48	22A	FO3500	J111442	20A	FO3200	J111636	16A	FO3200
	*J1304 78		FO3100						
VRVM3K	*J1114 35	17B	FO3200	J1212 24	12A	FO3200			
VRVM30V	*J1116 34	15A	FO3200	J1114 40	19A	FO3200			
VRVM4A	J1108 46	21A	FO3500	J1108 57	28A	FO3500	J1114 30	15A	FO3200
	J1116 29	15B	FO3200	*J1304 74		FO3100			
VRVM4K	*J1114 33	16B	FO3200	J1212 19	09B	FO3200			
VRVM40V	*J1116 30	14B	FO3200	J1114 34	16A	FO3200			
VRVM5A	J1108 64	31A	FO3500	J1109 70	33A	FO3200	J1116 33	17B	FO3200
	*J1302 80		FO3100						
VRVM5K	*J1109 59	31 B	FO3200	J1212 21	10B	FO3200			
VRVM50V	*J1116 31	16B	FO3200	J1109 68	32A	FO3200			
VRVM6A	J1108 62	30A	FO3500	J1109 60	28A	FO3200	J1116 39	19B	FO3200
	*J1302 72		FO3100						
VRVM6K	*J1109 57	30B	FO3200	J1212 23	11B	FO3200			
VRVM60V	*J1116 42	18B	FO3200	J1109 62	29A	FO3200			
VRVM7A	J1108 60	29A	FO3500	J1109 79	39B	FO3200	J1116 52	26A	FO3200
	*J1302 78		FO3100						
VRVM7K	*J1109 76	37A	FO3200	J1212 25	12B	FO3200			
VRVM70V	*J1116 54	25A	FO3200	J1109 77	38B	FO3200			
VRWENA	*J1102 59	31B	FO3402	J1127 01	02B	FO3402			
VRWVDAV	*J1116 66	32A	FO3601	J1103 29	14B	FO3602	J1103 40	19A	FO3602
	J1103 53	28B	FO3603	J1103 66	31A	FO3603	J1109 50	23A	FO3602
	J1112 61	32B	FO3602	J1113 61	32B	FO3603	J1109 50	23A	FO3603

Table 5-8. Right Hand Assembly Key Signal Lookup -Continued

Signal	Distribution								
VRWVD0	*J05 16		FO3401	J1102 68	32A	FO3402	J1106 48	22A	FO3402
	J1106 53	28B	FO3200	J1106 62	29A	FO3200	J1106 68	32A	FO3200
	J1116 76	37A	FO3601	J1223 01	02B	FO2200			
VTBITR	*J1106 72	34A	FO3500	J1112 47	25B	FO3500			
VTBITS	*J1112 51	27B	FO3500	J1106 73	36B	FO3500	J1107 29	15B	FO3500
	J1107 33	17B	FO3500	J1107 35	18A	FO3500	J1107 36	16A	FO3500
	J1116 09	05B	FO3500	J1116 15	07B	FO3500	J111622	14A	FO3500
	J1116 23	12A	FO3500						
VTCMT1U	*J1125 54	26A	FO3500	J1102 49	26B	FO3500	J1107 15	07B	FO3500
	J1112 23	11B	FO3500						
VTCMT2U	*J1125 56	28B	FO3500	J1102 04	04A	FO3500	J1102 52	24A	FO3500
	J1107 22	14A	FO3500	J1111 37	18B	FO3500			
VTCN1AV	*J1107 10	06B	FO3500	J1102 01	02B	FO3500	J1111 36	17A	FO3500
VTCN2AV	*J1107 24	13A	FO3500	J1106 61	32B	FO3500	J1106 78	38A	FO3500
	J1112 25	12B	FO3500						
VTDTSA	*J1102 09	04B	FO3500	J1107 39	19B	FO3500	J1116 20	10A	FO3500
VTESE0	*J1106 14	09A	FO3500	J1104 34	16A	FO3500	J1104 35	17B	FO3500
	J1105 48	22A	FO3500	J1107 05	03B	FO3500	J1112 34	16A	FO3500
	J1112 35	17B	FO3500	J1113 77	38B	FO3500	J1116 05	03B	FO3500
	J1124 36	17A	FO3200						
VTESTA	*J1102 47	25B	FO3500	J1103 23	11B	FO3500			
VTESTD4	*J1232 06	05A	FO3500	J04 38		FO3500			
VTESTR	*J1103 27	13B	FO3500	J1105 43	23B	FO3500	J1106 07	03A	FO3602
	J1106 26	14A	FO3603	J1327 71	36A	FO2602			
VTESTS	*J1105 45	24B	FO3500	J1103 25	12B	FO3500	J1106 59	31B	FO3500
	J1106 76	37A	FO3500	J1113 11	05B	FO3500	J1232 08	06A	FO3500
VTEST1X	*J1118 04	02A	FO3500	J1314 03	02B	FO5203			
VTIBTA	*J1112 27	13B	FO3500	J1105 17	08B	FO3301	J1105 18	01A	FO3301
	J1105 23	11B	FO3301	J1105 47	25B	FO3301	J1106 37	18B	FO3302
	J1113 41	22B	FO3302	J1113 48	22A	FO3302	J1113 54	25A	FO3302
VTRAD0T	*J1213 08	04A	FO3500	J1302 59		FO3100	J1304 59		FO3100
VTRAD1T	*J1213 10	05A	FO3500	J1302 26		FO3100			
VTRAD2T	*J1213 14	06A	FO3500	J1302 31		FO3100			
VTRAD3T	*J1213 13	07A	FO3500	J1302 24		FO3100			
VTRAD4T	*J1213 17	08B	FO3500	J1302 27		FO3100			
VTRAD5T	*J1213 07	04B	FO3500	J1304 26		FO3100			
VTRAD6T	*J1213 09	05B	FO3500	J1304 31		FO3100			

Table 5-8. Right Hand Assembly Key Signal Lookup -Continued

Signal	Distribution								
VTRAD7T	*J1213 11	06B	FO3500	J1304 24		FO3100			
VTRAD8T	*J1213 15	07B	FO3500	J1304 27		FO3100			
VTRAD9T	*J1213 18	09A	FO3500	J1302 68		FO3100	J1304 68		FO3100
VTRV11C	*J1108 51	27B	FO3500	J1127 65	34B	FO3500			
VTRV12C	*J1108 54	25A	FO3500	J1127 71	36A	FO3500			
VTRV21C	*J1108 65	33B	FO3500	J1127 22	12A	FO3500			
VTRV22C	*J1108 66	32A	FO3500	J1127 24	13A	FO3500			
VTSPLA	*J1111 35	17B	FO3500	J1112 49	26B	FO3500			
V0D01A	*J1106 66	31A	FO3200	J1103 13	06B	FO3200			
V0D02A	*J1106 60	28A	FO3200	J1103 26	14A	FO3200			
V0D03A	*J1106 57	30B	FO3200	J1103 18	10A	FO3200			
V0D1B0E	*J1124 35	17B	FO3200	J1232 04	04A	FO3200			
V0D1B1E	*J1124 39	19B	FO3200	J1232 03	02A	FO3200			
V0D1B2E	*J1124 42	20A	FO3200	J1232 11	05B	FO3200			
V0D11AV	*J1107 49	23A	FO3200	J1124 31	15B	FO3200			
V0D110	*J1103 15	07B	FO3200	J1107 47	24A	FO3200			
V0D12AV	*J1107 48	21A	FO3200	J1124 29	14B	FO3200			
V0D120	*J1103 20	11A	FO3200	J1107 50	22A	FO3200			
V0D13AV	*J1107 46	22B	FO3200	J1124 30	15A	FO3200			
V0D130	*J1103 19	09B	FO3200	J1107 41	23B	FO3200			
V0D21D4	*J1232 01	02B	FO3200	J02 39		FO3200	J1231 05		FO3200
V0D22D4	*J1232 09	04B	FO3200	J02 40		FO3900	J1231 07	FO3200	
V0D23D4	*J1232 15	07B	FO3200	J02 42		FO3900	J1231 09	FO3200	
8ZIF10	*J01 54		FO3100	J1304 18		FO3100			
8ZN010	*J01 55		FO3100	J1304 52		FO3100			
8ZPR10	*J01 62		FO3100	J1304 06		FO3100			
8ZSA10	*J01 66		FO3100	J1302 42		FO3100			
8ZSB10	*J01 67		FO3100	J1302 52		FO3100			
8ZSP10	*J01 60		FO3100	J1304 42		FO3100			
8ZTE10	*J01 59		FO3100	J1302 18		FO3100			

Section III. ALTERABLE PROCESSOR

5-8. General (fig. 5-4). The alterable processor (AP) consists of the following eight sections:

High speed input buffer
Low speed input/output (I/O) logic
Arithmetic logic
Data file storage and address logic
8-input multiplexer (mux)
Program memory and command register
High speed output buffer
Timing and control

The AP is a special-purpose miniprocessor designed and programmed to discern ADP input messages for displayability for the particular console and properly process the screened information for ultimate video display. The AP determined displayability by utilizing information from the front panel switch settings. In addition, the AP compiles and transmits console status reports to the ADP. The DOU, contained in the ADP, provides synthetic video to refresh the console displays at a rate of 20 times per second or once every 50 ms. A maximum of 47 ms is required to transmit the synthetic video (also referred to as the display refresh file) to online consoles. The remainder of the 50 ms. Is utilized by the AP to receive, process, and transmit console status information to and from the front panel and the computer buffer/C-BIT. The AP utilizes a miniprocessor to transfer and manipulate the synthetic video and status information. Information is transferred throughout the AP, as for the entire display console, in the form of 16-bit words. A repertoire of 32 instructions provides the carious data transmission, logical, arithmetic, branch, and miscellaneous routines required. A 1024-word programmable read-only memory (PROM) stores the programmed sequence of instructions that control all operations. The AP program listing and additional descriptive information is provided in section XIV. A 256-word PROM is provided to store constraints and tables. This read-only storage is augmented by a storage of various resultants obtained during message processing.

a. *High Speed Input Buffer*. During normal operation, the synthetic video is supplied to the high speed input buffer from the DOU. This device is a direct multiplexed accessor, processing information directly from the computer memory. The high speed input buffer checks the 8-bit byte input for the start-of-word sync bit and proper parity. The 8-bit bytes are compiled into 16-bit words and temporarily stored for further processing by the AP. This processing is dependent upon control signals between the high speed input buffer and timing and control.

b. *Low Speed I/O Logic*. The low-speed I/O logic provides bidirectional low speed data transmission between the AP and the computer buffer/C-BIT or the front panel. This circuit identifies the type of transmission by generating the enable or command signals and utilizes the appropriate acknowledgment (request or indicator) to ensure proper data transfer.

c. *Arithmetic Logic*. The arithmetic logic provides all the logical, arithmetic, comparative, and shifting manipulation of data for the AP. The arithmetic logic processes data in 16-bit parallel mode with simple operations (addition , subtractions, AND, OR, etc) requiring 200 ns and more time-consuming operations (multiplication) requiring up to approximately 2 us.

d. *Data File Storage and Address Logic*. The data file storage and address logic contains the addressable 256-word constant PROM and the 128-word scratchpad RAM. The memories are addressed by the index counter/register which can be decremented sequentially or loaded with a new address from the command register output in the event of an indexing instruction.

e. *8-Input Mux*. The 8-input mux routes one of eight information sources to various AP functional circuits. The 8-input mux output is the data bus which is the primary path for AP data transmission.

f. *Program Memory and Command Register*. The program memory and command register contains the 1024-word program memory which stores the AP sequence of instructions. The program address counter can be incremented sequentially or loaded from the data bus. This counter is incremented or loaded at the end of each instruction cycle by the advance pulse. The command register stores the current operational code and utility field for decoding by timing and control.

g. *High Speed Output Buffer.* The high speed output buffer provides temporary storage for the high-speed data being transmitted to the display buffer.

h. *Timing and Control*. Timing and control contains the primary timing and instruction decode logic required by the AP to properly process the current instruction. The advance command indicates the termination of a current instruction and the initiation of the succeeding one. The advance command steps the command register, the output of which is decoded to provide the instruction indication and supplementary information which specifies or amends the instruction. Timing and control then generates a sequence of timing signals, the number and duration of which are dependent upon the complexity of the instruction. For certain instructions, the timing and control supplies a bus select code to the 8-bit mux identifying the source of information for the current instruction.

5-9. High Speed Input Buffer Detailed Description (fig. 5-5). The high speed input buffer consists of the following elements:

Input logic
Read/write memory and output register
Read/write address counter
Control logic

The high speed input buffer accepts the display refresh data from the DOU, generates the timing sequence required to write the data into a bipolar memory and, subsequently, to read the data for AP processing. The DOU inputs consist of eight data lines, one parity bit, and one sync bit. Each two sequential 8-bit bytes are assembled, stored, and read out as a 16-bit word. The maximum input transfer rate is 163,840 words/second, or one byte every nominal 2.75 us. The 8-bit byte plus parity is sensed by the input logic. The presence of the sync bit identifies the current data as the initial byte of the 32-bit word. Since the 8-bit data, plus parity input, must reflect odd parity, a signal on any of these lines generates the data present signal, which enables the control logic to commence the word storage sequence. The control logic senses the sync bit and enables the read/write memory and output register to store the current content of the input logic. The input logic also checks the initial byte of each message for proper parity status and supplies this status to the read/write memory. The input buffer is then cleared in preparation for the second byte. The second byte is sensed by the control logic and an even load signal is generated. The control logic then initiates the sequence required to write the 1 6-bit word into memory. The read/write enable signals, in conjunction with the read/write memory address, develop the proper sequence of control signals to ensure that the input words are written into memory and then made available to the output register on a FIFO basis. The input words are written into memory synchronously as received. The stored words are read from memory asynchronously as required for processing. The control logic monitors the write and read operations to ensure that an input word is not written over an unprocessed read word. Should the read/write memory capacity be approached, the input buffer almost-full signal will generate an inhibit signal to the DOU through the computer buffer/C-BIT logic to halt DOU data transmission. The read sync output informs the AP of the current control logic mode (read or write).

a. *Input Logic Jig. 5-6 FO-1)* The nine information lines from the DOU are applied to the ac coupled 1/0 circuit. The resultant levels are gated through the input buffer mux, by a computer buffer/C-BIT input buffer enable signal, to the inputs of the input buffer latches. A signal present on any of the data or parity latches generates the DOU data level to the control logic, initiating the word storage sequence. A sync bit signal to the control logic and control word detect circuit identifies the current data as the initial byte of a 4-byte word. When the input byte has been transferred to the read/write memory and output register, the input buffer latches are cleared by the control logic in preparation for the next byte. The logic checks each initial byte of each new message for proper parity. The byte load input to the control word detect circuit goes high each time an odd byte is loaded from the input logic. The coincidence of the sync bit and a data ONE in input bit O indicating a new message) sets the control word detect circuit. This allows the parity check circuit to check the 9-bit input for proper parity. A high level to the read/write memory and output register indicates proper parity. The input buffer enable level from the computer buffer/C-BIT to the input buffer mux remains low except when the DOU inhibit is active or when the console is in the radar only display mode. The device maintenance input goes high when the console is placed in the test mode. This permits the input buffer mux to accept the data, parity, and sync bit from the computer buffer/C-BIT.

b. *Read/Write Memory and Output Register (fig. 5-7, FO-2).* The read/write memory and output register contains the even and odd byte input buffers which assemble the input word, the bipolar read/write memory, and the output register which stores the word for subsequent processing.

(1) Even and odd byte input buyers. Each byte latched by the input logic is supplied to the odd and even byte input buffers. An odd byte load signal from the control logic stores the first byte in the odd byte input buffer. An even byte load signal loads the second byte into the even byte input buffer. A high display message format level indicates that the current word is legitimate and may be processed. A low display message level, which is detected by the even parity mux and even byte input buffer, causes the 4 LSBs of the input even byte to be forced to zero. This prevents the AP from processing the current message.

(2) Bipolar read/write memory. The address counter chip select signal selects one *of* two groups of eight chips in the bipolar read/write memory. The read/write address counter memory address signal selects 1 of the 16 memory locations in that group. The control logic write enable signal determines the current mode of operation. The write enable signal, when high, transfers the contents of the even and odd byte input buffers into the addressed memory location. The write enable signal, when low, supplies the word contained in the addressed memory location to the output register. When the read enable signal goes low, the word is stored in the output register. The word is then available to the AP 8-input mux for processing. The bipolar read/write memory comprises eight memory chips. Each chip is self-contained and includes an address buffer, address decoder, a 16-word by 4-bit memory cell, and write and sense amplifiers. The eight memory chips are arranged in two groups of four each. Each group of 4 provides storage for 16 words of 16 bits each, with each chip storing 4 bits.

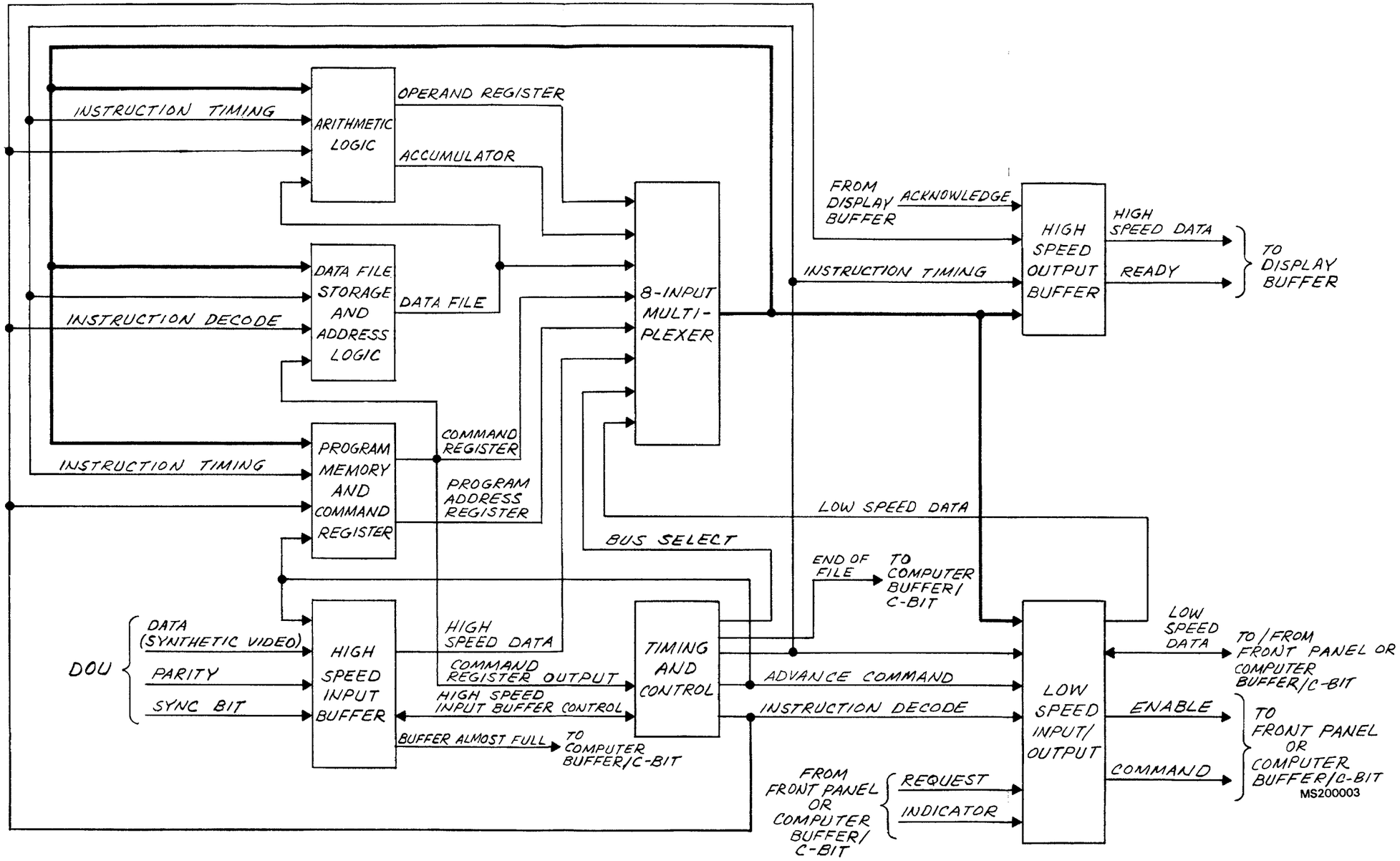

Figure 5-4. Alterable Processor Block Diagram

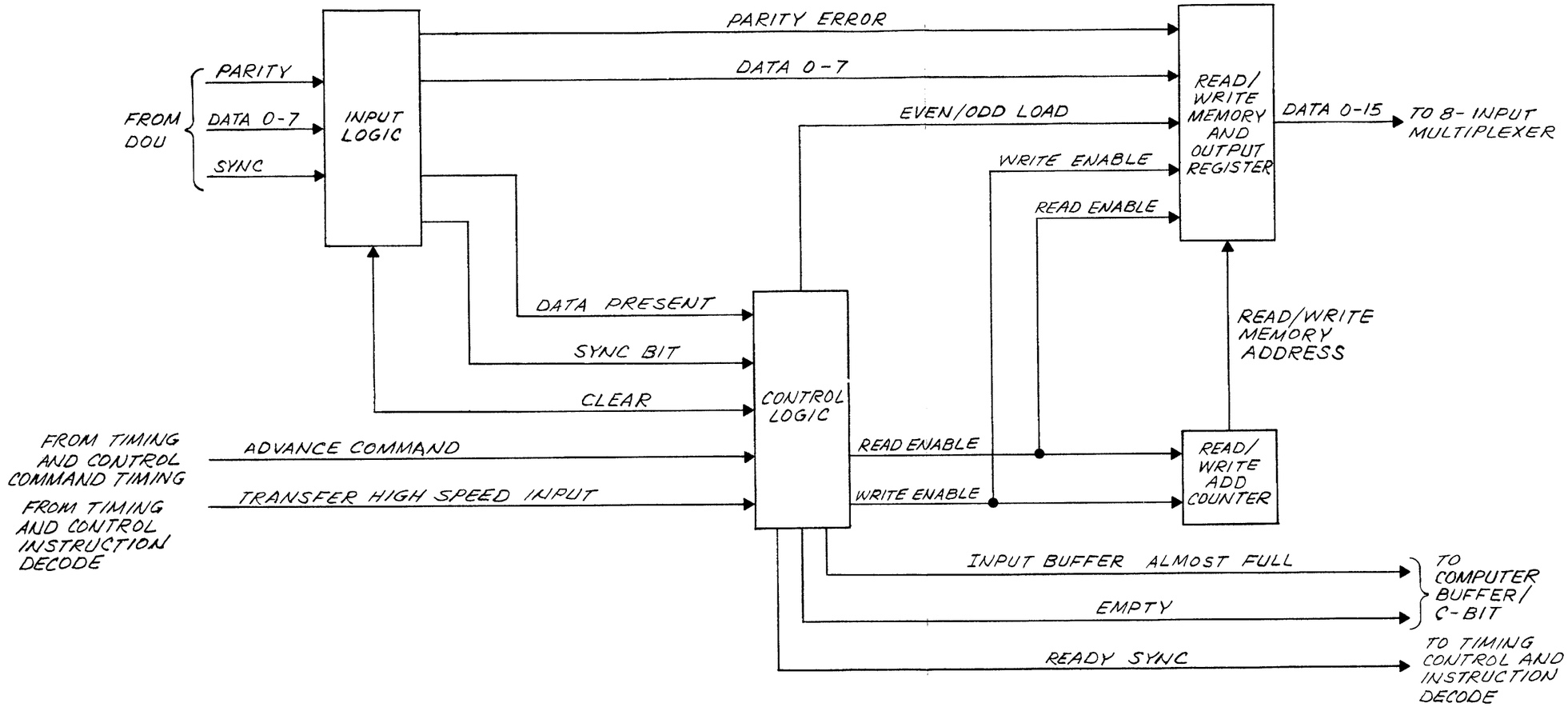

Figure 5-5. High Speed Input Buffer Block Diagram

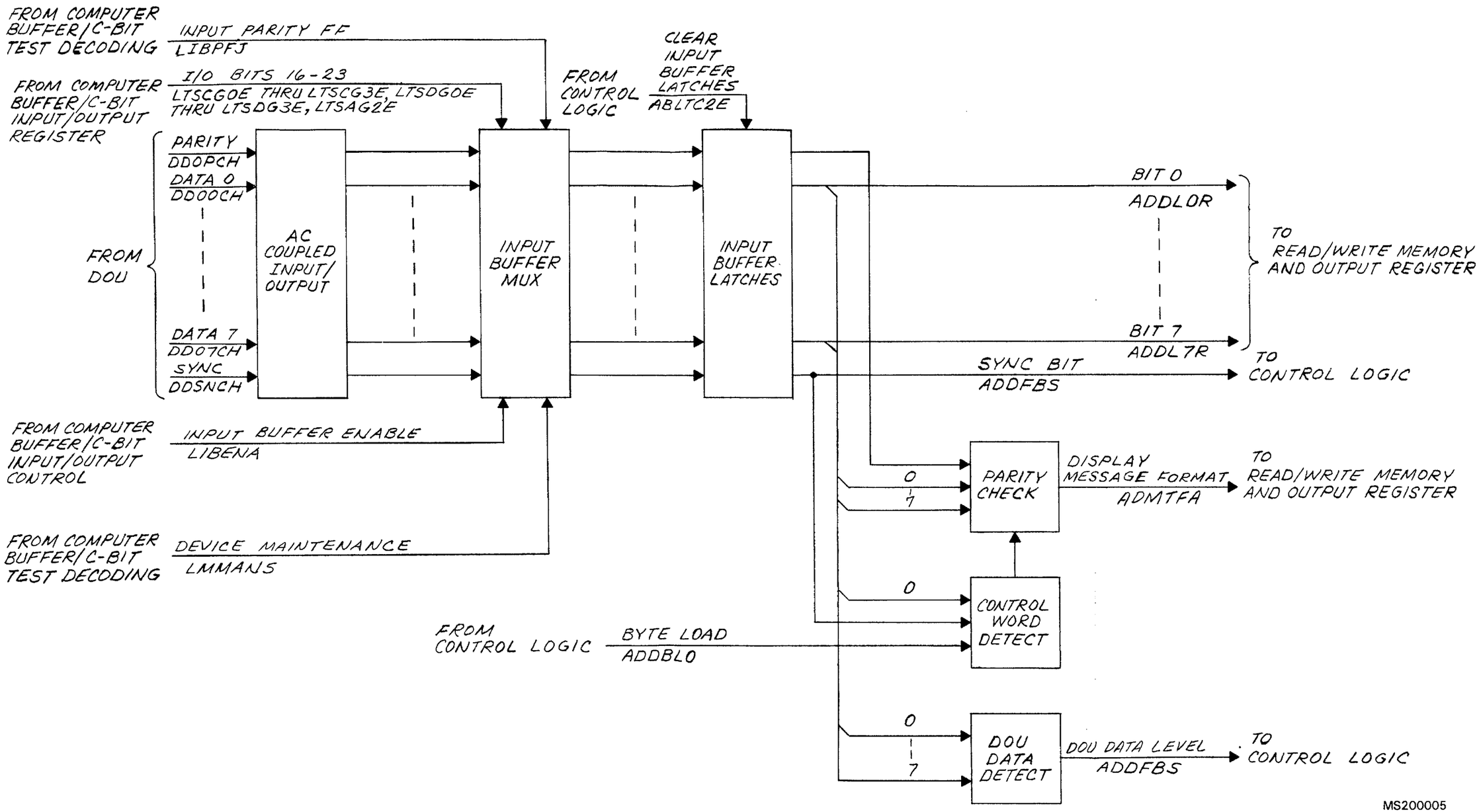

Figure 5-6. High Speed Input Buffer Input Logic Block Diagram

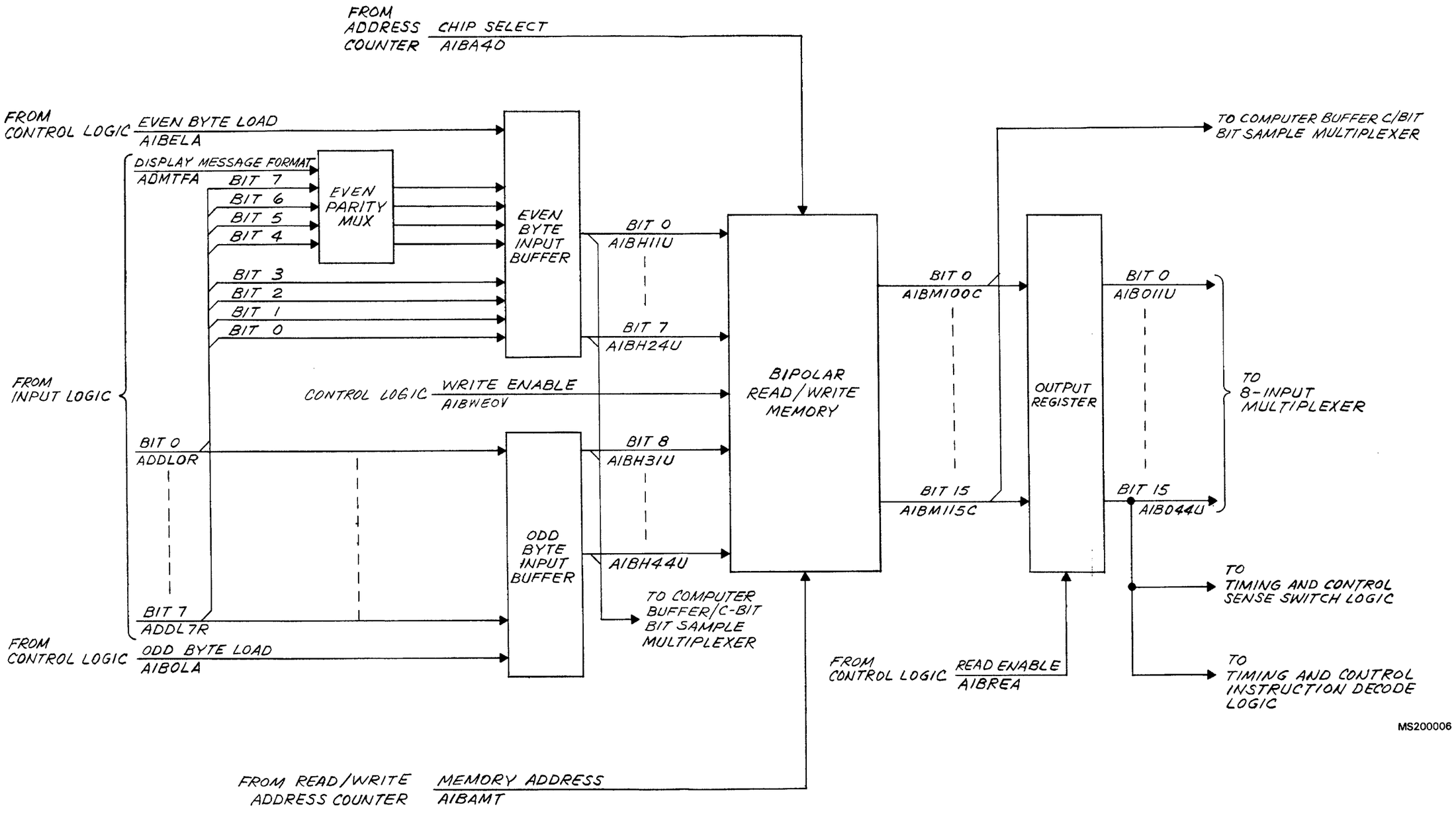

Figure 5-7. High Speed Input Buffer Read/Write Memory and Output Register Block Diagram

The 2 groups of 8 chips provide storage for 32 words of the display refresh file. The computer buffer/C-BIT, during the maintenance mode of operation, samples bits from the bipolar read/write memory and odd/even byte input buffers.

c. Read/Write Address Counter (fig. 5-8, FO-3). The read/write address counter generates the binary read and write addresses and forwards the selected address to the read/write memory and output register. The read and write counter circuits are functionally identical; therefore, only the write circuit is described. Counting is enabled by the concurrence of the write enable and write address bit 4 signals from the control logic. These signals are coincident every other write routine for one clock pulse time. The three counter LSBs are reversed and combined with write address bit 4 to provide the required memory addressing sequence, as illustrated in table 5-9. When the select read address signal is low, the write memory address is gated through the memory address mux to the read/write memory and output register. Write register bit 4 is combined with the counter MSB to determine which group of 16 out of 32 memory chips is currently being selected.

d. *Control Logic (fig 5-9, FO-4).* The control logic generates the timing sequence required to address the input buffer memory and to transfer the input data to and from the memory. This circuit also monitors the addressing logic to prevent stored data from being destroyed before it is processed. The timing diagram (fig. 5-10) illustrates the sequence of input data processing. In order to maintain the maximum transfer rate for data from the DOU, the control logic responds immediately by initiating a write routine when an input data byte is sensed. A read routine is dependent upon the time required by the AP to process each 16-bit word and is asynchronous with the input data. Since only one memory location is addressed at one time and the current read and write address differs, parallel logic is provided for the two functions. Logic interlocking is provided to ensure that a write routine prevails.

(1) Data detect and timing register. When an initial data byte is latched in the input buffer (DOU data signal active), the data detect and timing register initiates a 2-count control cycle. The initial count, in conjunction with the active sync bit level from the input logic, is applied to the odd/even load circuit and is gated to the read/write memory and output register as the odd byte load signal. The second count clears the input logic data latches. The second data byte, which is applied to the odd/even load circuit, generates the even byte load signal to the read/write memory register. The second data byte also generates an input buffer load signal to the word detect, indicating that a 1 6-bit word has been received. This signal initiates the write routine. The write routine signal is applied to the address delay circuit which energizes the address select latch. The delay is required to permit the memory address to be incremented to the proper write address. The address delay signal enables the address valid circuit to be enabled by the succeeding clock pulse. The address select latch, in conjunction with the active address valid circuit, generates the write enable signal. The write enable signal is then sent to the read/write address counter and the read/write memory and output register, transferring the 1 6-bit word from the input register to the selected location in the read/write memory. The write enable signal allows the write address bit 4 circuit to be toggled by each succeeding write routine. This signal is used in the read/write address counter to develop the MSB (bit 4) of the write address.

(2) AP timing and control command timing logic. The AP timing and control command timing logic initiates a read routine by forwarding the advance command and transfer high speed input signals to the input buffer ready and input ready sync circuits. This initiates a read address sequence similar to that described for the write routine. However, since the address select latch remains off, a read address select and, subsequently, a read enable is generated. The read enable signal transfers the word currently stored in the selected memory location to the output register and increments the read address counter. The read enable signal is also applied to the input buffer ready, which enables the input ready sync to prepare the logic for the next read routine. In the event that a write and read routine occur simultaneously, the condition of the address select ensures that the write routine prevails.

(3) Write and read memory addresses. The write and read memory addresses are monitored by the file address control, which utilizes an eight-stage, up-down counter. This counter is incremented for each write operation and decremented for each read operation. When the file address control reaches a count of 28, which indicates that the write address is approaching a memory location containing unprocessed data, an input buffer-almost-full signal is forwarded to the computer buffer/C-BIT, AP, and DOU interface circuit. The resultant inhibit signal to the DOU will temporarily halt input data transfer.

(4) File address control. The file address control is also monitored by the input buffer not reading logic. When sufficient read data is processed, the empty level signal is activated. The empty level signal or the input buffer ready level will generate the input buffer not reading signal, indicating that the DOU may reinitiate input data transmission.

5-10. Low Speed Input/Output Logic Detailed Description (fig. 5-11, FO-5). The low speed I/0 logic consists of the following elements:

Low speed input acknowledge set
Set output enable
Set enable flip-flop
Channel number circuit

Table 5-9. Counter/Memory Address Conversion

Memory address	Address counter A	B	C	D	AIBXOJ	Memory address D	C	B	A	Chip select
1	0	0	0	1	1	0	0	0	1	2
2	1	0	0	0	0	0	0	1	0	2
3	1	0	0	0	1	0	0	1	1	2
4	0	1	0	0	0	0	1	0	0	2
5	0	1	0	0	1	0	1	0	1	2
6	1	1	0	0	0	0	1	1	0	2
7	1	1	0	0	1	0	1	1	1	2
14	1	1	1	0	0	1	1	1	0	2
15	1	1	1	0	1	1	1	1	1	2
0	0	0	0	1	0	0	0	0	0	1
1	0	0	0	1	1	0	0	0	1	1
2	1	0	0	1	0	0	0	1	0	1
3	1	0	0	1	1	0	0	1	1	1
4	0	1	0	1	0	0	1	0	0	1
14	1	1	1	1	0	1	1	1	0	1
15	1	1	1	1	1	1	1	1	1	1
0	0	0	0	0	0	0	0	0	0	2
1	0	0	0	0	1	0	0	0	1	2
2	1	0	0	0	0	0	0	1	0	2

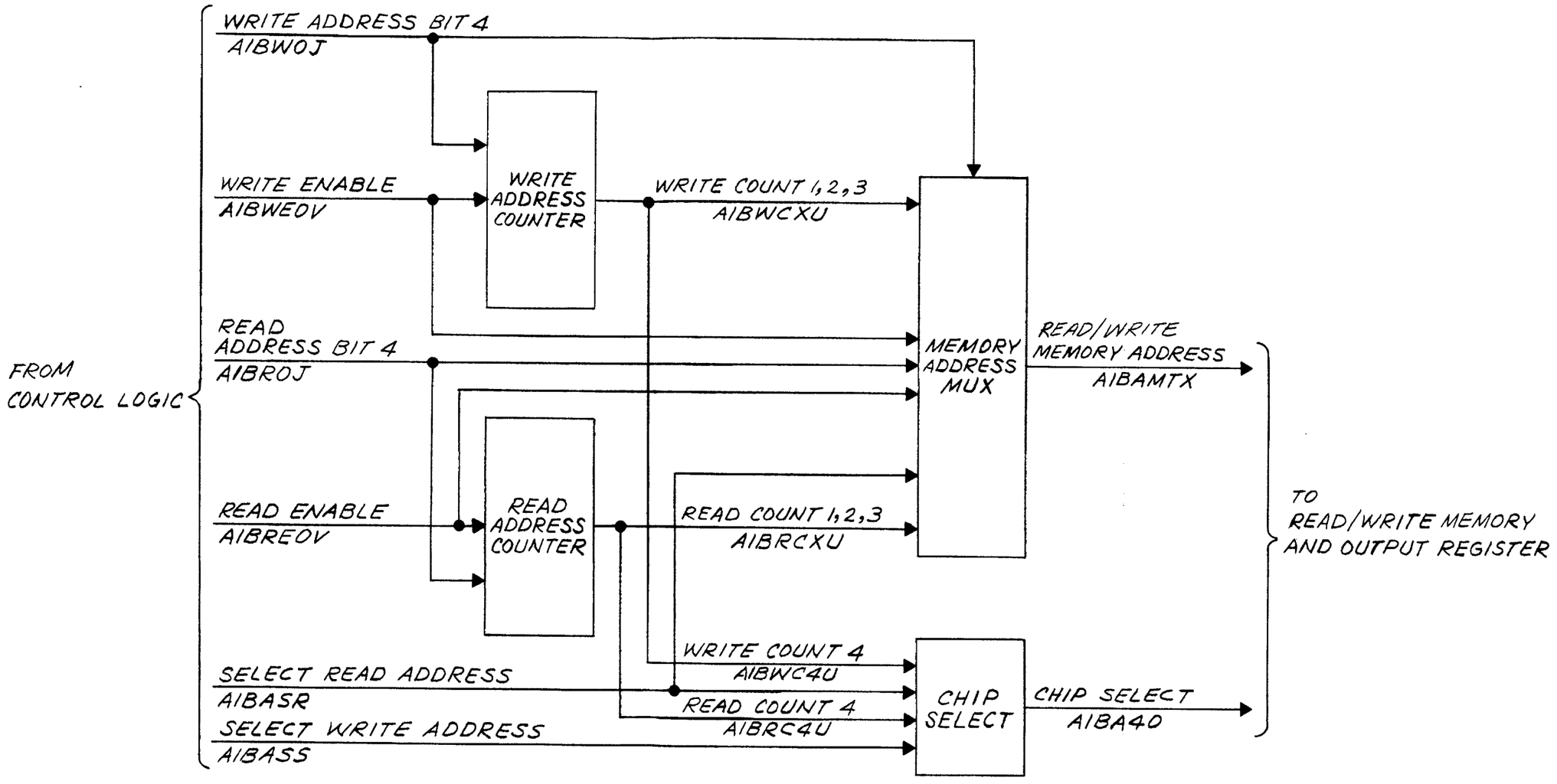

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Figure 5-8. High Speed Input Buffer Read/Write Address Counter Block Diagram

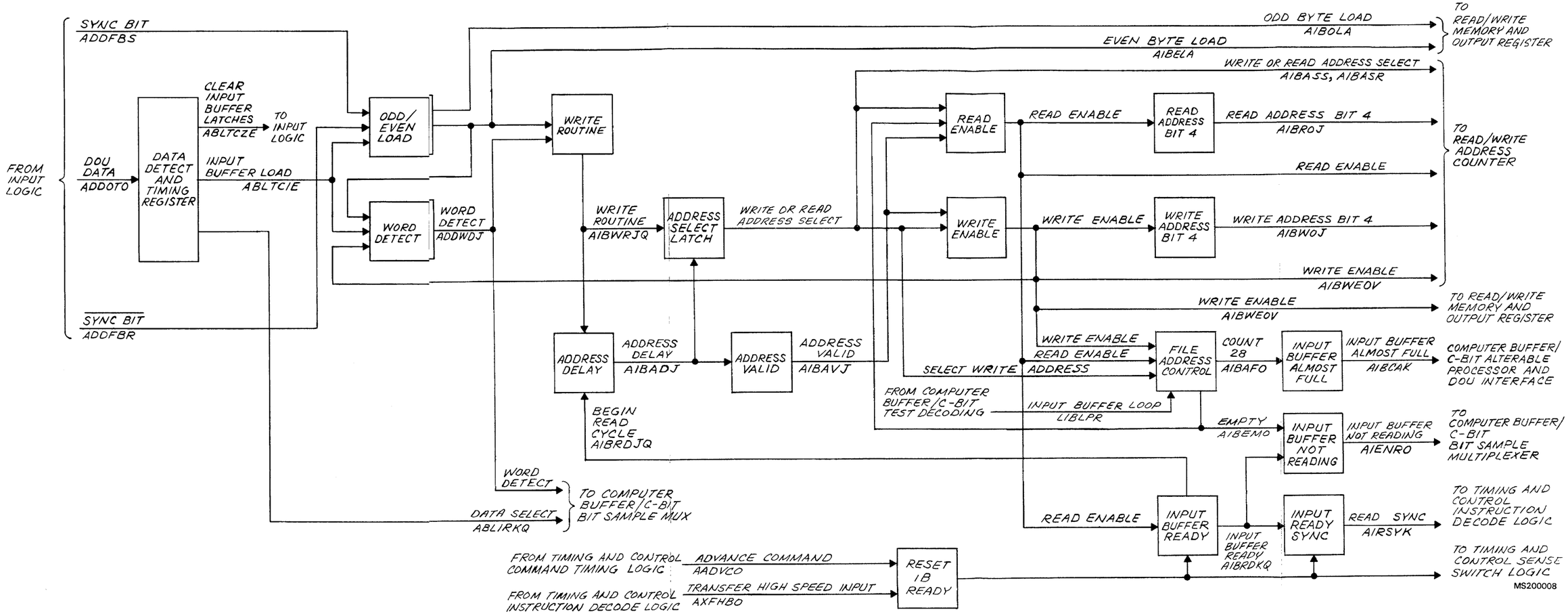

Figure 5-9. High Speed Input Buffer Control Logic Block Diagram

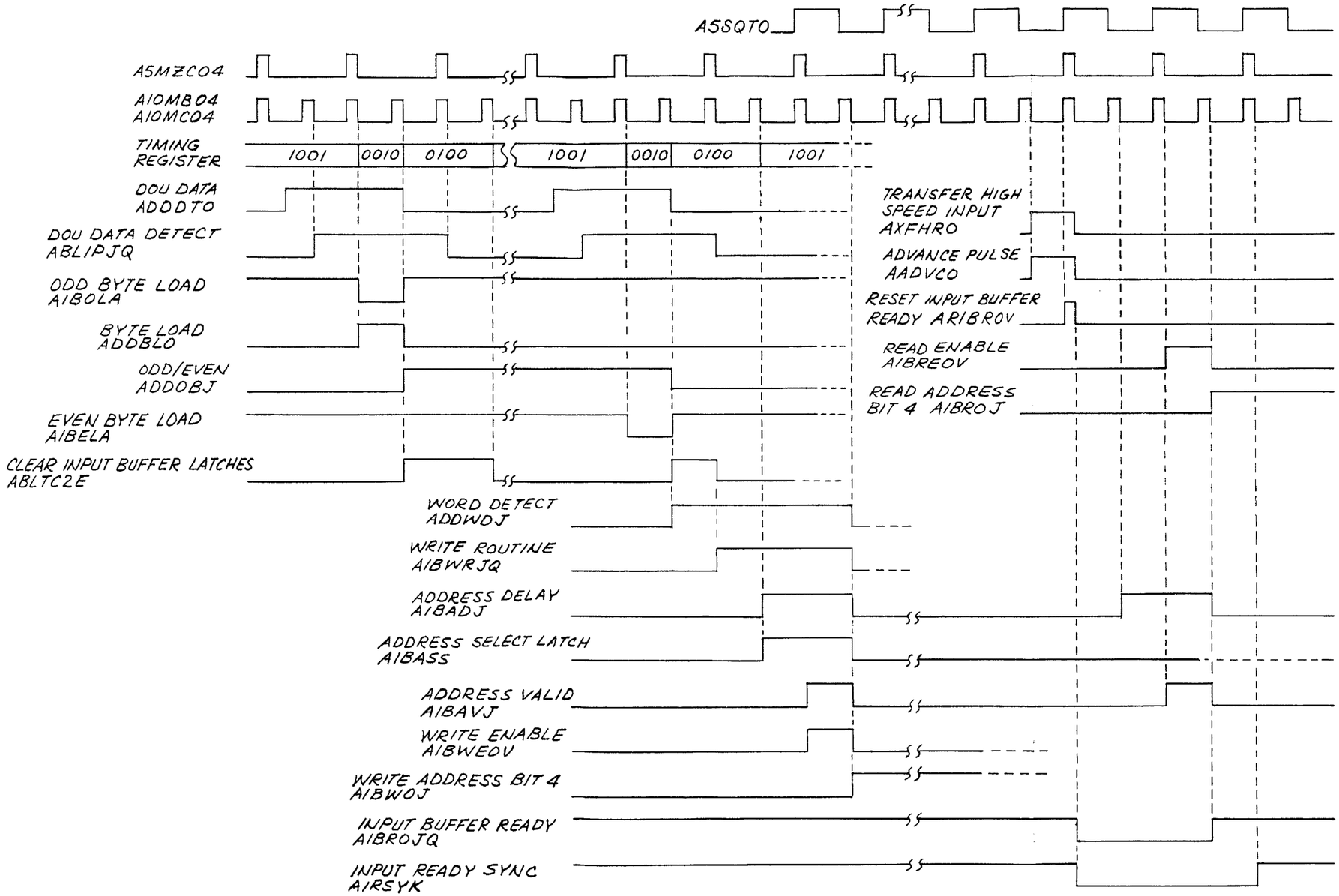

Figure 5-10. High Speed Input Buffer Control Logic Timing Diagram

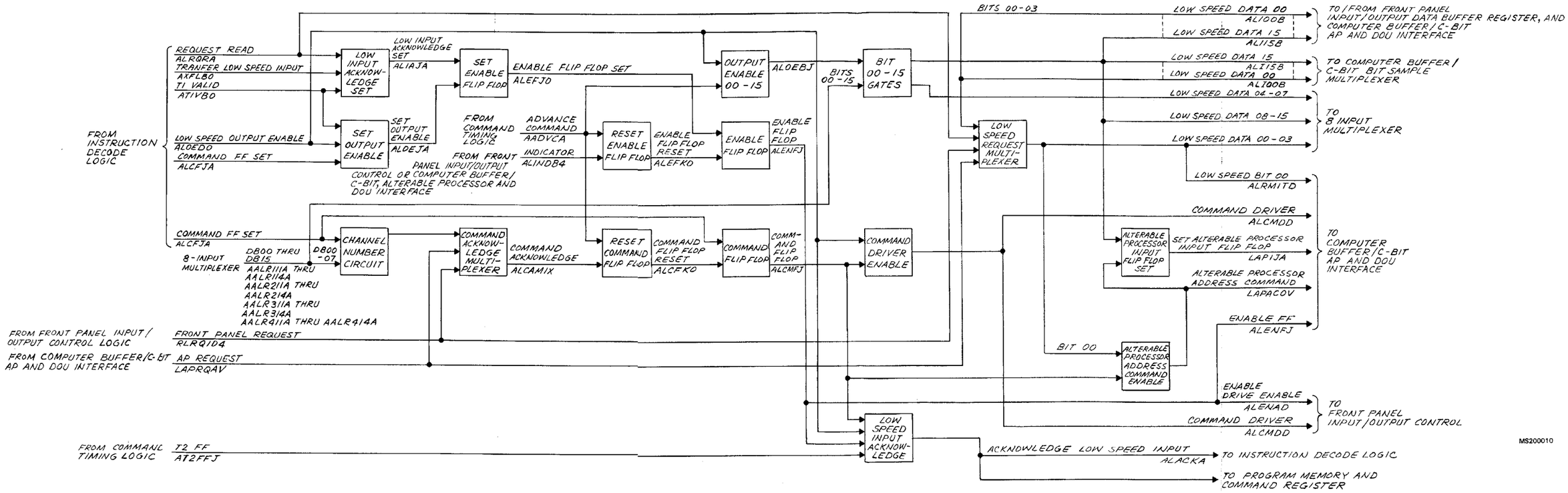

Figure 5-11. Low Speed Input/Output Block Diagram

Command acknowledge mux
Reset enable flip-flop
Reset command flip-flop
Output enable 00- 15
Enable flip-flop
Command flip-flop
Bit 00-15 gates
Command driver enable
Low speed input acknowledge
Low speed request mux
AP address command enable
AP input flip-flop set

The low speed I/O logic provides bidirectional communication for command and data information between the AP, computer buffer/C-BIT, and the front panel logic. Figure 5-12 illustrates the low speed I/O bus arrangement. The 16-bit word currently selected upon the data bus can be routed to the computer buffer/C-BIT or the front panel logic. The word from either the computer buffer/C-BIT or the front panel logic can be applied to the 8-input multiplexer. The source and destination for the current operation is dependent upon the current instruction and the associated utility field. The low speed I/O logic also generates control signals, which describe direction of transmission and the type of word being transferred and checks for the appropriate acknowledgment. For a data word, the enable output signal and the indicator response signal are utilized, and for a command word, the command output signal and the request response are utilized.

a. The occurrence of a CBL instruction and a ONE in bit CR05 (indicating a command and not an enable instruction) enables the command flip-flop set line which sets the command flip-flop and provides the load input to the channel number circuit. The active command signal notifies the computer buffer or the front panel logic that command control information is active. The input to the channel number circuit is a binary decode of the 8 LSBs of the data bus information. Bits 6 and 7 are utilized to determine whether the data is associated with the front panel logic (bit 6 a ONE) or the computer IOX (bit 7 a ONE). This code is utilized to direct the required request through the command acknowledge mux. The request response or the advance command signal resets the command flip-flop. The advance command is used as a reset signal since the front panel requires additional time to prepare the desired data for transmission. A second CBL instruction is programmed to provide for this delay.

b. The request read input to the low speed request mux goes low for a copy instruction (with CR06 true) indicating a request (as opposed to a low speed data) word. The front panel request or the AP request are then applied to low speed output bits 4 or 3 respectively while bits 1 and 2 are forced to ONE. For any other type of instruction, the request read line is high, and data bus information is selected for low speed data bits 0 thru 3.

c. When the word being transferred is a command, the active command FF signal and a ONE in data bit O develops the AP address command enable. When the current bit on the low speed line from the data bus is a ZERO, the computer buffer/C-BIT is informed that the current command is for AP input data. When low speed data bit 8 is a ONE, the set AP input FF signal is generated. Both of these signals are forwarded to the computer buffer/C-BIT as indications of the type of command (AP input or output) currently being processed.

d. The low speed enable function involves any instruction that requires the transfer of data (as opposed to command) information through the low speed I/O logic. When the proper operational code is detected, the enable flip-flop is set at time T1 valid. The low input acknowledge set is enabled for any STL command or for any copy command with CR06 a ZERO (indicating low speed data content). The set output enable goes active for a CBL instruction with CR05 a ZERO, indicating a data (as opposed to a command) word. Either of these conditions sets the enable flip-flop, resulting in an enable signal to the computer buffer/C-BIT and front panel logic. An active low speed output enable (CFL or CBL instruction) sets the output enable flip-flop, gating the information from the data bus to the low speed I/O bus. The enable flip-flop is reset by either the proper indicator response or by the advance signal.

e. The low speed acknowledge gate is tested at time T2 for each CFL or CBL instruction. As long as the proper acknowledgment has been received (enable and command flip-flops reset), an active signal is forwarded to the instruction decode logic and to the program memory and command register.

5-11. Arithmetic Logic Detailed Description (fig. 5-13, FO-6). The arithmetic logic consists of the following elements:

Arithmetic logic A thru D
OPR serial input gate
MSB MDY gate
MSB arith gate
MSB end-around gate
Right shift input decode
Look-ahead carry generator
Carry sample select
Stored count $\neq 0$
ALU $\neq$ all 1s
MSB carry decode
ALU C-BIT sample low
ALU C-BIT sample high
ALU control decode logic
ALU function encoder
OPR select gate
ALU carry mux
ALU function mux
OPR shift decode
Right shift decode

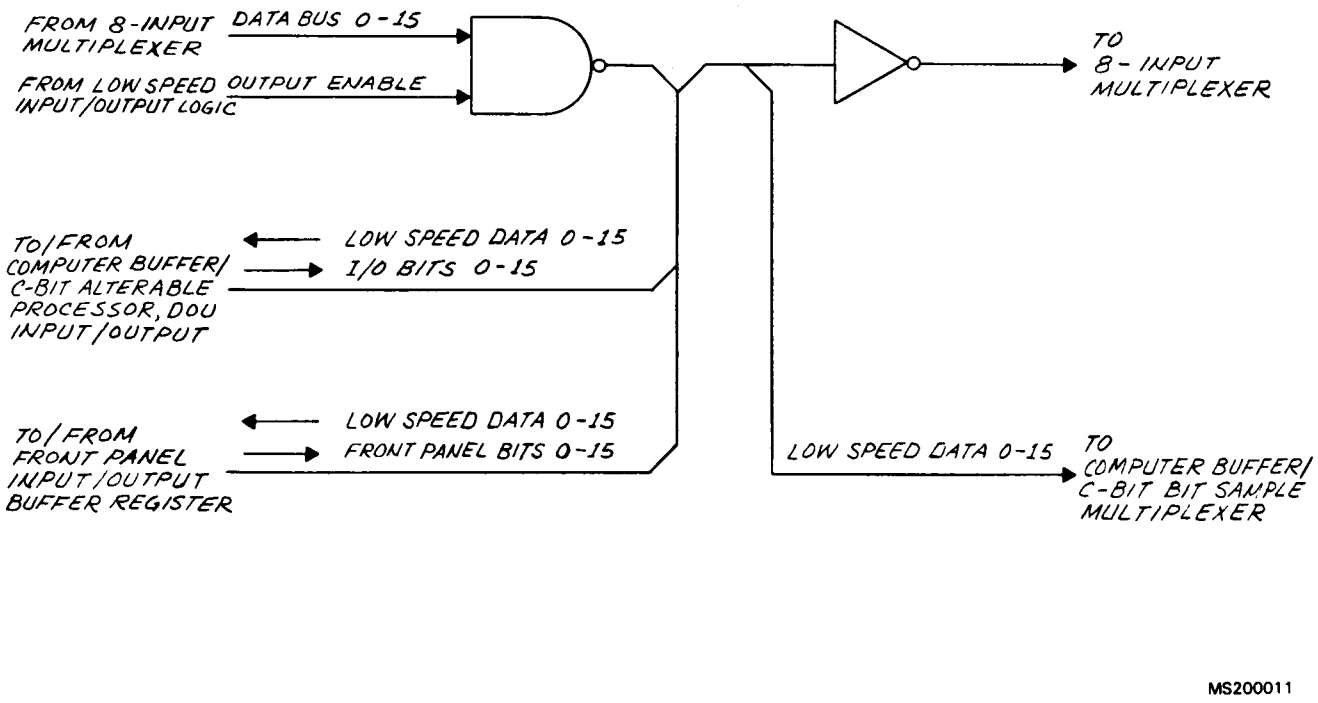

Figure 5-12. Low Speed Input/Output Logic Data Flow

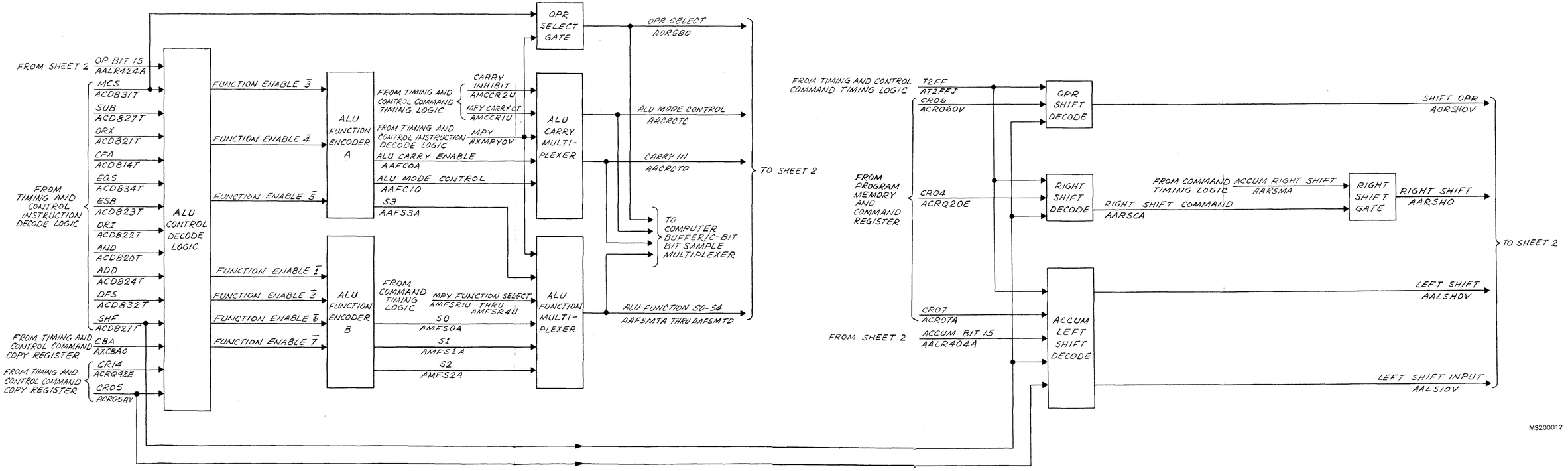

Figure 5-13. Arithmetic Logic Block Diagram (Sheet 1 of 2)

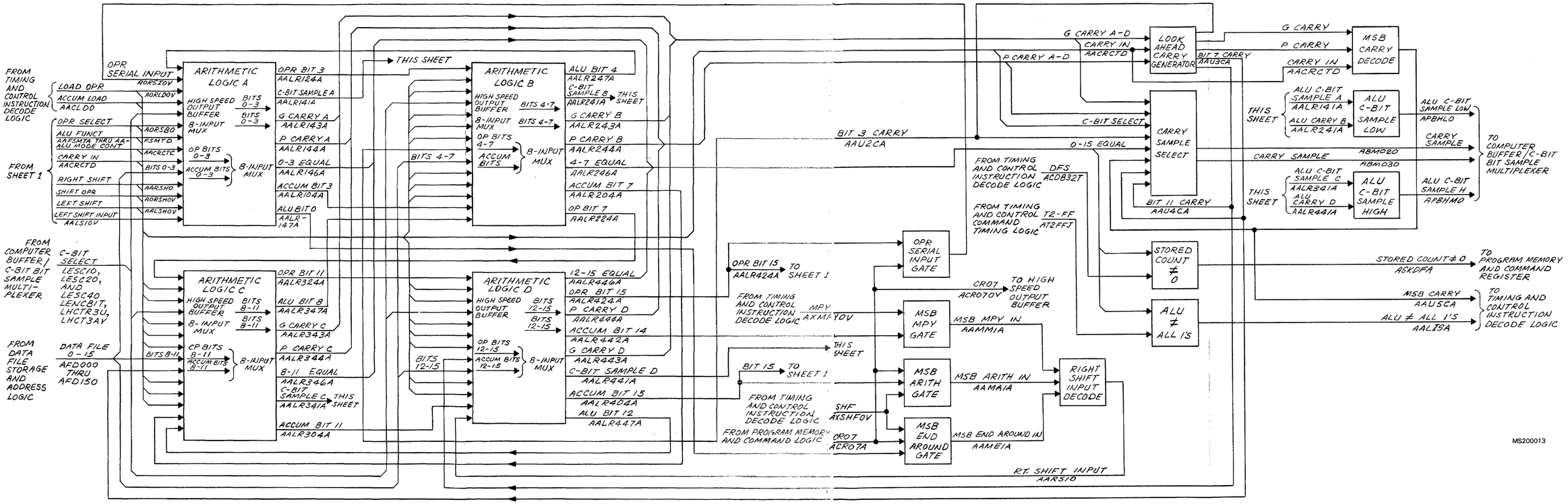

Figure 5-13. Arithmetic Logic Block Diagram (Sheet 2 of 2)

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ACCUM left shift decode
Right shift gate

a. *Arithmetic Logic.* The arithmetic logic performs all the Boolean, arithmetic, comparison, and shifting manipulation of AP data. The function decoding for all Boolean and arithmetic operations, with the exception of the MPY instruction, is also performed by this circuit. The operand register, arithmetic logic unit (ALU) input mux, ALU C-BIT sample mux, arithmetic logic unit, right shift mux, and accumulator (see fig. 5-14) is a detailed breakdown of arithmetic logic A thru D shown in figure 5-13 and processes 4 bits of the 16-bit word. The operand register and the accumulator provide the primary word-size, scratchpad memories for the AP. An active load OPR (CFO + CBO) stores 4 bits from the data bus into the operand register. An active shift OPR (SHF • CR06) permits the operand register to be left shifted. The serial input signal (OPR MSB • CR07) permits an end-around left shift. The current operand data is supplied to the 8-input mux and to the ALU input mux. The OPR select determines whether the operand data or data file information is gated to the ALU B input. The other (A) input to the ALU is the data currently selected on the data bus. The ALU performs a variety of Boolean and arithmetic operations as determined by the mode, carry, and function inputs. The ALU output is routed through the right shift mux to the accumulator. Thus, the ALU operates on information from the data bus and either operand or file data. Accumulator data can be placed on the data bus to be combined with either the operand or file data. In addition, data bus information can be routed directly through the ALU and stored in the accumulator. For SHF or MPY instructions, the 4 bits can be shifted one place to the right in the right shift mux. The left shift input (SHF • CRO5), going active, shifts the accumulator data left one place for each clock time that the signal remains active. The left shift input (CR07 • ACC MSB) permits an end-around shift of accumulator data. Individual output bits are provided to accommodate carry, shift, and equality comparison functions. The operand MSB is supplied to the next ALU stage in the event an operand shift function is required. The propagate carry and generate carry signals are applied to the look-ahead carry generator to provide synchronous carry generation for the next ALU stage. The ALU LSB is provided as an input to the next least significant ALU for end-around right shift operations. The accumulator MSB is supplied to the next significant ALU for left shift ALU operations.

b. *ALU Control Decode Logic.* The ALU control decode logic (see fig. 5-13) combines the pertinent instructions and required control bits to determine the ALU function. The inputs are decoded into seven function enable lines which are supplied to two ALU function encoders; table 5-10 lists the equations for each of the function enable lines. Each pertinent instruction will activate one function enable line to one or both of the function encoders. Table 5-11 lists the resultant function codes and the attendant ALU functions. Table 5-12 provides a complete listing of the ALU functions for the various permutations of ALU selection, mode, and carry indications. The mode (M) input, when high, inhibits the internal bit-to-bit carry. Each of the four circuits are then independent functional entities and Boolean operations are performed. In this logical mode, the carry input is irrelevant and is ignored. When the mode input goes low, an arithmetic operation is performed. The carry input, when low, can then be propagated through the four circuits of the ALU. The carry input and two carry outputs are combined in the look-ahead carry generator to provide the carry input for the next four-stage ALU. The data file information is distributed in groups of 4 bits. Inputs from the high speed output buffer and to/from the 8-input mux are shown internal to the circuits and are part of the arithmetic logic. The bussed inputs (ie, OPR load and select, accumulator load, ALU function, mode and carry enables, and the various shift enables) are applied in parallel to all four arithmetic logic circuits. Operand register and accumulator information are daisy-chained through the four arithmetic logic circuits. Carry and equality signals are shown bussed to the appropriate output gating. The LSB for each ALU stage is routed to the next least significant stage to accommodate right shift operations. Logic is provided to gate the outputs of the most significant ALU stage. When the CRO7 bit is low, OPR bit 15 is gated to the first ALU stage operand register. The MSB MPY gate is enabled by ACC BIT 14 • MPY; the MSB ARITH gate is enabled by CRO7 . ACC BIT 15 • SHF; the MSB end-around gate is enabled by CRO7 • SHF • ALU BIT 0. Any one of these conditions supplies a ONE to the LSB of the most significant ALU stage, providing the required MSB for a right shift operation.

c. *Look-Ahead Carry Generator.* The look-ahead carry generator provides synchronous carry generation for the four ALU stages (during a subtraction operation, the borrow bit is generated). The carry bit is generated by comparing the carry-in bit and the propagate (P carry) and generate (G carry) bits from ail four stages and developing carry overflow indications in accordance with table 5-13. The carry bits for the second, third, and fourth stages are provided on the carry bit 3, 7, and 11 lines, respectively. The MSB carry bit is utilized in the instruction decode logic during an MCS instruction to indicate absolute magnitude comparison.

d. *DFS, ESB, and EQS Instructions.* The bit 0-15 equal outputs from the four ALU circuits are used for the DFS, ESB, and EQS instructions. The DFS instruction is utilized to clear a file memory location. This is accomplished by decrementing the file information by one until the remainder is all ZEROs, as indicated by a low signal on the stored count $\neq 0$ output line. The ALU $\neq$ all 1s output is utilized in the instruction decode logic to check for bit or word equality during an ESB or EQS instruction.

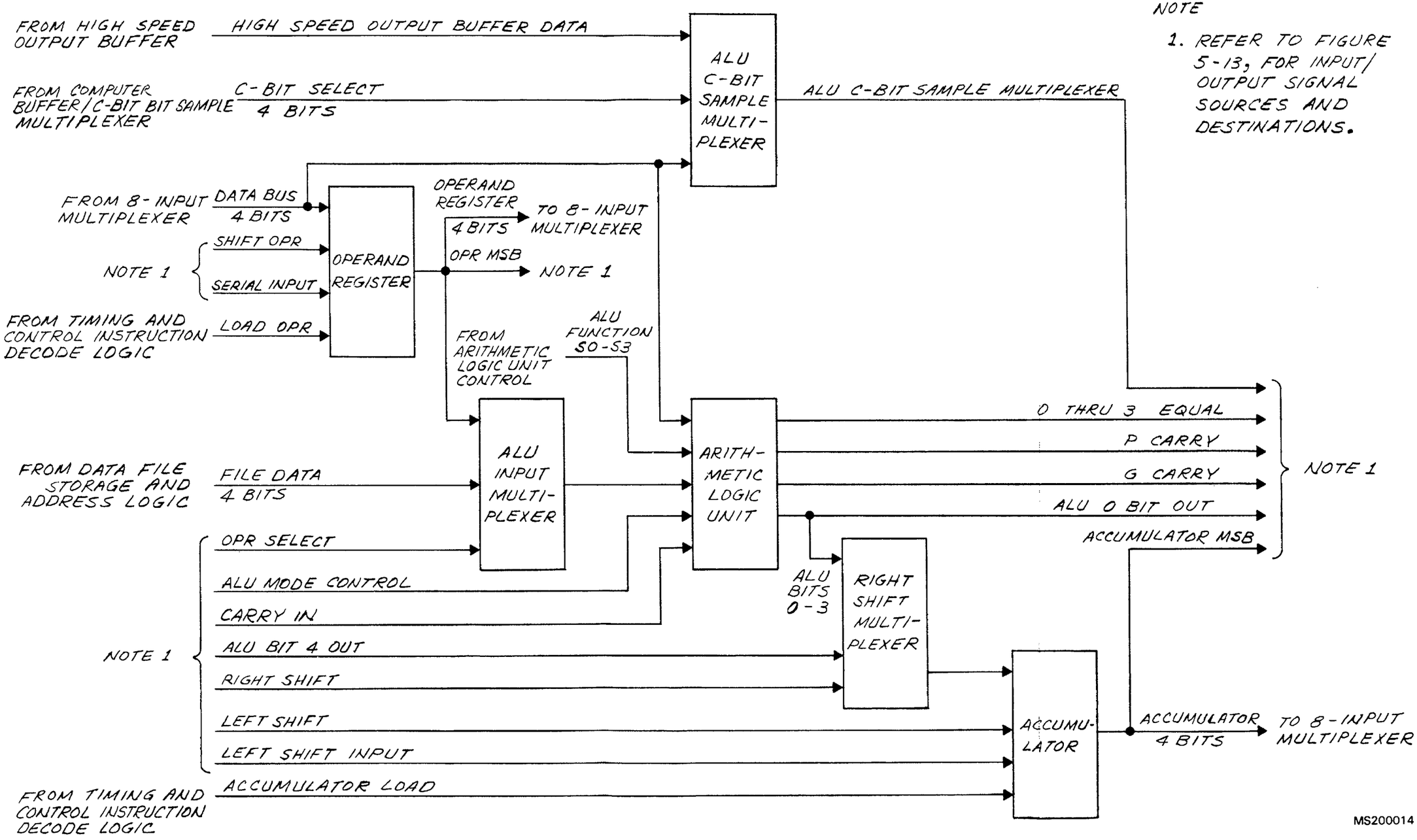
Table 5-10. ALU Control Decoding Scheme

Priority encoder	Input	Equation
A	$\overline{3}$	SUB + (MCS • $\overline{\text{OR15}}$)
	4	[SHF + CFA + EQS + ESB + ORI + AND + (CBA • $\overline{\text{CR05}}$)] • [($\overline{\text{CBA}}$ • $\overline{\text{CR05}}$) +CBA]
	5	[ADD + DFS + (MCS • OR15)] • CR14
B	1	[ADD + ESQ + (MCS • OR15)] • CR14
	3	AND
	6	ORX + ORI + SUB + ($\overline{\text{OR15}}$)] • MCS)
	7	[DFS + CFA + SHF + ($\overline{\text{CBA}}$ • $\overline{\text{CR05}}$)] • [$\overline{\text{CBA}}$ + ($\overline{\text{CBA}}$ • $\overline{\text{CR05}}$)]

Table 5-11. ALU Function Codes (Except MPY)

Instruction		Priority Encoder		ALU code						
Oct	Mnemonic	U1	U7	S3	S2	S1	S0	C0	M	ALU Function
04	CBA*	$\overline{4}$	$\overline{7}$	H	H	H	H	H	H	A
14	CFA	$\overline{4}$	$\overline{7}$	H	H	H	H	H	H	A
20	AND	$\overline{4}$	$\overline{3}$	H	L	H	H	H	H	A • B
21	ORX	--	$\overline{6}$	L	H	H	L	H	H	A ⊕ B
22	ORI	$\overline{4}$	$\overline{6}$	H	H	H	L	H	H	A + B
23	ESB	$\overline{4}$	--	H	L	L	L	H	H	$\overline{\text{A + B}}$
24	ADD	5	1	H	L	L	H	H	L	A PLUS B
25	SUB	$\overline{3}$	$\overline{6}$	L	H	H	L	L	L	A MINUS B
27	SHF	$\overline{4}$	$\overline{7}$	H	H	H	H	H	H	A
31	MCS (OR15)	$\overline{5}$	$\overline{1}$	H	L	L	H	H	L	A PLUS B
31	$\overline{\text{MCS}}$ ($\overline{\text{OR15}}$)	$\overline{3}$	$\overline{6}$	L	H	H	L	L	L	A MINUS B
32	DFS	$\overline{5}$	$\overline{7}$	H	H	H	H	H	L	A MINUS 1
34	EQS	$\overline{4}$	$\overline{1}$	H	L	L	H	H	H	$\overline{\text{A + B}}$
	NONE	--	--	L	L	L	L	H	H	A

*For CR05=ZERO



NOTE

1. REFER TO FIGURE 5-13, FOR INPUT/OUTPUT SIGNAL SOURCES AND DESTINATIONS.

Figure 5-14. Arithmetic Logic A thru D Detailed Block Diagram

Table 5-12. ALU Logic and Arithmetic Operations

Selection				Active-high data M = H logic	Active-high data M = L: Arithmetic operations	
S3	S2	S1	S0	Functions	C_n = H (No carry)	C_n = L (With carry)
L	L	L	L	$F = \overline{A}$	F = A	F = A PLUS 1
L	L	L	H	$F = \overline{A + B}$	$F = A + \overline{B}$	F = (A + B) PLUS 1
L	L	H	L	$F = A\overline{B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2s COMPL)	F = ZERO
L	H	L	L	$F = \overline{AB}$	F = A PLUS $\overline{AB}$	F = A PLUS AB PLUS 1
L	H	L	H	$F = \overline{B}$	F = (A + B) PLUS AB	F = (A-B) PLUS $A\overline{B}$ PLUS 1
L	H	H	L	$F = A \oplus B$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	$F = A\overline{B}$	F = AB MINUS 1	$F = A\overline{B}$
H	L	L	L	$F = \overline{A + B}$	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	$F = \overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = $(\overline{A + B})$ PLUS AB	F = $(\overline{A + B})$ PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	$F = \overline{A + B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A + B) PLUS A	F = $(\overline{A + B})$ PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

5-12. Data File Storage and Address Detailed Description (fig. 5-15, FO-7). The data file storage and address logic consists of the following elements:

Index counter/register
Index function enable
File address adder
Constant file 128-255 enable
RAM select decoder
Constant file address decoder
C-BIT sample mux
Scratchpad
Constant file 16 x 256
File data gating

The data file addressing scheme is controlled by the states of the BST instruction, the CR09 (indexing) bit, and the CR07 bit. The BST instruction requires that the current program address be stored in scratchpad file location 0. Therefore, this instruction forces an all ZERO scratchpad file address. For other than a BST instruction, the addressing scheme is dependent upon the state of the CR09 indexing bit. When this bit is a ZERO, the 8 LSBs of the command register are used directly to address the data file. When this bit is a ONE, the content of the index counter/register is added to the command register address to produce the file address. The CR07 bit determines which portion of the file is addressed: a CR07 ONE addresses the constant PROM portion while a CR07 ZERO addresses the scratchpad RAM portion.

a. *Index Counter/Register.* The index counter/ register is an eight-stage binary down counter that is mechanized to sequentially decrement for a DIS instruc- tion. For a copy into index instruction (CBI or CFI), the index counter load signal stores the 8 LSBs from the data bus in the index counter/register.

b. *File Address Adder.* Data file addressing is mechanized by the eight-stage index counter and two 4-bit arithmetic logic units which comprise the file address adder. The required addressing scheme is determined by the function code to the file address adder,

Table 5-13. Look-Ahead Carry Generator Truth Table

Inputs									Outputs				
$\overline{C_n}$	G0	P0	G1	P1	G2	P2	G3	P3	$\overline{C0}$	$\overline{C1}$	$\overline{C2}$	G	P
X	H	H							L				
L	H	X							L				
X	H	X							H				
H	H	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	H	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	H	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

X = Irrelevant

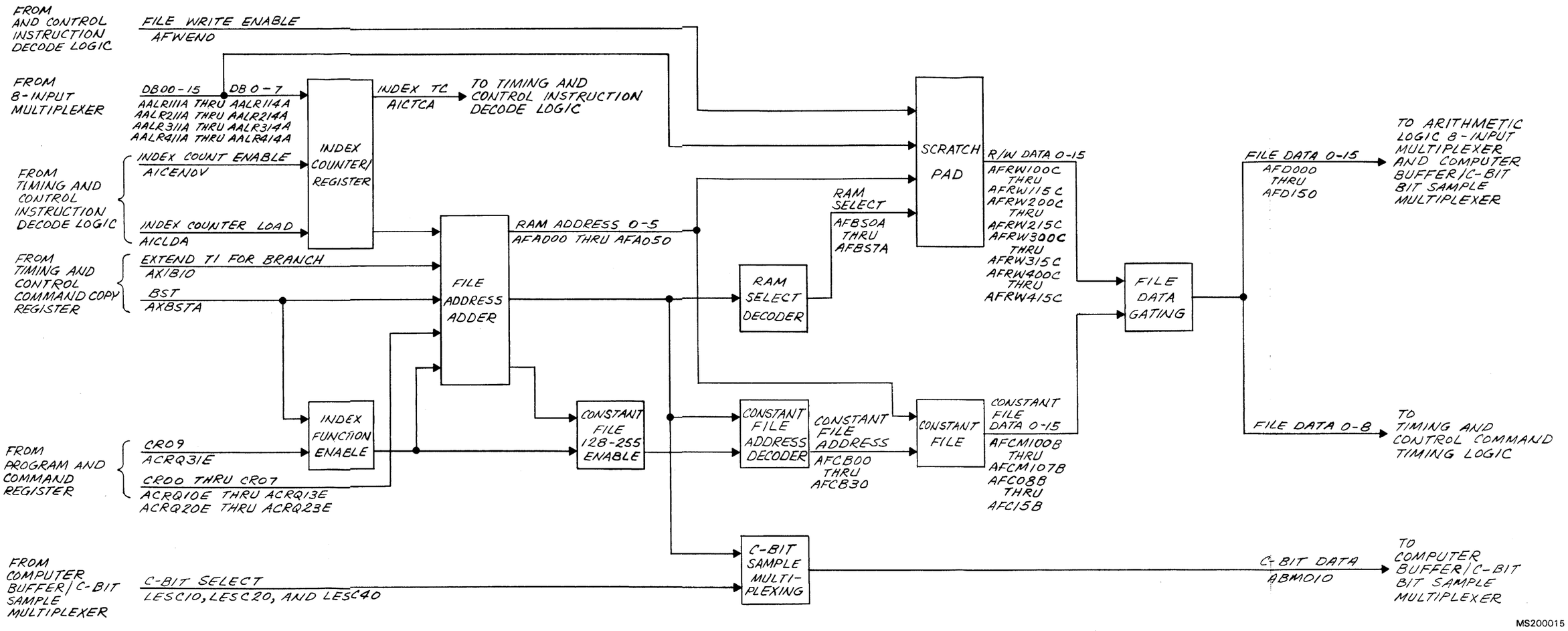


Figure 5-15. Data File Storage and Address Block Diagram

which is in turn determined by the states of the BST and CRO9 inputs, as follows:

ALU function input	*Logic state*
SO	Hold high
S and $\overline{M}$	High for $\underline{BST} + \overline{CR09}$
	Low for $\overline{BST} \cdot CR09$
S2	High for $\overline{BST} \cdot \overline{CR09}$
	Low for BST + CR09
S3	High for $\overline{BST}$
	Low for BST

Therefore, the decoder function inputs to the file address adder are:

	ALU function inputs					
Equation	S3	S2	SI	S0	M	ALU function
BST . CR09	0	0	1	1	1	Logic 0
$BST \cdot \overline{CR09}$	0	0	1	1	1	Logic 0
$\overline{BST} \cdot CR09$	1	0	0	1	0	A plus B
$\overline{BST} \cdot \overline{CR09}$	1	1	1	1	1	A

The above equations demonstrate that the BST instruction forces an all ZERO address. The BST combined with an active indexing bit results in addition of the index counter/register and command register 8 LSBs, while the BST • CR09 simply applies the command register bits to the data file address lines.

c. *Constant File.* The constant file is a 256-word x 16-bit PROM, comprising eight 512-bit memory locations. For each address, two PROMs are selected to each output one of sixty-four 8-bit bytes, constituting the 1 6-bit stored data word. A ONE in the CR07 bit enables the constant file address decoder. The carry bit from the file address adder is combined with the index function enable to determine whether the upper half (0-127) or the lower half (128-255) of the constant file is being addressed. Thus, the upper half of the constant file can only be accessed when the index option is selected (BST CR09). The four-line output from the constant file address decoder thus selects two of the eight PROMs. The 6 LSBs from the file address adder select 1 of the 64 constant file words.

d. *Scratchpad File.* When the CRO7 is a ZERO, constant file addressing is disabled and scratchpad file addressing is enabled. The scratchpad file is mounted upon four PCBs, each containing eight 64-bit bipolar RAM chips. The 4 MSBs from the file address adder are combined in the RAM select decoder to select four of eight chips on one of the four PCBs. The 4 LSBs select one of the four 16-bit word locations. Writing into the scratchpad file is enabled by the file write enable from the instruction decode logic. At all other times, the selected word from the file is supplied to the file data gating. The file data gating routes the selected data file word to the 8-input mux, the arithmetic logic, and the computer buffer/C-BIT BIT sample mux.

5-13. 8-input Multiplexer Detailed Description (fig. 5-16, FO-8). The 8-input mux is used to route data information from one of eight sources to the data bus. The data bus supplies the selected information word in parallel to eight destination registers. The source and destination is determined by decoding the current command word. Sixteen 8-input muxs provide the switching function to the data bus. A 3-bit binary code from the data bus select logic determines which one of the eight inputs for each mux is selected. The significance of the eight sets of input data is described in table 5-14. Figure 5-17 illustrates the AP data transmission paths, the inputs and outputs to and from the 8-input mux, and the 3-bit bus select code. The 3-bit bus select code is defined in paragraph 5-16. The bus distributes the selected information to the arithmetic logic unit, operand register, index register, data file, program address counter, high speed output register, and low speed output bus. The data to the arithmetic logic unit and high speed output register is active high, while all other destinations receive active low data.

5-14. Program Memory and Command Register Detailed Description (fig. 5-18, FO-9). The program memory and command register consists of the following elements:

Count gate
Load gate
Program address counter
Program address decoder
Display memory
Program command mux
Command input mux
Command register
AP test breakpoint
Transfer high decode
Copy file gate
Transfer low decode

The program memory aid command register provides the addressing, permanent storage, and temporary output storage for the command words. The command word storage is provided by a 1024 word x 16 bit PROM containing a repertoire of 32 preselected instructions. The particular instruction is determined by decoding bits 10 thru 14 of the command word as illustrated in table 5-15.

a. *Program Address Counter.* A 10-bit program address counter is utilized to select one of the 1024 instructions stored in the display memory. When the display console is initialized, the counter is cleared to all ZEROs. The counter can then be incremented by each advance command to sequentially address each of the 1024 storage locations. Branch instructions (CFB, CCB,

and BST) require that the program counter be branched to a new starting address. The presence of any one of these instructions generates the load signal at T1 invalid time. The program address counter is then loaded with the 10 LSBs currently on the data bus. The program address counter is also incremented by any one of several skip routines or by external signals (stored count ¹ 0 and acknowledge low speed input). These instructions permit the program address counter to be incremented during an instruction cycle as well as at the end. The program memory comprises four bipolar read/write memory PCBs, each capable of storing 512 8-bit bytes. Each board contains eight 512-bit bipolar PROM chips. The 5 LSBs of the program address counter are utilized to binarily select one of the sixty-four 8-bit bytes stored.

b. *Program Address Decoder.* Program address bits 6 thru 8 are decoded to provide a unary module 64 signal which selects one of the eight PROM chips. Program address bit 9 selects two of the four addressed chips to provide the 1 6-bit command word at the output of the program command mux. The command input mux selects between the stored command word or a test word from the computer buffer/C-BIT logic. The output from the command input mux is loaded into the command register by the advance command signal. The command information from the program command mux, the command input mux, and the command register is distributed to various AP and computer buffer/C-BIT logic for decoding and control signal applications.

c. *Program and Command Register Logic.* Some initial decoding (transfer high speed required, transfer low speed required, and copy file) is performed by the program memory and command register logic. The equation ([CR10 • CR11] + CR12) • CR13 • CR14 defines the copy bus instructions 03 thru 07 (refer to table 5-15). When source code bits CR07 thru CR09 are I 10 (indicating the high speed output buffer), the transfer high speed required signal is generated. The source code bits are defined in paragraph 5-16. When CR07 thru CR09 are 010 (indicating the low speed output buffer), the transfer low speed required signal is generated. The equation CR12 • CR13 • CR14 defines copy file instructions 14 thru 17. Thus a CFA, CFO, CFL, or CFH instruction develops the copy file signal.

5-15. High-Speed Output Buffer Detailed Description (fig. 5-19, FO-10). The high-speed output buffer consists of the following elements:

Load gate
Control word detect
Set control word flip-flop
DC control word flip-flop
High speed output ready
Output buffer
Extend T1 necessary

The high speed output buffer provides the temporary storage for the high speed data being transmitted to the DB and generates the required indication for the initial word of each message. High speed date outputting is initiated by the transger to the high speed output buffer signal which goes active for a CBH or CFH instruction and generates the load signal at T1 valid time. The signal loads the information currently on the data bus into the output buffer and sets the high speed output ready flip-flop. The active high speed ready signal informs the DB that an output word is available and also generates the extend T1 necessary signal to the instruction decode logic. This prolongs the TI phase until the DB acknowledges acceptance of the output word. The DB acknowledge resets the high speed output ready flip-flop terminating the ready and extend T1 necessary signals. Logic is provided to identify the initial control word of each message transmitted to the DB. The signals utilized are dependent upon the current instruction repertoire. An active input to the control word detect indicates that the initial control word of a message is available in the high speed input buffer, and the current command reflects a copy instruction with a high speed input buffer source code. The load signal then sets the DC control word flip-flop, forcing a ONE in the most significant digit of the DC word. The DC control word flip-flop is reset by the DB acknowledge signal.

5-16. Timing and Control Detailed Description (fig.5-20). The timing and control consists of the following elements:

Command copy register
Command timing logic
Sense switch logic
Instruction decode logic
Data bus select logic

The timing and control decodes the current command word to provide the various timing and control signals required by the AP to process the current instruction. Command word decoding is controlled by the advance command which indicates the termination of a current instruction cycle and the beginning of a new instruction cycle. The advance command signal instructs the program memory and command register to load the next instruction. The op code and the utility field for this next instruction are supplied to timing and control. The advance command also loads the 5-bit op code into the command copy register. The command copy register provides supplementary storage for the op code in addition to supplementary instruction decoding (BST, CCB and CBA). The instruction decode logic is used for primary command word decoding and provides indications of the current instruction. Table 5-16 defines the command word utility field by instruction and op code. The instruction decode logic combines the indications with pertinent utility field bits and generates the control levels required to ensure that the proper data is processed in the proper sequence. The instruction decode logic also provides the majority of control signals required by the AP to transfer and manipulate data. The instruction

Table 5-14. 8- Input Multiplexer input Data Description.

Input	Bits	Signal name	Mnemonic	Source
I0	0-15	ACCUM 0-15	AALRΔΔΔA	Arithmetic logic
I1	0-15	OPAND 0-15	AALRΔΔΔA	Arithmetic logic
I2	0-15	LA DATA 0-15	ALBΔΔOV	Low speed I/O
I3	0-15	HS DATA 0-15	AIBOΔΔV	High speed read/write register
I14	0-15	FILE DATA 0-15	AFDΔΔO	Data file storage and address logic
I15	0-9	CMD REG 0-9,	ACRΔΔΔΔ	Program memory and command register
	12-15	CMD REG 12-15		Command copy register
			ACC11JQ	
	10,11	CMD REG 10,11		
I6	0-9	PACO-PAC9	APACΔΔU	Program memory and command register
	0-10	No connection		
I7	0-2	Address select 0-2	ACADΔO4	Computer buffer C-BIT I/O Register
	3	DOU inhibit	LRQOV01	Computer buffer/C-BIT, AP and DOU interface
	4	DOU request inhibit	LDRQ1AV	
	5	Ground		
	6	Sense switch 6	KSWO6D4	Display controller timing and control sense switch logic
	7	Sense switch logic 7	KSWO7D4	
	8	Sense switch 8	KSWO8D4	
	9	DOU overrun	LDORNOV	Computer buffer/C-BIT AP and DOU interface
	10	CPU Mem Par Err Word	LMPECOV	
	11	CPU Mem Par Err T.O.	LMPEDOV	
	12	DOU memory time out	LMPTOAOV	
	13	Radar only display enable	LRODEJ	
	14,15	Ground		

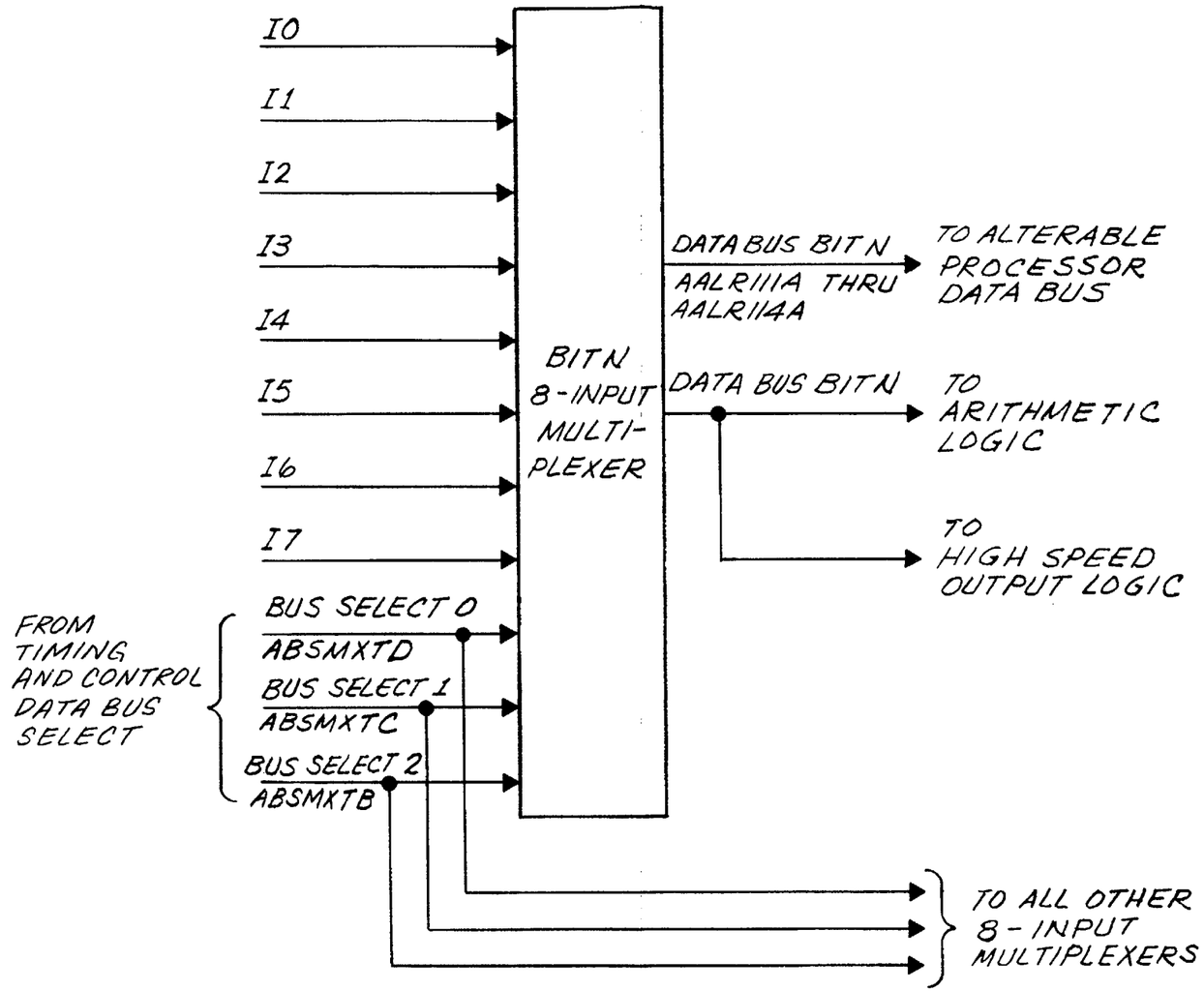
Note: Δ indicates multi-line mnemonic (0-15, A thru D, etc)

Table 5-15. Instruction Decoding

	Command word bits							
Octal	15	14	13	12	11	10	Mnemonic	Instruction
00		0	0	0	0	0	SSW	Set sense switch
01		0	0	0	0	1	RSW	Reset sense switch
02		0	0	0	1	0	TSS	Test sense switch
03		0	0	0	1	1	CBI	Copy bus into index
04		0	0	1	0	0	CBA	Copy bus into accumulator
05		0	0	1	0	1	CBO	Copy bus into operand
06		0	0	1	1	0	CBL	Copy bus into low speed
07		0	0	1	1	1	CBH	Copy bus into high speed
10		0	1	0	0	0	STA	Store accumulator
11		0	1	0	0	1	STO	Store operand

Table 5-15. Instruction Decoding-Continued

Octal	Command word bits 15	14	13	12	11	10	Mnemonic	Instruction
12		0	1	0	1	0	STL	Store low speed
13		0	1	0	1	1	STH	Store high speed
14		0	1	1	0	0	CFA	Copy file to accumulator
15		0	1	1	0	1	CFO	Copy file to operand
16		0	1	1	1	0	CFL	Copy file to low speed
17		0	1	1	1	1	CFH	Copy file to high speed
20		1	0	0	0	0	AND	And
21		1	0	0	0	1	ORX	Exclusive OR
22		1	0	0	1	0	ORI	Inclusive OR
23		1	0	0	1	1	ESB	Examine selected bits
24		1	0	1	0	0	ADD	Add
25		1	0	1	0	1	SUB	Subtract
26		1	0	1	1	0	MPY	Multiply
27		1	0	1	1	1	SHF	Shift
30		1	1	0	0	0	CFB	Copy file and branch
31		1	1	0	0	1	MCS	Magnitude compare-skip
32		1	1	0	1	0	DFS	Decrement file-skip
33		1	1	0	1	1	CFI	Copy file into index
34		1	1	1	0	0	EQS	Equality-skip
35		1	1	1	0	1	DIS	Decrement index and skip
36		1	1	1	1	0	CCB	Copy command register and branch
37		1	1	1	1	1	BST	Branch and store



NOTE: INPUTS I0 THRU I7 ARE DESCRIBED IN TABLE 5-14.

MS200016

Figure 5-16. 8-Input Multiplexer

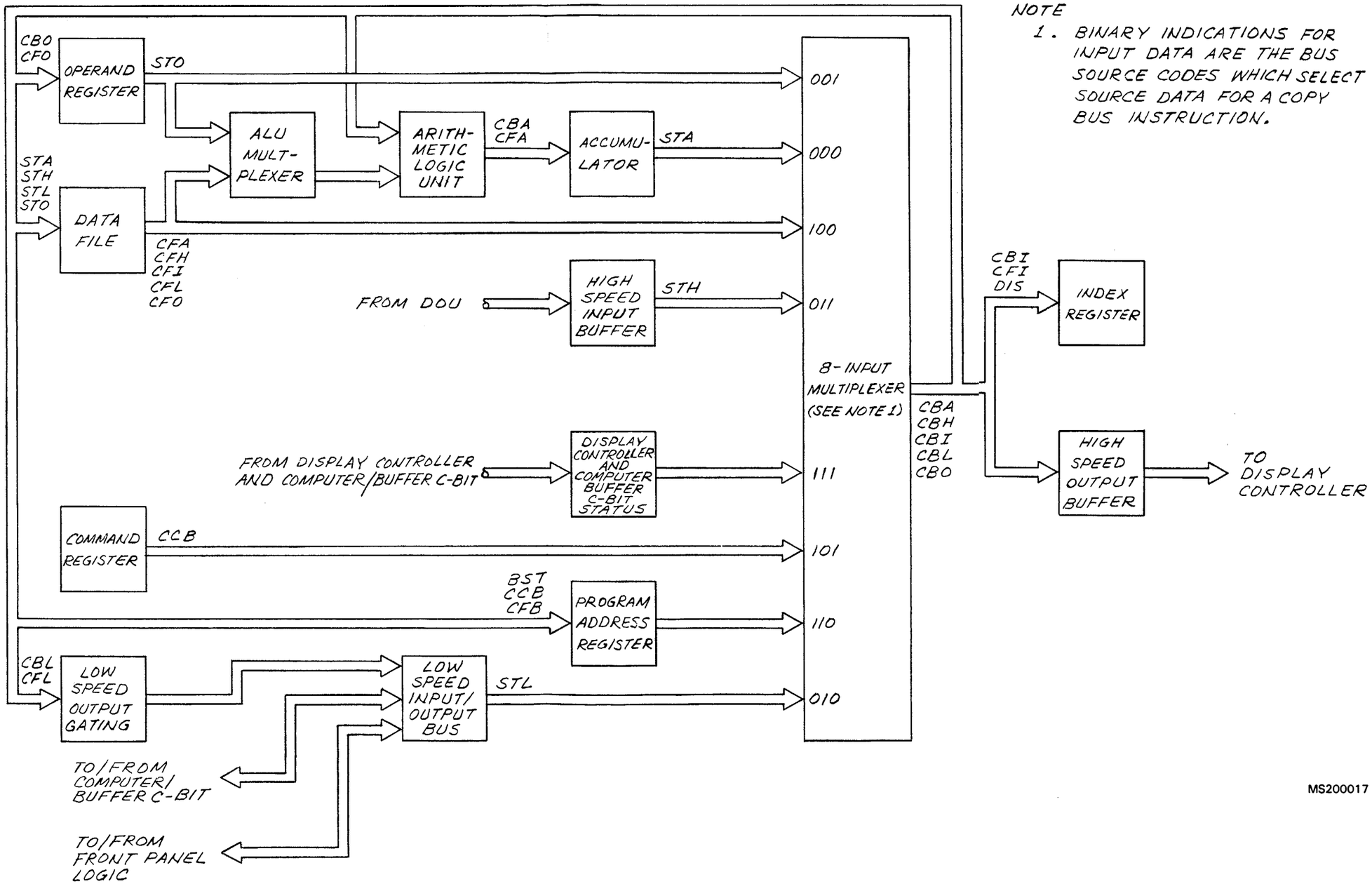


Figure 5-17. Alterable Processor Data Transmission

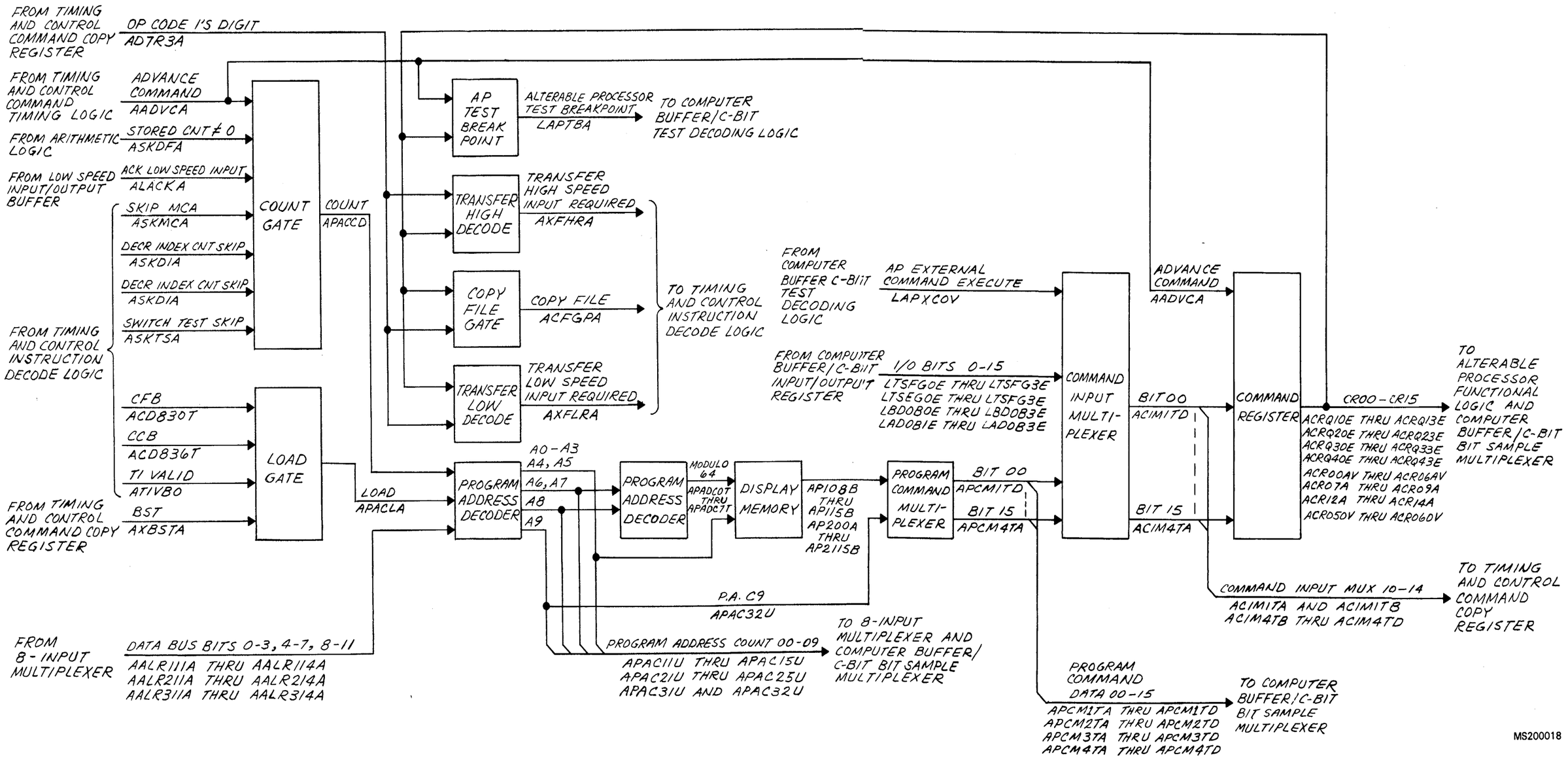


Figure 5-18. Program Memory and Command Register Block Diagram

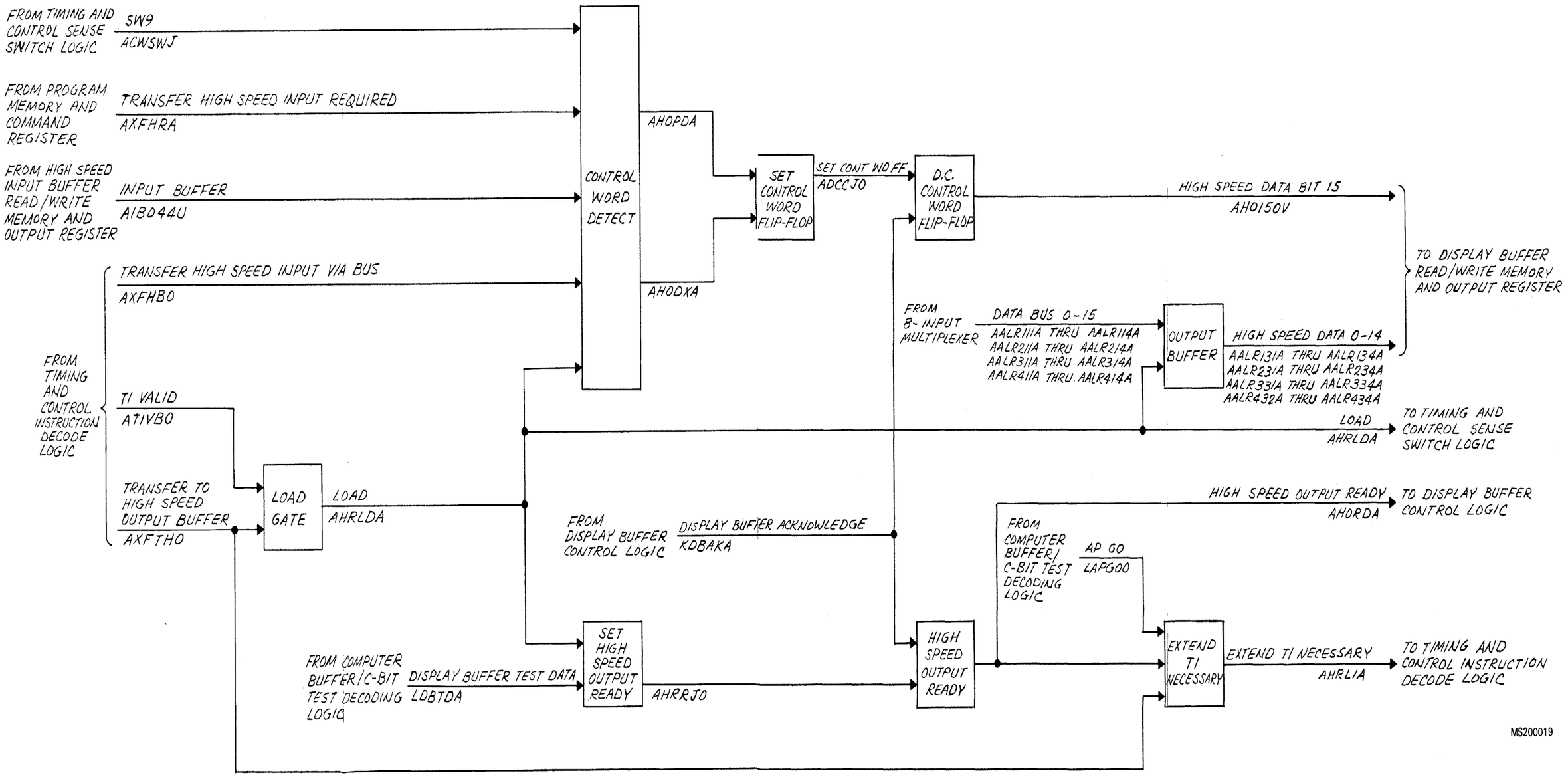


Figure 5-19. High Speed Output Buffer Block Diagram

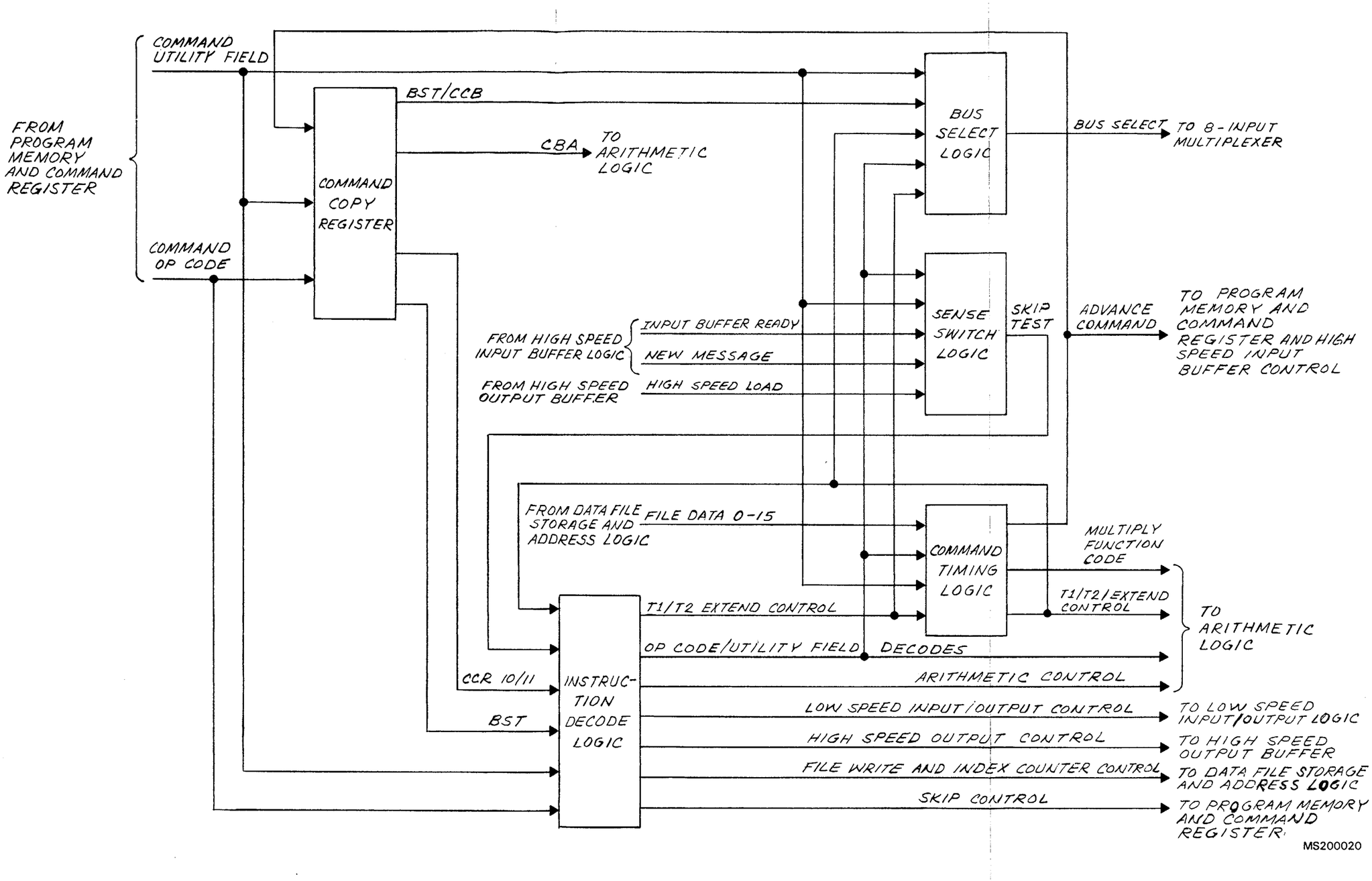


Figure 5-20. Timing and Control Block Diagram

Table 5-16. Command Set Description

OP code	INST	Command word utility										Command Description
		Index Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
00	SSW	(SW9)	SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW1	SW0	Set sense switches 0 thru 9. If bit is "1", corresponding switch is set.
01	RSW	(SW9)	SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW1	SW0	Reset sense switches 0 thru 9. If bit is "1", corresponding switch is reset.
02	TSS	(SW0)	SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW2	SW0	Test sense switch. Skip next instruction if any selected sense switch is not set.
03	CBI	SOURCE REG MSB	SOURCE REG 2 LSB	SOURCE REG LSB	Bus Code = 010 1 = Req. 0 = Ldata							Load 8 LSB contents of bus into index register. Bits 7 thru 9 specify source register to bus.
04	CBA	SOURCE	SOURCE	SOURCE	Bus Code = 010 1 = Req. 0 = Ldata	INVERT N OPTION						Load contents of bus into accumulator. Bits 7 thru 9 specify source register.
05	CBO	SOURCE	SOURCE	SOURCE	Bus Code = 010 1 = Req. 0 = Ldata							Load contents of bus into operand register. Bits 7 thru 9 specify source register.
06	CBL	SOURCE	SOURCE	SOURCE	Not Used	1 = Comm 0 = Enable						Copy bus to low speed data interface. Bits 7 thru 9 specify source register.

Table 5-16. Command Set Description - Continued

OP code	INST	Command word utility: Index Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Command Description
07	CBH	SOURCE REG MSB	SOURCE REG 2 LSB	SOURCE REG LSB	Bus Code = 010 1 = Req. 0 = Ldata							Copy bus to high speed interface output bits 7 thru 9. Specify source register.
10	STA	INDES	Not used	MSB ← FILE ADDRESS → LSB								Contents of accumulator are copied into file. File address may be modified by contents of index register.
11	STO	INDEX	Not used	MSB ← FILE ADDRESS → LSB								Content of operand is copied into file. File address may be modified by contents of index register.
12	STL	INDEX	Not used	MSB ← FILE ADDRESS → LSB								Content of low speed interface is copied into file. File address may be modified by contents of index register.
13	STH	INDEX	Not used	MSB ← FILE ADDRESS → LSB								Contents of high speed input register are copied into file. File address may be modified by contents of index register.
14	CFA	INDEX	Not used	MSB ← FILE ADDRESS → LSB								Contents of file are copied into accumulator.
15	CFO	INDEX	Not used	MSB ← FILE ADDRESS → LSB								Contents of file are copied into operand register.
16	CFL	INDEX	Not used	MSB ← FILE ADDRESS → LSB								Contents of file are copied onto low speed data lines.
17	CFH	INDEX	Not used	MSB ← FILE ADDRESS → LSB								Contents of file are copied into high speed output buffer.
18	AND	INDEX	1 = Oprnd 0 = ACC	MSB ← FILE ADDRESS → LSB								File is logically ANDed with contents of accumulator. or operand register and result is stored in accumulator.

Table 5-16. Command Set Description - Continued

OP code	INST	Command word utility: Index Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Command Description
21	ORX	INDEX	1 = Oprnd 0 = ACC	MSB			FILE ADDRESS				LSB	File is exclusive Ored with contents of accumulator or operand register and result is stored in accumulator.
22	ORI	INDEX	1 = Oprnd 0 = ACC	MSB			FILE ADDRESS				LSB	File is inclusive Ored with contents of accumulator or operand register and result is stored in accumulator.
23	ESB	INDEX	1 = Oprnd 0 = ACC	MSB			FILE ADDRESS				LSB	Contents of file are compared to ACC or operand register. Skip if bit in file is 0 corresponding to a "1" bit in ACC or operand.
24	ADD	INDEX	1 = Oprnd 0 = ACC	MSB			FILE ADDRESS				LSB	File is added to contents of accumulator or operand and results are stored in accumulator.
25	SUB	INDEX	1 = Oprnd	MSB			FILE ADDRESS				LSB	File is subtracted from contents of accumulator or operand register and result is stored in accumulator.
26	MPY	INDEX	Not used	MSB			FILE ADDRESS				LSB	9 LSB's of file are the multiplier and operand register is the multiplicand. The 16 MSB's of result are stored in accumulator, LSB's dropped by truncation.
27	SHF	Not used	Not used	1 = Arith 0 = end around	Oprn Left	ACC Left	ACC	No. of shifts MSB 1 less than number of positions through which data is shifted.			LSB	Content of register is shifted as specified by bits 4 thru 7. The number of places the data is to be shifted is specified in bits 0 thru 3.
30	CFB	INDEX	Not used	MSB			FILE ADDRESS				LSB	Copy 10 LSB's of file into program add register and branch.
31	MCS	INDEX	Not used	MSB			FILE ADDRESS				LSB	Absolute magnitude compare of operand and contents of file. The next instruction is skipped if ABS value of operand ≤ file number (which must be POS).

Table 5-16. Command Set Description - Continued

OP code	INST	Command word utility										Command Description
		Index Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
32	DFS	INDEX	Not used	MSB ← FILE ADDRESS → LSB								Decrement contents of file by 1 and skip next instruction if contents were 0.
33	CFI	INDEX	Not used	MSB ← FILE ADDRESS → LSB								Copy 8 LSB contents of file into index register.
34	EQS	INDEX	1 = Oprnd 0 = ACC	MSB ← FILE ADDRESS → LSB								Equality of skip. The next instruction is sequence is skipped if the file does not equal operand or accumulator as specified by bit 8.
35	DIS	Not used				NOT USED						Decrement index register and skip next instruction if index register was 0.
36	CCB	MSB ← BRANCH ADDRESS → LSB										Branch to program location specified by bits 0 thru 9. This is an unconditional branch.
37	BST	MSB ← BRANCH ADDRESS → LSB										Branch to program location specified by bits 0 thru 9. Store present command register address.

decode logic, in conjunction with the command timing logic, generates the phase T1, T2, and extend signals which permit the AP the discrete times required to process an instruction and to extend those times dependent upon the complexity of the instruction. The source for data derived from the data bus is dependent upon the actual instruction and, in some cases, the contents of the utility field. The data bus select logic utilizes the decoded instruction information and pertinent utility field bits to select one of eight potential data bus sources. Table 5-17 defines the eight data bus source codes. The sense switch logic, under control of the SSW and RSW instructions, stores various AP internal and external status indications and supplies these indications for testing by the TSS instruction. The sense switch logic also monitors the status of data transfer from the high speed input and high speed output buffers.

Table 5-17. Source Codes

Bit 9	Bit 8	Bit 7	Source register
0	0	0	Accumulator
0	0	1	Operand
0	1	0	Low speed output
0	1	1	High speed input
1	0	0	Data file
1	0	1	Command register
1	1	0	Program address register
1	1	1	Fault bits

a. *Command Copy Register (fig. 5-21, FO-11).* The -command copy register provides supplementary storage for the 5-bit command word operational code and additional decoding for instructions. The 5-bit operational code is loaded into the command copy register from the same source and by the same advance command as for the command register. The outputs from the command copy register provide additional loading for the various decoding logic in the AP. Refer to table 5-15 for the significance of the various operational codes. Operational codes CCR 10, CCR 11, CR 12, CR 13, and CR 14 enable the BST decode. When the MSB of the utility field (CR09) is a ZERO, the extend TI for branch signal is supplied to the data file storage and address and instruction decode logic. Operational codes CCR10, CCR11, CR12, CR13, and CR14 define the CBA instruction and develop a control signal to the arithmetic logic. Operational codes CCR11, CR12, CR13, and CR14 define both the CCB and the BST instructions. However, the priority logic in the data bus select logic will utilize this CCB output only if the BST is inactive. The operational code 1's digit output is low for CCR10 and CCR11 and high for the remaining three permutations. This level is utilized in the program memory and command register for further instruction decoding.

b. *Command Timing (fig. 5-22, FO-12).* Command timing generates phase T1 and T2 control signals and extends these operation times to accommodate the current instruction. The circuit also develops the multiply function select and carry enable codes for an MPY instruction. The operation of the command timing logic is dependent upon the number of operations or clock times required to implement the particular instruction. There are two basic phases: T1 and T2. Each can be extended for one additional clock time by the extend circuit. For more time-consuming instructions, an extend counter is provided to extend phase T2 by a predetermined number of clock times.

(1) Simple instructions (SSW, RSW, STA, and STO) require only phase T1. Phase T2 is utilized for more complex instructions (MPY, SHF, or BST). The extend circuit is utilized for phase T1 and/or phase T2 primarily to permit memory address settling time when information is read from the data file. The extend counter is utilized to count the number of iterative operations, such as accumulator shifts or multiplication operations, or to provide a timeout for nonsynchronous instructions which involve the low speed output buffer (CFL and CBL). Phase T1 and T2 timing states are illustrated in figure 5-23. Phase TI and T2 generation logic is a free-running loop with the extend options determined by control signals from the instruction decode logic. When an instruction is completed, the advance command gate is enabled. The resultant advance command signal sets the T1 circuit and resets the T2 circuit, if required. The advance command signal to the program memory and command register increments the program address counter and loads the new command into the command register. The advance command signal is also distributed to various AP logic, indicating that a new instruction is about to be processed. As long as the current instruction is a single-step instruction and no extensions are required, the advance from the T1 signal again generates an advance command signal and the AP proceeds to the next addressed command.

(2) Examination of the current instruction and its accompanying utility field by the instruction decode logic may dictate that phase T1 must be extended by one clock time. This is indicated by the extend T1 signal which sets the extend circuit. The extend T1 signal also inhibits the advance from T1 input, blocking the advance command and the T1 valid input, maintaining the phase counter in the T1 phase. The T1 not extended output now goes inactive and permits the program memory and command register to access the next instruction. The T1 valid input going active indicates that all phase T1 conditions for the particular instruction have been satisfied. As long as no advance command signal is generated at this time, the T1 VALID signal resets the T1 circuit and sets the T2 circuit, initiating phase T2. Should no further extension be required for the current instruction, the active overflow and T2 FF signals enable the advance from T2

unless extended to generate the advance command signal, initiating a new instruction cycle.

(3) For a CFL, CBL, SHF, or MPY instruction, the extend counter is utilized to prolong phase T2. When phase T2 is prolonged, the CFL or CBL instruction is timed out and the required number of operations for the SHF or MPY instruction are controlled. The extend counter is also loaded by the T1 VALID signal, temporarily inhibiting the advance command signal. After the specified number of clocks, the overflow signal in conjunction with the T2 FF signal generates the advance command signal as previously described. Several instructions may require the program memory address counter to be advanced, which requires one additional phase T2 clock time for the memory address to settle. This condition is indicated by an active extend T2 necessary signal which inhibits the command advance signal and sets the extend circuit for one clock time. The escape gate is utilized to reinitialize the T1 and T2 circuits for a lockup in the reset condition at system turnon time.

(4) The extend counter is utilized during a CFL, CBL, SHF, or MPY instruction to prolong phase T2. For an SHF instruction, the 4 LSBs (CROO thru CR03) of the current utility field are routed through the extend counter select. These bits, which determine the number of places that the data will be shifted, are loaded into the extend counter by the T1 VALID signal. Actually, the number of shifts generated is the shift count plus one. The counter is then incremented until the overflow signal generates the advance command signal, terminating the instruction cycle.

(5) For a CFL instruction, the active set command FF and the inactive MPY instruction inputs causes the extend counter to be loaded with a 1 0 11 code at T1 valid. The counter is then incremented to overflow (four clocks or 800 ns). Normally, the front panel logic responds with an indicator within this time, setting the extend circuit and, subsequently, the advance command. Should the extend counter time out, the overflow signal generates the advance command signal and the AP proceeds to the next instruction.

(6) The CBL instruction utilizes two extend counter codes: 1 0 11 when CR05 is a ONE (for a command output) and 1 0 01 (for an enable output). Thus, the timeout for a command output is 800 ns and for an enable output is 1.2 us.

(7) For an MPY instruction, the extend counter is loaded with a 0 1 1 1 code, which requires eight additional counts to overflow. The 9 LSBs of the current data file information are utilized as the multiplier and are applied to the multiplier select. The 3 LSBs of the extend counter, which will cycle from binary 0 thru binary 7, are used to select the 0 thru 7 outputs of the multiplier select. The data file input to the multiplier select is arranged so that the two continuous bits, representing the current multiplier LSB and the previous multiplier LSB, are selected and applied to the MPY function. The multiply function provides the required multiplication function select and carry control codes for the arithmetic operation dictated by the multiplier bit comparison. In accordance with the multiplication scheme, a right shift enable is forwarded to the arithmetic logic until the final product is attained.

(8) The multiplication scheme provides a properly signed product regardless of the combination of multiplier and multiplicand signs. During a multiply operation, the multiplicand is stored in the operand register, the partial product in the accumulator, and the 9-bit LSBs from the data file are utilized as the multiplier. The logic procedure for obtaining the required product is as follows:

(a) Set the accumulator to all ZEROS.

(b) Beginning with the multiplier LSB, compare each multiplier bit with the next LSB (a ZERO previous LSB is assumed during the first compare).

1 When the two bits are equal, shift the accumulator right one bit.

2 When the two bits are not equal and the current (most significant) bit is ZERO, the multiplicand is added to the partial product and the resultant partial product is shifted right one bit.

3 When the two bits are not equal and the current bit is ONE, the multiplicand is added to the partial product and the resultant partial product is shifted right one bit.

For the most significant current bit comparison, the above rules apply except that the right shift is inhibited. Table 5-18 illustrates the bit combinations, the resultant decoding, the ALU input codes, and attendant ALU functions.

c. *Sense Switch Logic (fig. 5-24, FO- 3).* The sense switch logic stores various AP external and internal status indications. The sense switches operate under control of the SSW, RSW, and TSS instructions to set, reset, and test the switches. The 10-bit utility field in the instruction command words determines which one or combination of sense switches are affected. Sense switch 9 is also controlled by signals from the high speed input and high speed output buffers.

(1) Each of the sense switches is involved with a specific AP function. The state of the sense switch at any particular time is dependent on the sequence of instructions being processed, the status of the associated information and, in the case of sense switch 9, the status of data transfer between the AP and the DC. The following are brief descriptions of the functions with which the 10 sense switches are involved:

SSW 0 - Front panel switch group 111 - 116
SSW 1 - X, Y force stick processing

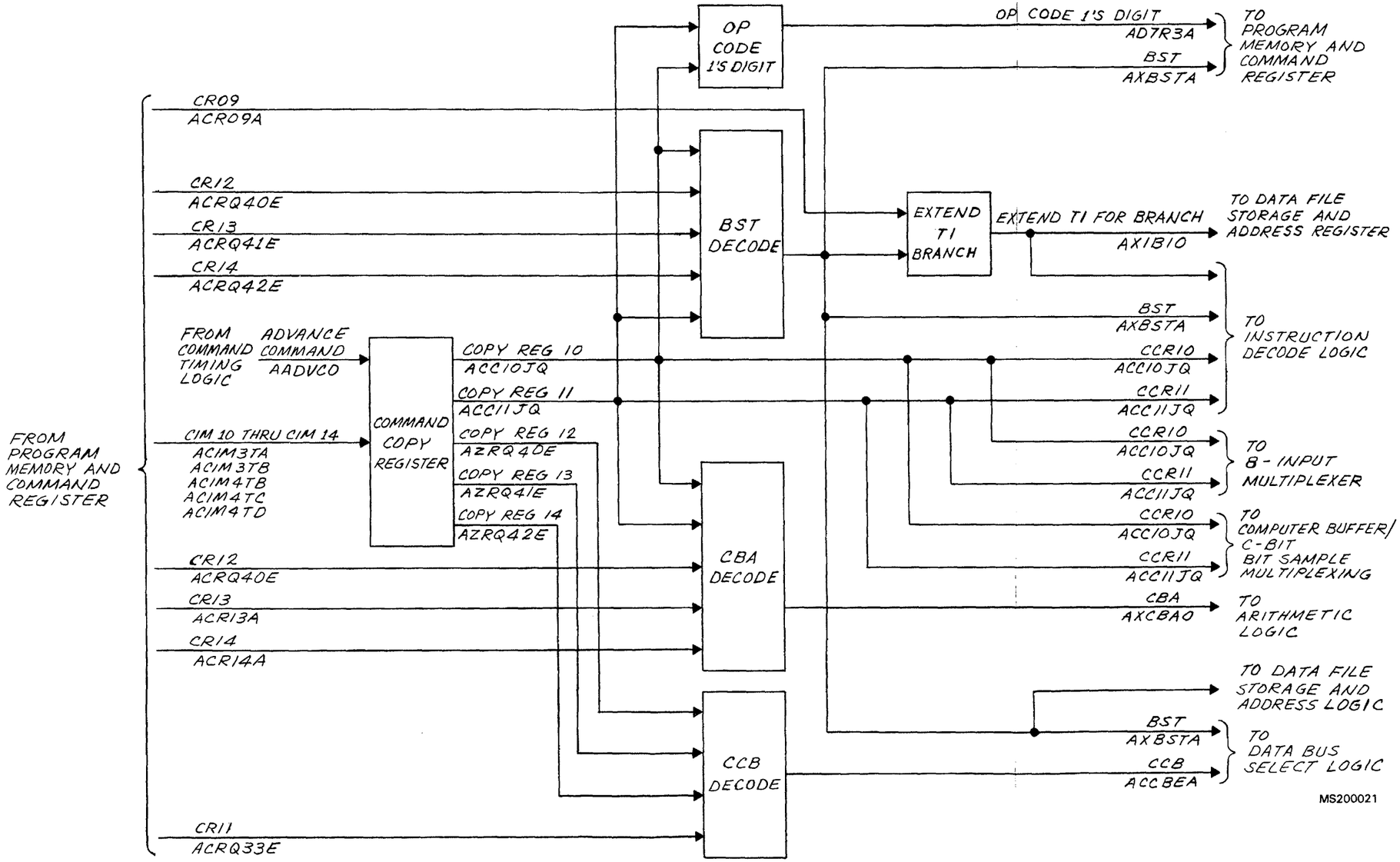


Figure 5-21. Timing and Control Command Copy Register Block Diagram

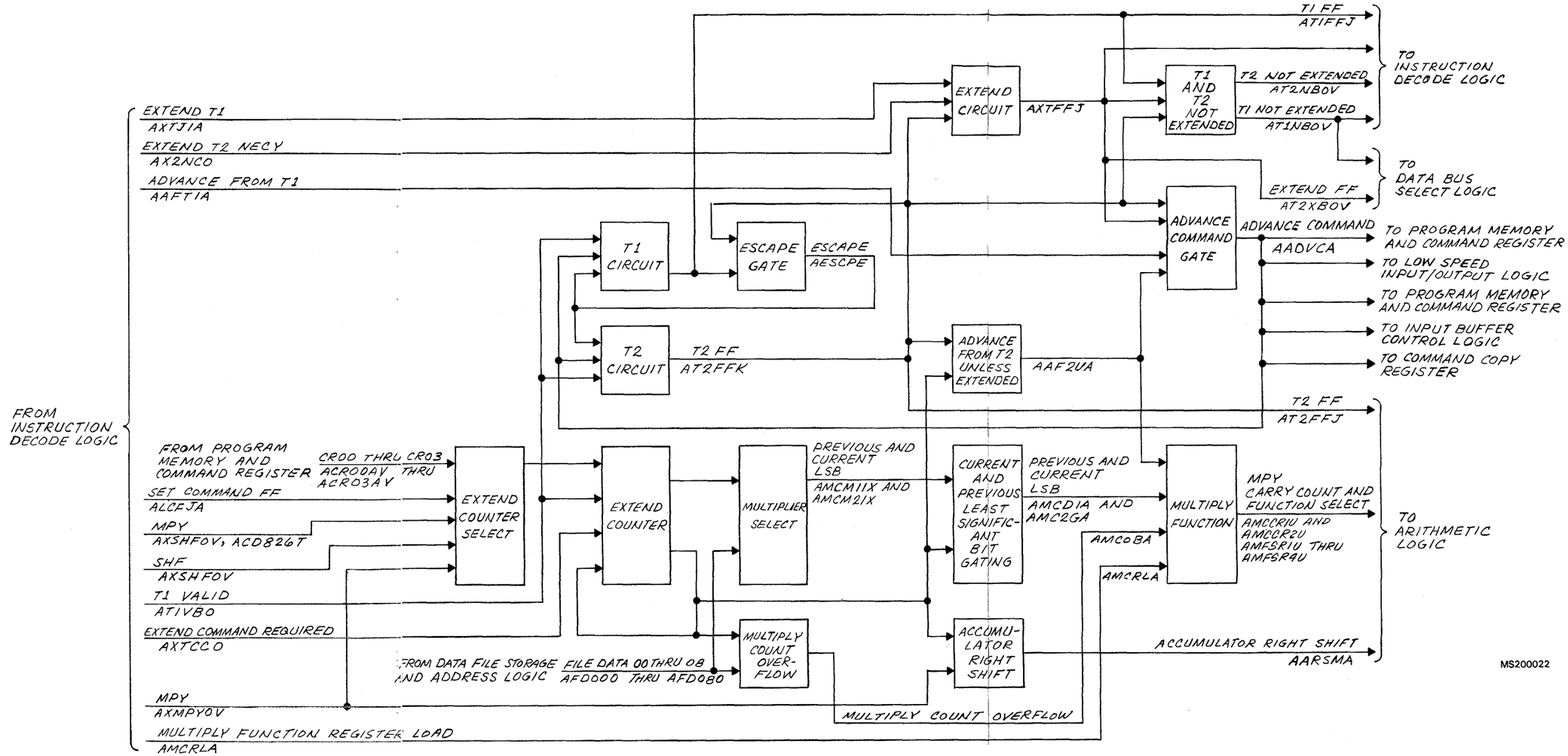


Figure 5-22. Timing and Control Command Copy Timing Block Diagram

T1V = T1 VALID
ADVC = ADVANCE COMMAND

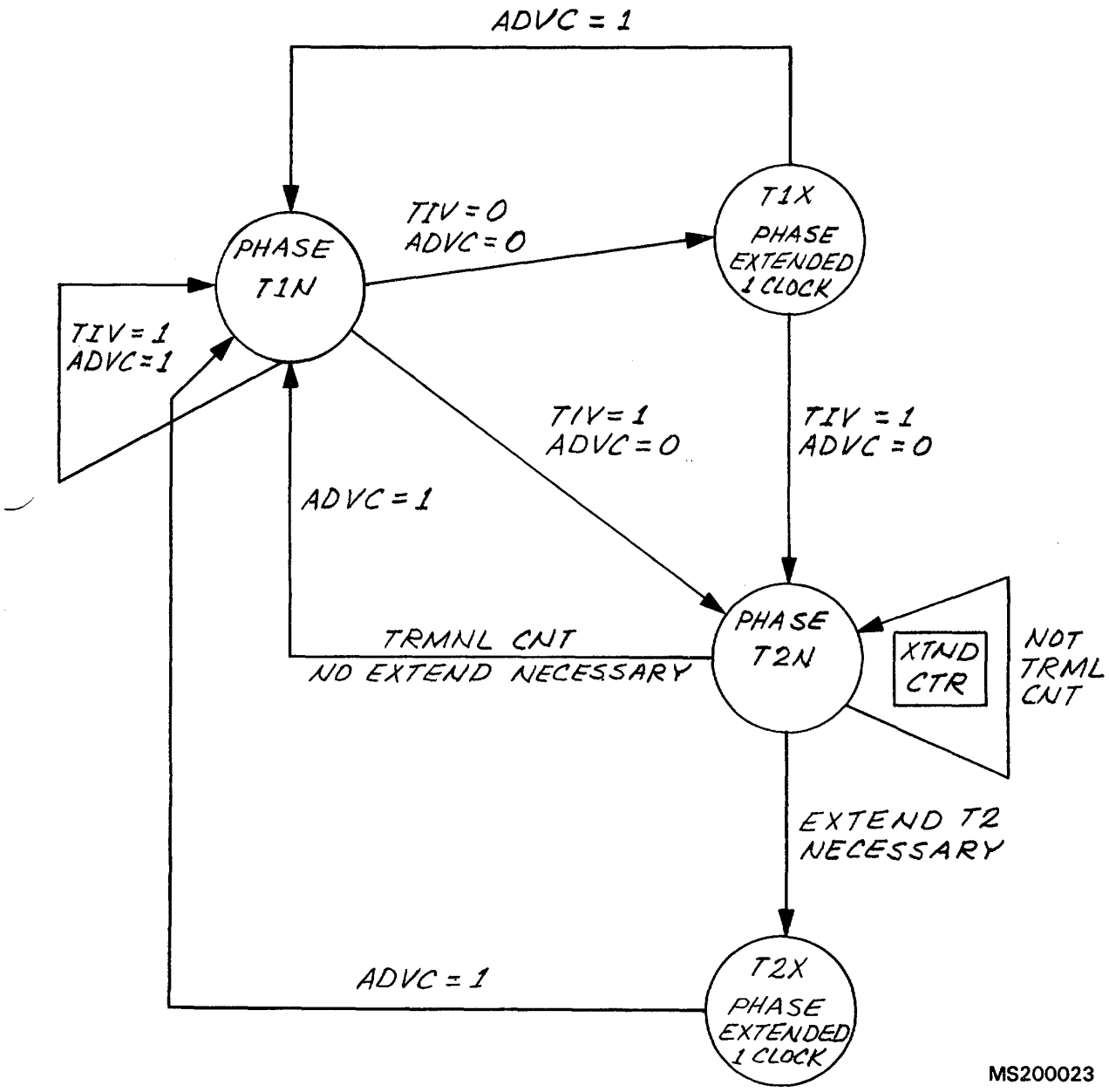


Figure 5-23. Phase T1/2 Timing States

Table 5-18. A Multiply Function Decoding

Multiplier LSB		Decoder input			Decoder output				ALU input						
Current	Previous	A2	A1	A0	3	2	1	0	S3	S2	S1	S0	C_N	$\overline{M}$	ALU function
0	0	L	L	L	H	H	H	L	L	L	L	L	H	L	A
0	1	L	L	H	H	H	L	H	H	L	L	H	H	L	A plus B
1	0	L	H	L	H	L	H	H	L	H	H	L	L	L	A minus B
1	1	L	H	H	L	H	H	H	H	H	H	H	H	L	A
Accumulator clear															
0	Terminal	H	L	L	H	H	H	H	L	L	H	H	H	H	Logic 0
1	Count	H	H	L	H	H	H	H	L	L	H	H	H	H	Logic 0

SSW 2 - Front panel switch group 40-51
SSW 3 - AP status reports
SSW 4 - Front panel switches 22 and 23
SSW 5 - Reinitialize location blinker
SSW 6 - Display console initialization
SSW 7 - DOU inhibit
SSW 8 - CPU request generation
SSW 9 - AP/DC message transfer status

(2) An SSW instruction allows the 10-bit utility field to be routed to the 10 sense switches. A ONE in any one or combination of this field sets the associated sense switch. For an RSW instruction, a ONE in any one or combination of the utility field resets the associated sense switch. Sense switch 9 is also set for a CBH instruction when a new message is available at the output of the high speed input buffer (ie, input buffer bit 15 and reset input buffer ready signals both active). Sense switch 9 is reset each time data is loaded into the high speed output buffer (ie, high speed load active).

(3) Sense switch sample gating continuously compares the states of the sense switches with the current utility field. The switch test skip signal goes high when any one of the sense switches is reset when the corresponding utility field bit is a ONE. This output is utilized by the TSS instruction in the instruction decode logic.

d. *Instruction Decode (fig. 5-25, FO-14).* The instruction decode logic decodes the 5-bit operational code currently stored in the command register to determine which one of 32 instructions shall be imple mented during the current operation. The decoded instruction is then combined with various AP timing and control signals to ensure that the instruction is performed upon the proper data and in the designed sequence. The significance of the 5-bit operational code and 1 O-bit utility field for each instruction is detailed in table 5-16. The significance of the source code bits is indicated in table 5-17. The operational codes are shown octally (00 thru 37) with each associated instruction. The attendant functions of each pertinent bit of the associated utility field is also indicated, in addition to a brief description of the instruction's logic functions. Table 5-16 should be referred to when analyzing each of the instruction decode functions. Command word bit 15 is not used.

(1) Command register bits 10 thru 14 are combined by a command decoder to develop an active level on one of 32 instruction output lines. The outputs from the decoder are distributed to logic elements in the instruction decode logic and other AP functional logic circuits. The command decoder octal outputs are used for groups of instructions that have common functional logic requirements.

(2) When either SSW or RSW goes active, a signal is supplied from the SSW/RSW gating to the sense switch logic to set or reset the sense switches as selected by the associated utility field. As long as the AP is in a go condition, and any selected sense switch is currently reset (skip test active), a TSS instruction to the TSS gate circuit generates the switch test skip signal which instructs the program memory and command register to skip the next instruction.

(3) Either an active STH instruction or a transfer high-speed input required signal from the program memory and command register will result in a transfer high speed input signal to the high speed input buffer control and the high speed output buffer. An active CBH or CFH signal instructs the high speed output buffer to accept a word from the indicated source.

(4) An active CFO or CBO instruction generates a load operand signal from the operand load circuit, which transfers the contents of the designated source into the arithmetic logic operand register at time T1. An active CBI or CFI instruction generates the index counter load signal from the index counter load circuit at time T1

(5) An active STL instruction generates the transfer low speed input via bus. This output is also activated by transfer low speed input required signal from the program memory and command register. However, since this input is a function of the copy instructions (CBI, CBA, CBO, and CBH), the request read signal is inhibited unless bit 6 of the current utility field is a ONE (indicating request data) and the STL instruction is inactive.

(6) An active BST to the file write circuit generates a file write enable signal to the data file storage and address logic at time T1. This instructs the data file storage and address logic to write the present command register address into the file and branch to the address specified by the current utility field. The CR12 and CD octal 1X inputs define instructions CFA, CFO, CFL, and CFH, for which data from the file is stored in the designated register. These inputs also generate a file write enable at time T1. For a DFS instruction, a DFS file write-enable signal is generated when command timing supplies an extend FF signal. The decremented file contents are then written back into the addressed file location.

(7) The CFL, CBL, SHF, and MPY instructions each require operation of the timing and control extend counter to prolong the phase T2 time slot. Any one of these instructions provides an extend command required signal from the extend command gate to command timing. An active CFL or CBL instruction to the low speed output enable provides a low speed output enable signal to the low speed I/O logic. The CBL instruction also activates the set command FF output as long as command bit 5 is a ONE.

(8) Several conditions will supply the accumulator load signal to the arithmetic logic. An active CBA, MPY, or CFA will load the accumulator from the designated source at time T1 Instructions 20 thru 27 (octal 2X) and DFS involve accumulator operations. The ESB command allows accumulator comparison; a SHF command with a bit 4 ONE (CR04 active) allows an accumulator shift. Since either of the above conditions prohibit disturbing the accumulator contents, they are used as inhibits to the accumulator load circuit. When the proper conditions are present, the T2 not extended signal generates the accumulator load signal.

(9) The bit/word test skip signal is generated at time T2 by an ESB or EQS instruction when the arithmetic logic indicates other than equality (ALU = ALL Is) between the data being compared. The skip MCA signal is generated at time T2, during an MCS instruction, when the absolute value of the operand register is equal to or less than (MSB carry high) the value being compared.

(I0) Some instructions and skip conditions require an extension of the T I and/or T2 phases to complete. The extend T2 necessary signal is generated whenever a bit/word test skip, skip MCA, or DFS signal occur. The extend T2 necessary signal is also developed when data is being supplied to the low speed I/O (acknowledge low speed input).

(11) Logic is provided to temporarily halt processing for instructions CBH, CFH, and STH. The CBH and CFH instructions involve the high speed output buffer which must wait for a DC acknowledgement for processing data. The STH involves the high speed input buffer, which must have a data word output available before the instruction can be implemented. An STH command develops the transfer high speed input. If the high speed input buffer is not prepared to output data, the input ready sync signal inhibits the T1 GO signal and enables the I/O wait line. The inactive T1 GO signal prevents the file write enable from being generated. When the input ready sync signal goes inactive, the I/O wait condition is terminated and the instruction is processed. In a similar manner, for a CBH or CFH instruction, a low extend T1 necessary signal inhibits the T1 GO signal and enables the I/O wait condition until the high speed output buffer is prepared to process a data word.

(12) Various instructions and contingent conditions require that phase T1 be extended. For example, any instruction that involves transfer of information from the data file storage requires additional time for the memory address to settle. A TSS instruction directly enables the T1 extend circuit. The T1 extend circuit collects a group of instructions that may require extension of phase T1. The extend T1 for branch signal indicates a BST instruction or a ONE in index CR bit 9,either of which may require extension of phase T1 for the program address to settle. The decrement index skip signal is enabled whenever a DIS instruction is generated while the index register reflects all ZEROS (index TC active). The above conditions are combined with the MPY, CFI, and CFR instructions in addition to the switch test skip and copy file signals to generate the extend T1 signal. The extend T1 signal is enabled by the above stated signals only when the logic is in the phase T1 GO condition.

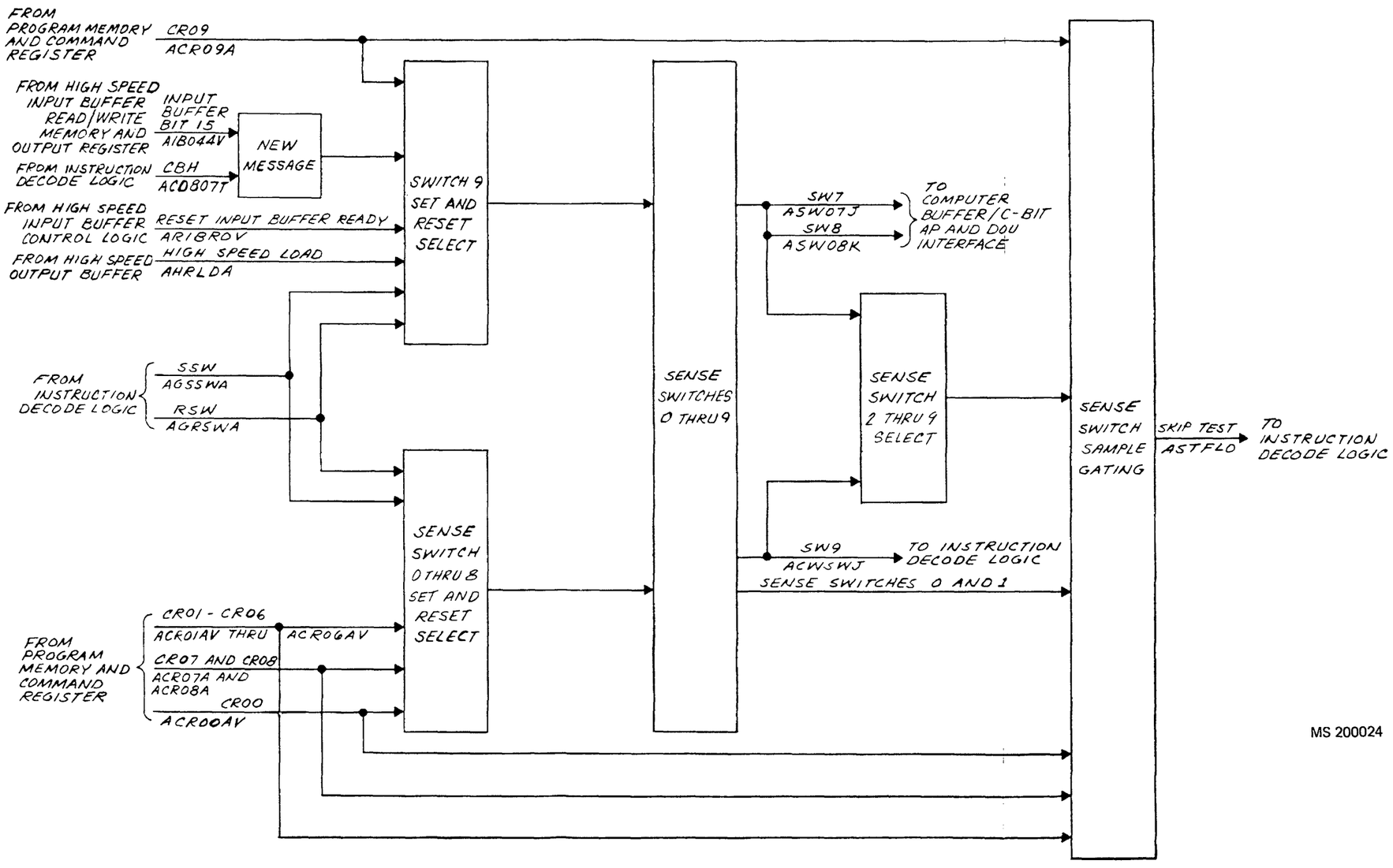
(13) The multiply function register load signal is generated when the extend T1 signal goes active during an MPY instruction. The index count enable goes active when the T1 GO is enabled and a DIS instruction is active. The T1 VALID signal indicates that all preconditions for a particular instruction phase T1 operation are satisfied and that the T1 phase for that instruction can be terminated. These conditions are the absence of an I/O WAIT, TI WAIT, or extend T1 signal and the active T1 flip-flop signal from command timing. The advance from T1 signal is developed when, for a specific group of instructions, all conditions are satisfied to permit the logic to advance from TI to the next instruction phase.

e. *Data Bus Select (fig. 5-26, FO-15).* The data bus select utilizes current command word information to select the data bus source for a particular instruction.

(1) The bus select is controlled by the CD octal 80 signal from the instruction decode logic. When this signal goes low (indicating that the current instruction is one of octal 00 thru 07), the bus select chooses the CR07, CR08, and CR09 inputs for data bus selection. These three bits constitute the source code for copy instructions CBI, CBA, CBO, CBL, and CBH (refer to table 5-17). The bus select coding is identical to that for the source coding. For all other instructions which utilize the data bus, the CD octal 80 input is high.

(2) The operand register is selected for a group of instructions when utility bit CR08 is a ONE. These instructions are ESB and EQS and include all instructions 20 thru 27 (CD octal 82 high), with the exception of MPY and SHF. The low speed data is selected by the STL instruction while high speed data is selected by the STH instruction.

(3) The copy file instructions are defined by CD octal 81 and CR 12 going high, selecting data file information. When phase T2 is extended, the data file source is selected by instructions CFB, MCS, DFS, or CFI (CD octal 83 and CRI2 high). The command register is utilized as the bus data source for a CCB or BST command. The T1 not extended signal, which indicates that the timing and control is in phase T1, permits the BST instruction to select the program address counter as the data bus source.



MS 200024

Figure 5-24. Timing and Control Sense Switch Logic Block Diagram

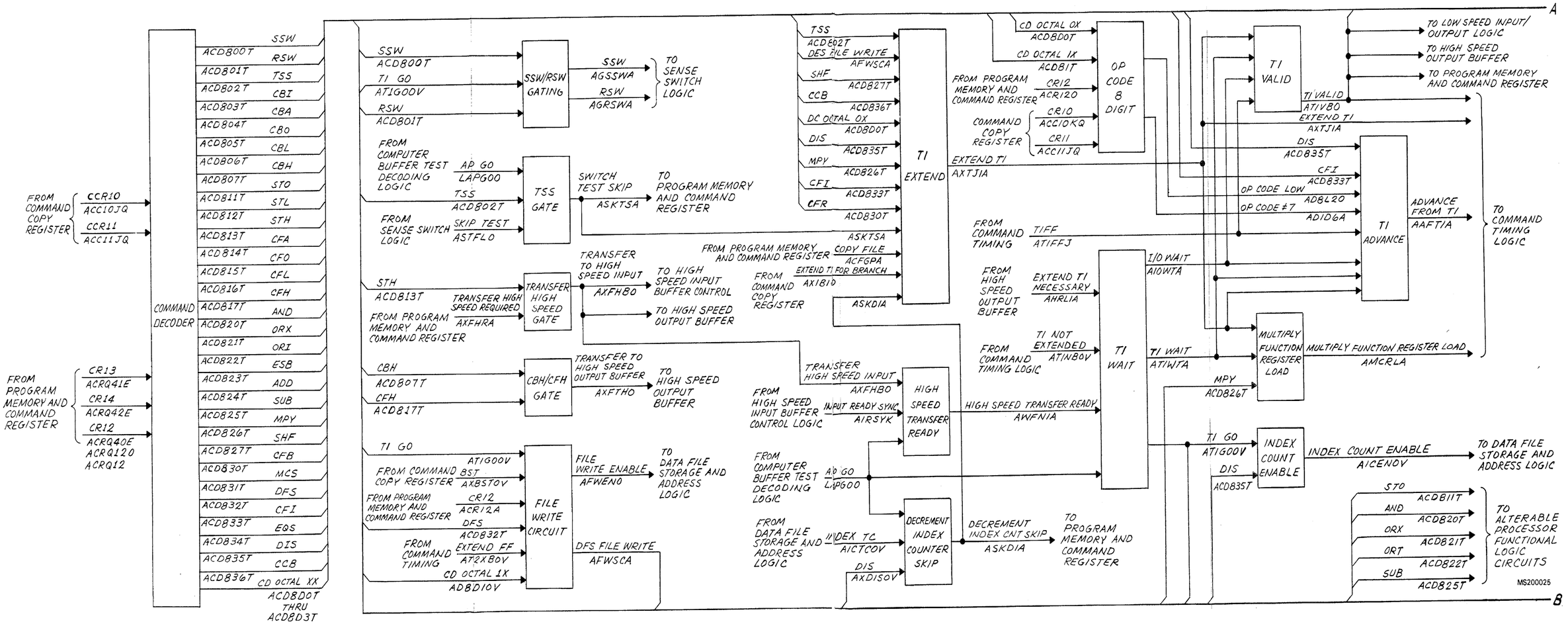


Figure 5-25. Timing and Control Instruction Decode Block Diagram(Sheet 1 of 2)

5-241/(5-242 blank)

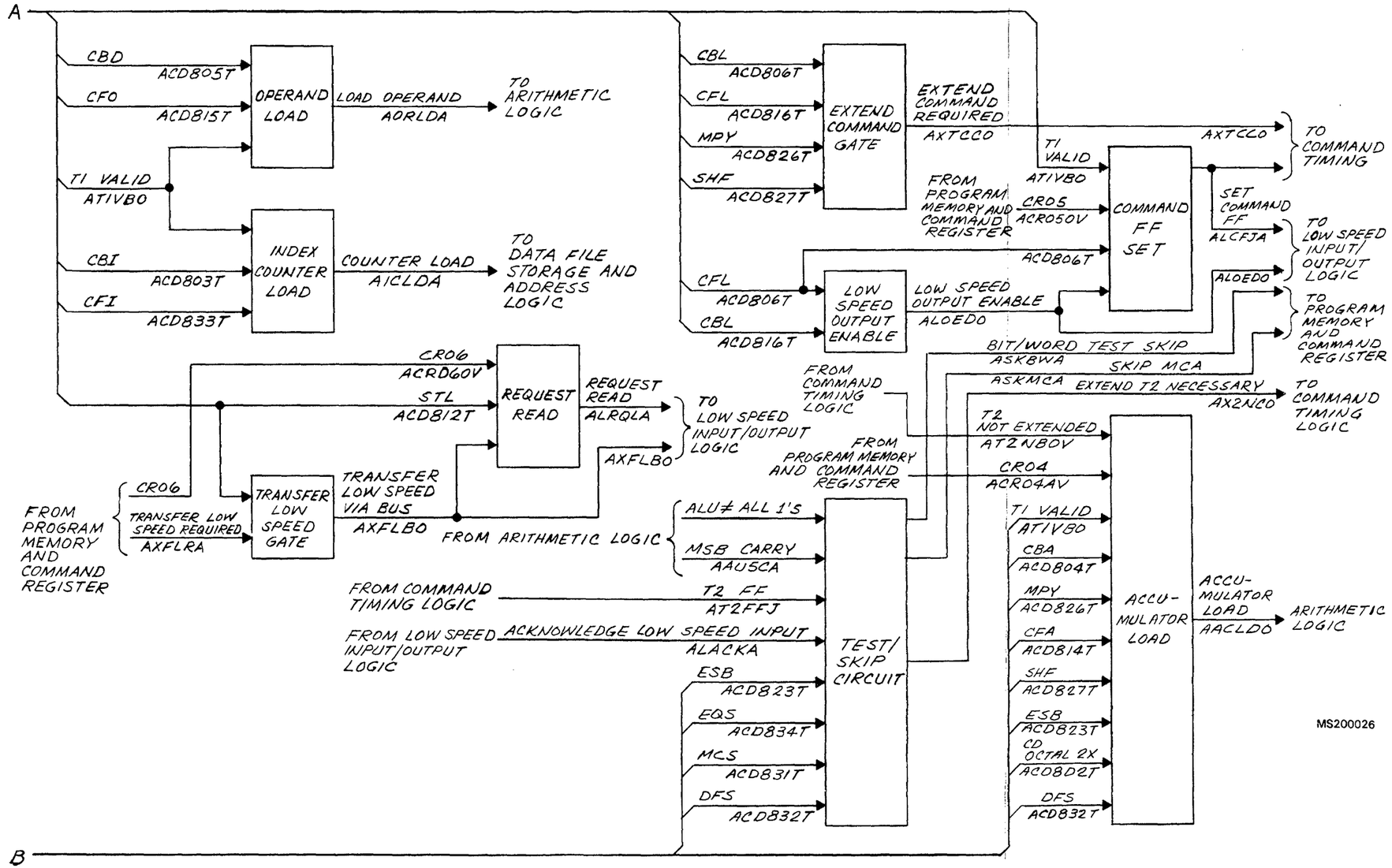
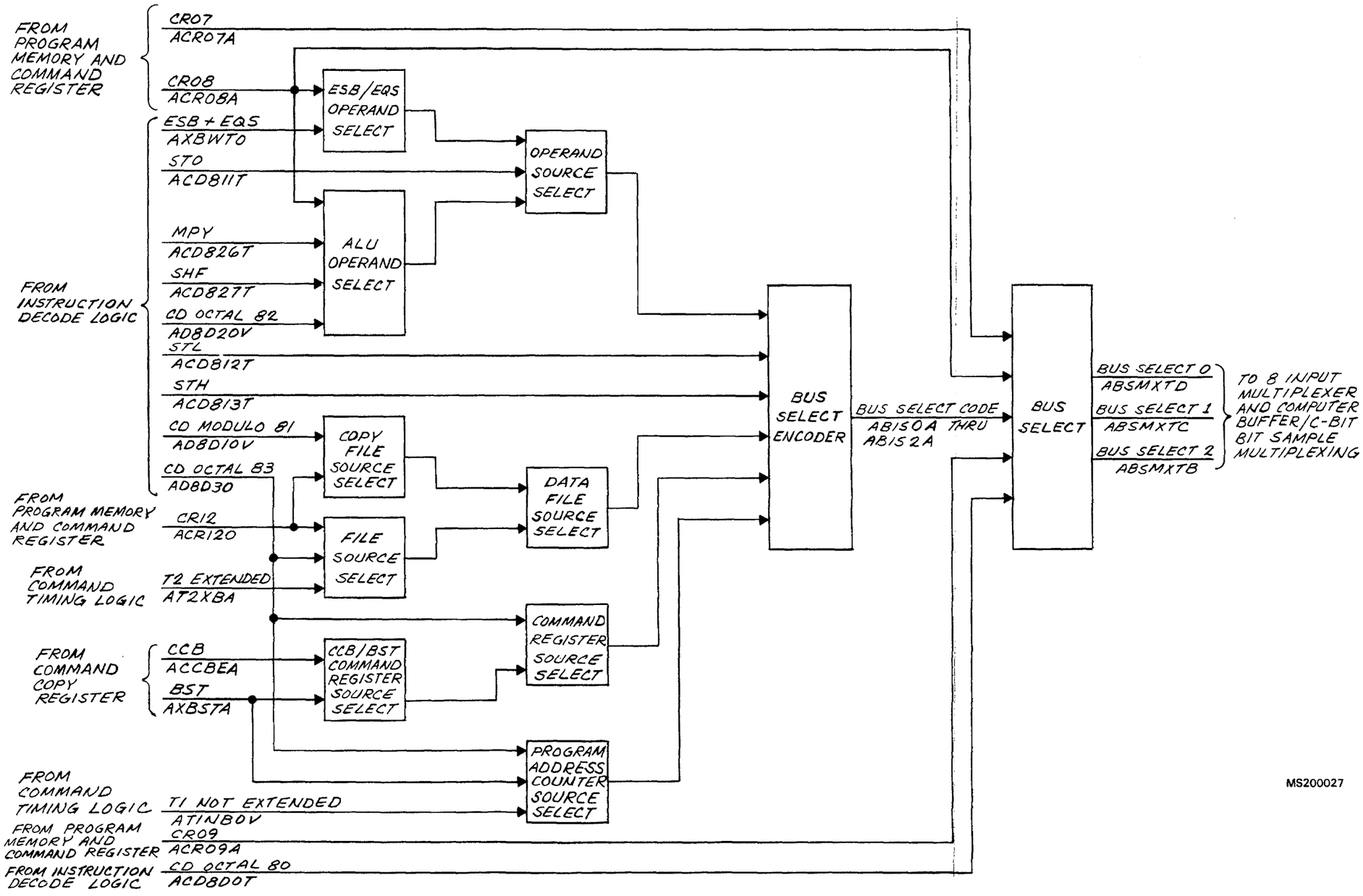


Figure 5-25. Timing and Control Instruction Decode Block Diagram(Sheet 2 of 2)

5-243/(5-244 blank



MS200027

Figure 5-26. Timing and Control Data Bus Select Logic Block Diagram

Section IV. DISPLAY CONTROLLER

5-17. General (fig. 5-27). The DC consists of the following eight sections:

Arithmetic logic
Data file storage and address logic
8-input mux
Program memory and command register
High speed output buffer
Serial-to-parallel buffer
Low speed input buffer
Timing and control

The DC is a special-purpose miniprocessor designed and programmed to accept display buffer input messages preselected by the AP, and to format the data for distribution to the DG. The DC also provides the controls necessary to interface the VC and the RIE with the DG. The DC continuously monitors the DB to determine if data is available. If data is not available, the VC is checked for transfer of sweep information to the DG. When the DB contains data, the start of a message is indicated by the MSB of the first word sent. During this time, the VC is again checked for sweep information. The DC will then read in the subsequent words in the message, format the message for the DG, make checks of the VC, and send the data to the DG ensuring that the DG has completed one task before given another task. The DC individually sends each symbol, line, and alphanumeric (A/N) to the DG. Positional data is sent for each symbol, line, and A/N along with a check for completion before proceeding. Upon detecting that sweep information is loaded and read to be transferred from the VC, the DC saves the current DG X and Y coordinates in the scratchpad memory, passes sine and cosine information from the RIE to the DG, and enables the transfer of sweep information from the VC. This process interleaves the radar sweeps with the synthetic data received through the DB. The DC utilizes a miniprocessor to transfer and manipulate the DB information. Information is transfer- red throughout the DC, as for the entire display console, in the form of 16-bit words. A repertoire of 30 instructions provides the various data transmissions, logical, arithmetic, branch, and miscellaneous routines required. A 1024-word PROM stores the programmed sequence of instructions that control all operations. The DC program listings and additional information is provided in section XIV. A 256-word PROM is provided to store constants and tables. This read-only storage is augmented by a 64-word RAM for scratchpad storage of various resultants obtained during message processing.

a. *Arithmetic Logic.* The arithmetic logic provides all the logical, arithmetic, comparative, and shifting manipulation of data for the DC. The arithmetic logic processes data in 16-bit parallel mode, with simple operations (addition, subtraction, AND, OR, etc.) requiring approximately 200 ns and more complex operations requiring up to approximately 2 μs.

b. *Data File Storage and Address Logic.* The data file storage and address logic contains the addressable 256-word constant PROM and the 64-word scratchpad RAM. The memories are addressed by the index counter/register, which can be decremented sequentially or loaded with a new address from the command register output in the event of an indexing instruction.

c. *8-Input Mux.* The 8-input mux routes one of seven information sources to various DC functional circuits. The 8-input mux output is the data bus which is the primary path for DC data transmission.

d. *Program Memory and Command Register.* The program memory and command register contains the 1024-word program memory which stores the DC sequence of instructions. The program address counter can be incremented sequentially or loaded from the data bus. This counter is incremented or loaded at the end of each instruction cycle by the advance signal. The command register stores the current operational code and utility field for decoding by timing and control and for low speed control data distribution to the DG.

e. *High Speed Output Buffer.* The high speed output buffer provides temporary storage for the high speed data being transmitted to the DG.

f. *Serial-to-Parallel Buffer.* Radar SIN 0 and COS 0 position data, accompanied by a sweep data strobe, is supplied from the RIE to the serial-to-parallel buffer. The serial-to-parallel buffer converts the data into parallel form for distribution to the 8-input mux. The data represents radar sweep positional information which indicates the direction the radar antenna is pointing.

g. *Low Speed Input Buffer.* The low speed input buffer supplies control data to the display generator to identify the data sent from the high speed output buffer. The low speed input buffer also receives a VC control signal which is used through the high speed output to increase the crt intensity.

h. *Timing and Control.* Timing and control contains the primary timing and instruction decode logic required by the DC to properly process the current instruction. The advance command indicates the termination of a current instruction and the initiation of the succeeding one. The advance command steps the command register the output of which is decoded to provide the instruction indication and supplementary information which specifies or amends the instruction. Timing and control then generates a sequence of timing signals; the number and duration are dependent upon the complexity of the instruction. For certain instructions, the timing and control supplies a bus select code to the 8-input mux

identifying the source of information for the current instruction. Timing and control also interfaces with the DB for read/write modes of operation and with the VC for VC status and test control.

5-18. Arithmetic Logic Detailed Description (fig. 5-28, FO-16). The arithmetic logic consists of the following elements:

Arithmetic logic A thru D
OPR serial input gate
MSB arith gate
MSB end-around gate
Right shift input decode
Look-ahead carry generator
Carry sample
Stored count ≠ 0
ALU ≠all Is
MSB carry decode
ALU C-BIT sample low
ALU C-BIT sample high
ALU control decode logic
ALU function encoder
OPR shift decode
Right shift decode
ACCUM left shift decode

The arithmetic logic performs all the Boolean, arithmetic, comparison, and shifting manipulation of DC data. The function decoding for all Boolean and arithmetic operations is also performed by this circuit. The operand register, ALU input mux, ALU C-BIT sample mux, arithmetic logic unit, right shift mux, and accumulator (see fig. 5-29) is a detailed breakdown of arithmetic logic A thru D shown in figure 5-28, and processes 4 bits of the 16-bit word. The operand register and the accumulator provide the primary word-size scratchpad memories for the DC. An active load OPR (CFO + CBO) stores the 4 bits from the data bus into the operand register. An active shift OPR (SHF CR06) permits the operand register to be left-shifted. The serial input signal (OPR MSB CR07) permits an end-around left shift. The current operand data is supplied to the 8-input mux and to the ALU input mux. The OPR select determines whether the operand data or data file information is gated to the ALU B input. The other (A) input to the ALU is the data currently selected on the data bus. The ALU performs a variety of Boolean and arithmetic operations as determined by the mode, carry, and function inputs. The ALU output is routed through the right shift mux to the accumulator. Thus, the ALU operates on information from the data bus and either operand or file data. Accumulator data can be placed on the data bus to be combined with either operand or file data. In addition, data bus information can be routed directly through the ALU and stored in the accumulator. For an SHF instruction, the four bits can be shifted one place to the right in the right shift mux. The left shift input (SHF CR05) going active shifts the accumulator data left one place for each clock time that the signal remains active. The left shift input (CR07 ACC MSB) permits an end-around shift of accumulator data.

a. Individual output bits are provided to accommodate carry, shift, and equality comparison functions. The operand MSB is supplied to the next ALU stage in the event an operand shift function is required. The propagate carry and generate carry signals are applied to the look-ahead carry generator to provide synchronous carry generation for the next ALU stage. The ALU LSB is provided as an input to the next least significant ALU for end-around right shift operations. The accumulator MSB is supplied to the next significant ALU for left shift ALU operations.

b. The ALU control decode logic combines the pertinent instructions and required control bits to determine the ALU function. The inputs are decoded into seven function enable lines which are supplied to two ALU function encoders; table 5-19 lists the equations for each of the function enable lines. Each pertinent instruction will activate one function enable line to one or both of the function encoders. Table 5-20 lists the resultant function codes and the attendant ALU functions. Table 5-21 provides a complete listing of the ALU functions for the various permutations of ALU selection, mode, and carry indications. The mode (M) input, when high, inhibits the internal bit-to-bit carry. Each of the four stages are then independent functional entities and Boolean operations are performed. In this logical mode, the carry input is irrelevant and is ignored. When the mode input goes low, an arithmetic operation is performed. The carry input, when low, can then be propagated through the four stages of the ALU. The carry input and two carry outputs are combined in the look-ahead carry generator to provide the carry input for the next four-stage ALU. The data file information is distributed in groups of 4 bits. Inputs from the high-speed output buffer and to/from the 8-input multiplexer are shown internal to the circuits and are part of the arithmetic logic. The bussed inputs (OPR load and select, accumulator load, ALU function, mode and carry enables, and the various shift enables) are applied in parallel to all four arithmetic logic circuits. Operand register and accumulator information are daisy-chained through the four arithmetic logic circuits. Carry and equality signals are shown bussed to the appropriate output gating. The LSB for each ALU stage is routed to the next least significant stage to accommodate right shift operations.

c. Logic is provided to gate the outputs of the most significant ALU stage. When the CR07 bit is low, OPR bit 15 is gated to the first ALU stage operand register. The MSB ARITH gate is enabled by CR07 ACC BIT 15, and the MSB END AROUND gate is enabled by CR07 SHF ALU BIT 0. Any one of these conditions supplies a ONE to the LSB of the most significant ALU stage, providing the required MSB for a right shift operation.

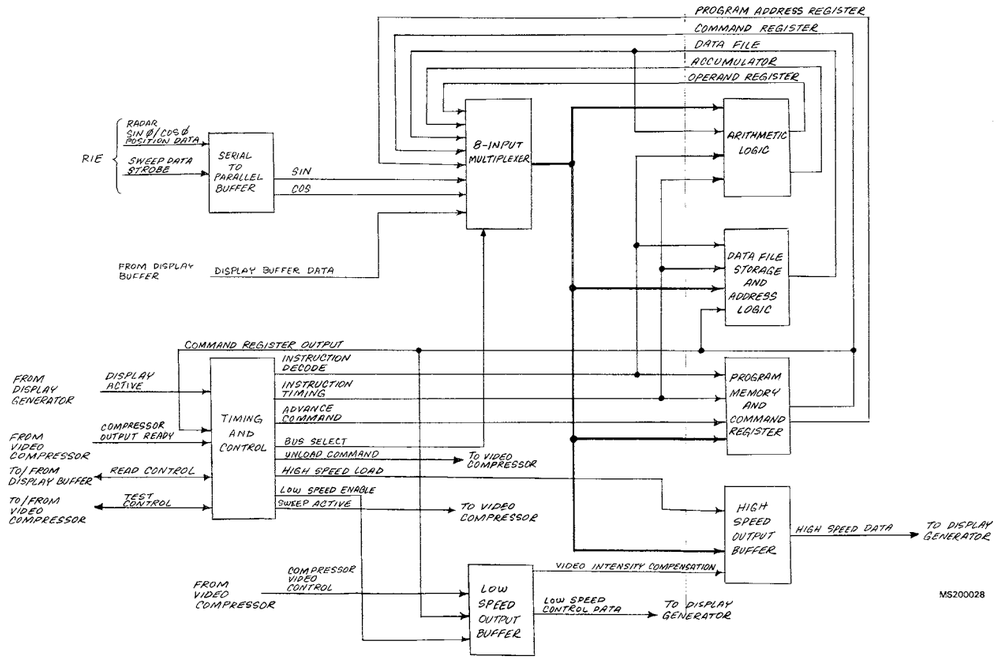


Figure 5-27. Display Controller Block Diagram

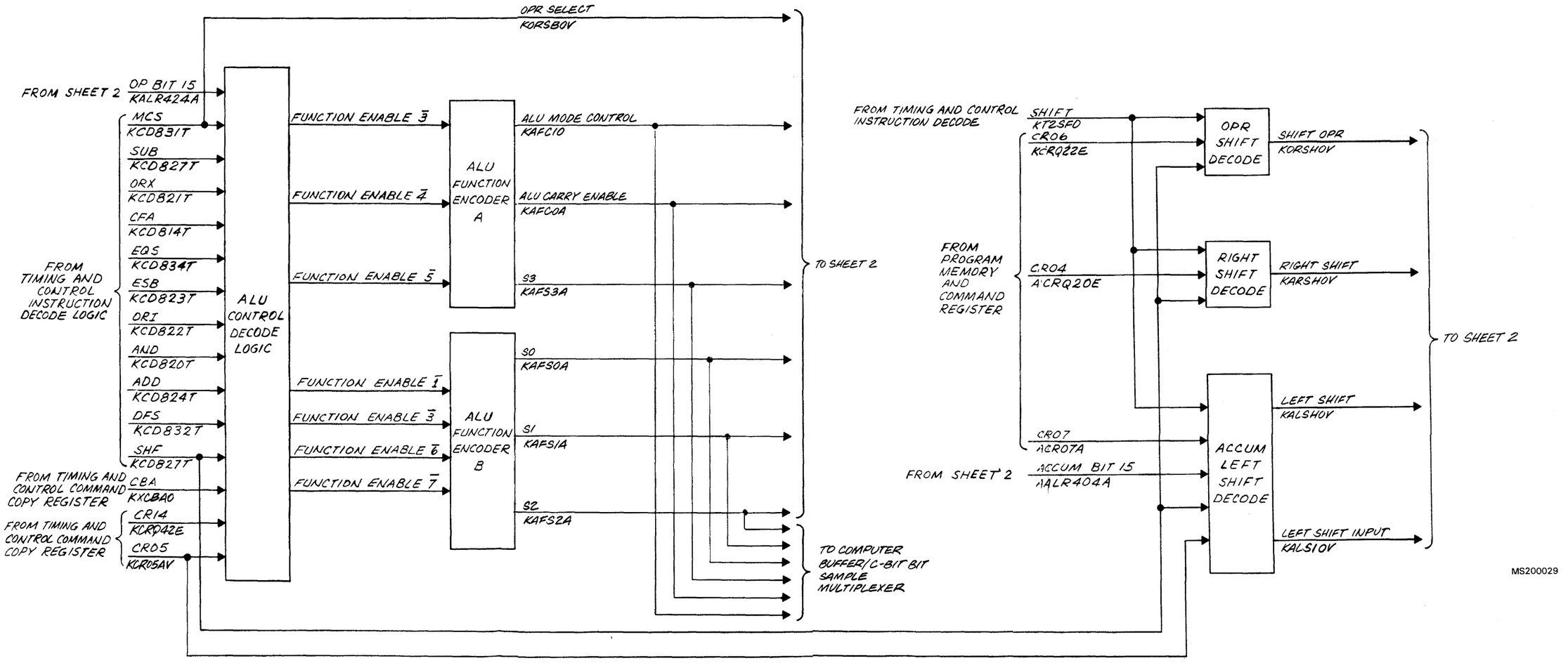


Figure 5-28. Arithmetic Logic Block Diagram (Sheet 1 of 2)

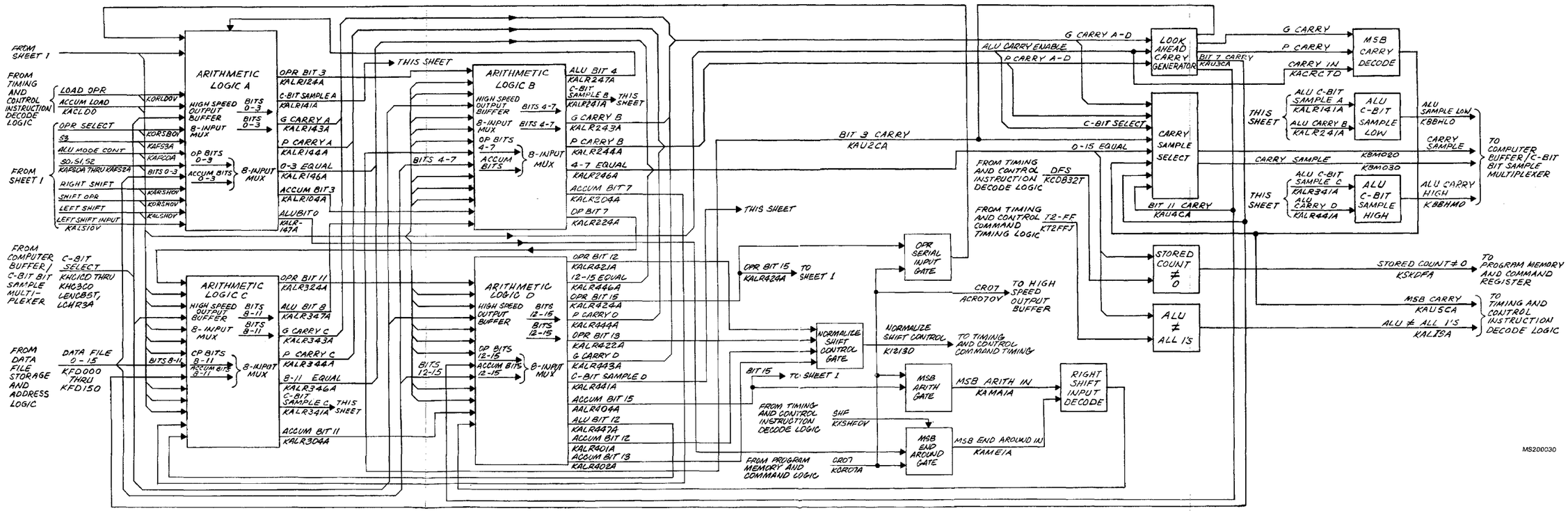


Figure 5-28. Arithmetic Logic Block Diagram (Sheet 2 of 2)

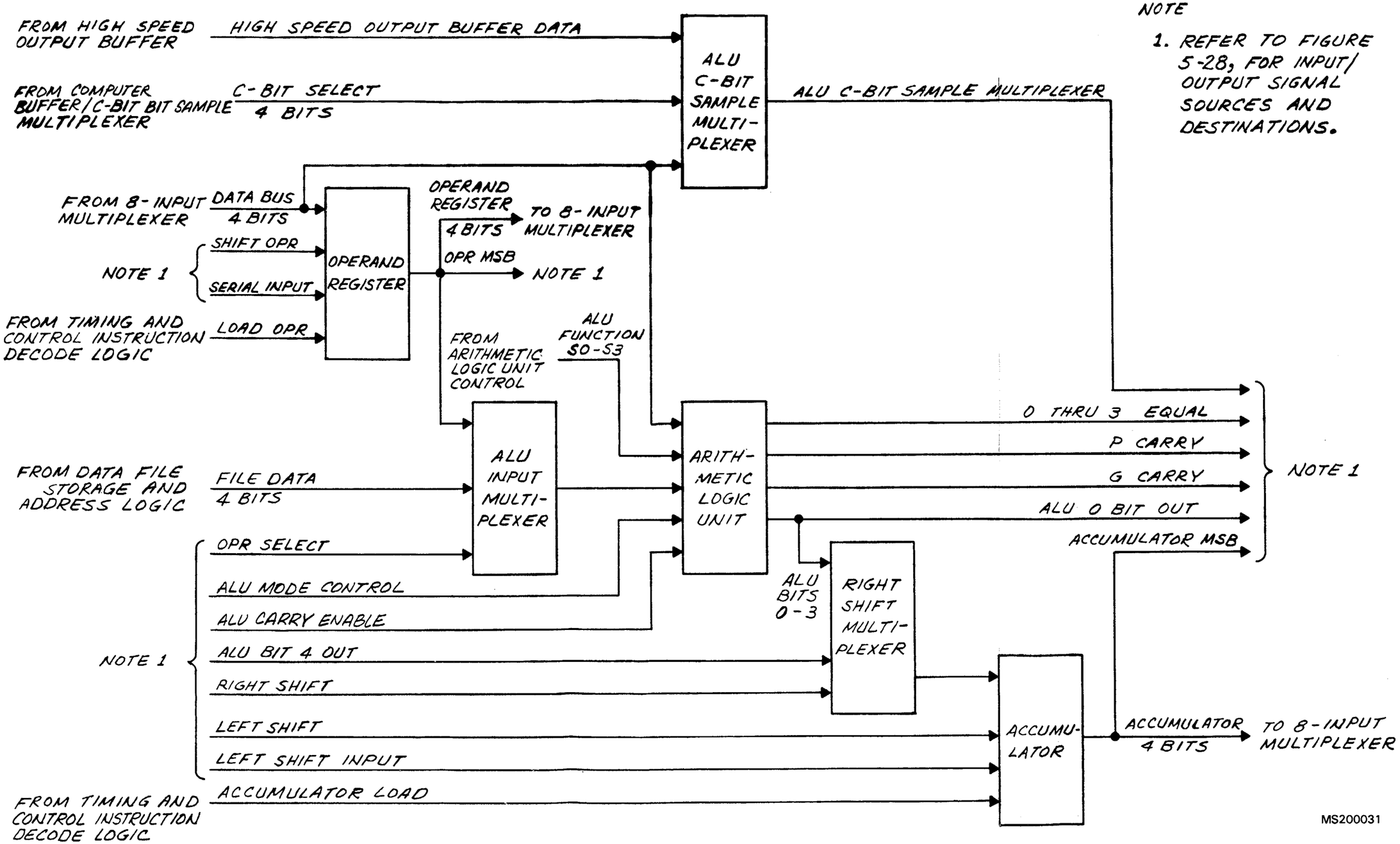


Figure 5-29. Arithmetic Logic A thru D Detailed Block Diagram

Table 5-19. ALU Control Decoding Scheme

Priority encoder	Input	Equation
A	3	SUB + (MCS • $\overline{\text{OR15}}$)
	4	[SHF + CFA + EQS + ESB + ORI + AND + (CBA • $\overline{\text{CR05}}$)]
		[($\overline{\text{CBA}}$ • $\overline{\text{CR05}}$) + CBA]
	5	[ADD + DFS + (MCS • OR15)] • CR14
B	1	[ADD + EQS + (MCS • OR15)] • CR14
	3	AND
	6	ORX + ORI + SUB + $\overline{\text{(OR15}}$ • MCS)
	7	[DFS + CFA + SHF + ($\overline{\text{CBA}}$ + $\overline{\text{CR05}}$[] • [$\overline{\text{CBA}}$ + (CBA • $\overline{\text{CR05}}$)]

Table 5-20. ALU Function Codes

Instruction		Priority Encoder		ALU code						
Oct	Mnemonic	U1	U7	S3	S2	S1	SO	CO	M	ALU function
04	CBA*	$\overline{4}$	$\overline{7}$	H	H	H	H	H	H	A
14	CFA	$\overline{4}$	$\overline{7}$	H	H	H	H	H	H	A
20	AND	$\overline{4}$	$\overline{3}$	H	L	H	H	H	H	A • B
21	ORX	--	$\overline{6}$	L	H	H	L	H	H	A ⊕ B
22	ORI	$\overline{4}$	$\overline{6}$	H	H	H	H	H	H	A + B
23	ESB	$\overline{4}$	--	H	L	L	L	H	H	$\overline{\text{A}}$ + B
24	ADD	$\overline{5}$	$\overline{1}$	H	L	L	H	H	L	A PLUS B
25	SUB	$\overline{3}$	$\overline{6}$	L	H	H	L	L	L	A MINUS B
27	SHF	$\overline{4}$	$\overline{7}$	H	H	H	H	H	H	A
31	MCS (OR15)	$\overline{5}$	$\overline{1}$	H	L	L	H	H	L	A PLUS B
31	$\overline{\text{MCS}}$ (OR15)	$\overline{3}$	$\overline{6}$	L	H	H	L	L	L	A MINUS B
32	DFS	$\overline{5}$	$\overline{7}$	H	H	H	H	H	L	A MINUS 1
34	ESQ	$\overline{4}$	$\overline{1}$	H	L	L	H	H	H	$\overline{\text{A + B}}$
	NONE	--	--	L	L	L	L	H	H	A

*For CR05 = ZERO

Table 5-21. ALU Logic and Arithmetic Operations

Selection					Active - high data M = L: Arithmetic operations	
S3	S2	S1	S0	M = H logic functions	C_n = H (No carry)	C_n = L (With carry)
L	L	L	L	$F = \overline{A}$	F = A	F = A PLUS 1
L	L	L	H	$F = \overline{A + B}$	F = A + B	F = (A = B) PLUS 1
L	L	H	L	$F = \overline{A}B$	$F = A + \overline{B}$	$F = (A + B)$ PLUS 1
L	L	H	H	F =0	F = MINUS 1 (2's COMPL)	F = ZERO
L	H	L	L	$F = A\overline{B}$	$F = A \text{ PLUS } A\overline{B}$	$F = A \text{ PLUS } A\overline{B} \text{ PLUS 1}$
L	H	H	L	$F = \overline{B}$	$F = (A = B) \text{ PLUS } A\overline{B}$	$F = (A - B) \text{ PLUS } A\overline{B} \text{ PLUS 1}$
L	H	H	L	F = A + B	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	$F = A\overline{B}$	$F = A\overline{B}$ MINUS 1	$F = A\overline{B}$
H	L	L	L	$F= \overline{A} + B$	F = A PLUS AB	F A PLUS AB PLUS 1
H	L	L	H	$F = \overline{A + B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	$F = (A + \overline{B}) \text{ PLUS } AB$	$F = (A + \overline{B}) \text{ PLUS } AB \text{ PLUS 1}$
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	$F = A + \overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A+B) PLUS A	$F = (A + \overline{B}) \text{ PLUS A PLUS 1}$
H	H	H	H	F = A	F = A MINUS 1	F = A

d. The look-ahead carry generator provides synchronous carry generation for the four ALU stages (during a subtraction operation, the borrow bit is generated). The carry bit is generated by comparing the carry-in bit (ALU carry enable) and the propagate (P carry) and generate (G carry) bits from all four stages and developing carry overflow indications in accordance with table 5-22. The carry bits for the second, third, and fourth stages are provided on the carry bit 3, 7, and 11 lines, respectively. The MSB carry bit is utilized in the instruction decode logic during an MCS instruction to indicate absolute magnitude comparison.

e. The bit 0-15 equal outputs from the four ALU circuits are used for the DFS, ESB, and EQS instruc- tions. The DFS instruction is utilized to clear a file memory location. This is accomplished by decrementing the file information by one until the remainder is all ZEROS, as indicated by a low signal on the stored count ≠ 0 output line. The ALU ≠ all 1's output is utilized in the instruction decode logic to check for bit or word equality during an ESB or EQS instruction.

5-19. Data File Storage and Address Detailed Description (fig. 5-30, FO-17)The data file storage and address logic consists of the following elements:

Index counter/register
Index function enable
File address adder
Constant file 128-255 enable
RAM select decoder
Constant file address decoder
C-BIT sample mux
Scratchpad
Constant file 16 X 256
File data gating

The data file addressing scheme is controlled by the states of the BST instruction, the CR09 (indexing) bit, and the CR07 bit. The BST instruction requires that the current program address be stored in scratchpad file location 0. Therefore, this instruction forces an all ZERO scratch- pad file address. For other than a BST instruction, the addressing scheme is dependent upon the state of the CR09 indexing bit. When this bit is a ZERO, the 8 LSBs

Table 5-22. Look-Ahead Carry Generator Truth Table

Inputs									Outputs				
Cn	G0	P0	G1	P1	G2	P2	G3	P3	C0	C1	C2	G	P
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	H	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					H		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

X = Irrelevant

of the command register are used directly to address the data file. When this bit is a ONE, the content of the index counter/register is added to the command register address to produce the file address. The CR07 bit determines which portion of the file is addressed; a CR07 ONE addresses the constant PROM portion while a CR07 ZERO addresses the scratchpad RAM portion.

a. *Index Counter/Register.* The index counter/ register is an eight-stage binary down counter that is mechanized to sequentially decrement for a DIS instruction. For a copy into index instruction (CBI or CFI), the index counter load signal stores the 8 LSBs from the data bus in the index counter/register.

b. *Data File Addressing.* Data file addressing is mechanized by the eight-stage index counter and two 4-bit arithmetic logic units which comprise the file address adder. The required addressing scheme is determined by the function code to the file address adder, which is in turn determined by the states of the BST and CR09 inputs, as follows:

ALU function input	Logic state
S0	Hold high
S1 and M	High for $\underline{BST} + \overline{CR09}$
	Low for $\underline{BST} \bullet CR09$
S2	High for $\overline{BST} \bullet CR09$
	Low for $BST + CR09$
S3	High for $\overline{BST}$
	Low for BST

Therefore, the decoder function inputs to the file address adder are:

	ALU function inputs				
Equation	S3	S2	S1	S0	ALU function
$BST \bullet CR09$	0	0	1	1	Logic 0
$\underline{BST} \bullet \overline{CR09}$	0	0	1	1	Logic 0
$\overline{BST} \bullet CR09$	1	0	0	1	A plus B
$\overline{BST} \bullet \overline{CR09}$	1	1	1	1	A

The above equations demonstrate that the BST instruction forces an all ZERO address. Combined with an active indexing bit, the BST instruction results in addition of the index counter/register and command register 8 LSBs, while the BST * CR09 simply applies the command register bits to the data file address lines.

c. *Constant File Addressing.* The constant file is a 256-word x 1 6-bit PROM, comprising eight 51 2-bit memory locations. For each address, two PROMs are selected, each to output one of sixty-four 8-bit bytes, constituting the 16-bit stored data word. A ONE in the CR07 bit enables the constant file address decoder. The carry bit from the file address adder is combined with the index function enable to determine whether the upper half (0-127) or the lower half (128-255) of the constant file is being addressed. Thus, the upper half of the constant file can only be accessed when the index option is selected $(\overline{BST} \bullet CR09)$. The four-line output from the constant file address decoder thus selects two of the eight PROMs. The 6 LSBs from the file address adder select one of the 64 constant file words.

d. *Scratchpad File Addressing.* When the CR07 bit is a ZERO, constant file addressing is disabled and scratchpad file addressing is enabled. The scratchpad file is mounted upon two PCBs, each containing eight 64-bit bipolar RAM chips. The 4 MSBs from the file address adder are combined in the RAM select decoder to select four of eight chips on one of the two PCBs. The 4 LSBs select one of the four 16-bit word locations. Writing into the scratchpad file is enabled by the file write enable from the instruction decode logic. At all other times, the selected file word is supplied to the file data gating. The file data gating routes the selected data file word to the 8-input mux and the computer buffer/C-BIT BIT sample mux.

5-20. 8-Input Multiplexer Detailed Description (fig. 5-31, FO-18). The 8-input mux is used to route data information from one of seven sources to the data bus. The data bus supplies the selected information word in parallel to eight destination registers. The source and destination is determined by decoding the current command word. Sixteen 8-input muxs provide the switching function to the data bus. A 3-bit binary code from the data bus select logic determines which one of the eight inputs for each mux is selected. The significance of the eight sets of input data is described in table 5-23. Figure 5-32 illustrates the DC data transmission paths, the input and outputs to and from the 8-input mux, and the 3-bit bus select code. The 3-bit bus select code is defined in paragraph 5-25. The data bus distributes the selected information to the arithmetic logic unit, operand register, index register, data file, program address counter, and high speed output register. The data to the arithmetic logic unit and high speed output register is active high while all other destinations receive active low data.

5-21. Program Memory and Command Register Detailed Description (fig. 5-33, FO-19). The program memory and command register consists of the following elements:

Count gate
Load gate
Program address counter
Program address decoder
Display memory
Command input mux
Command register
DC test breakpoint
OP code Is digit

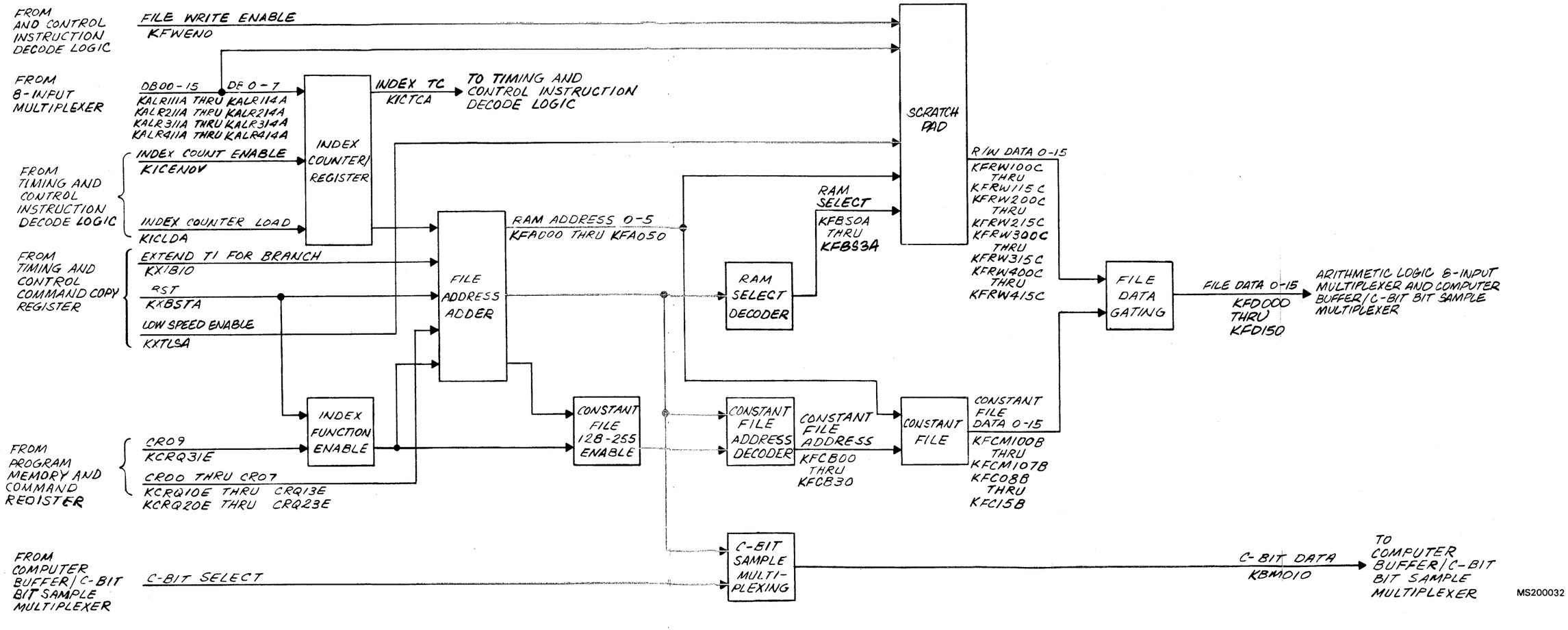
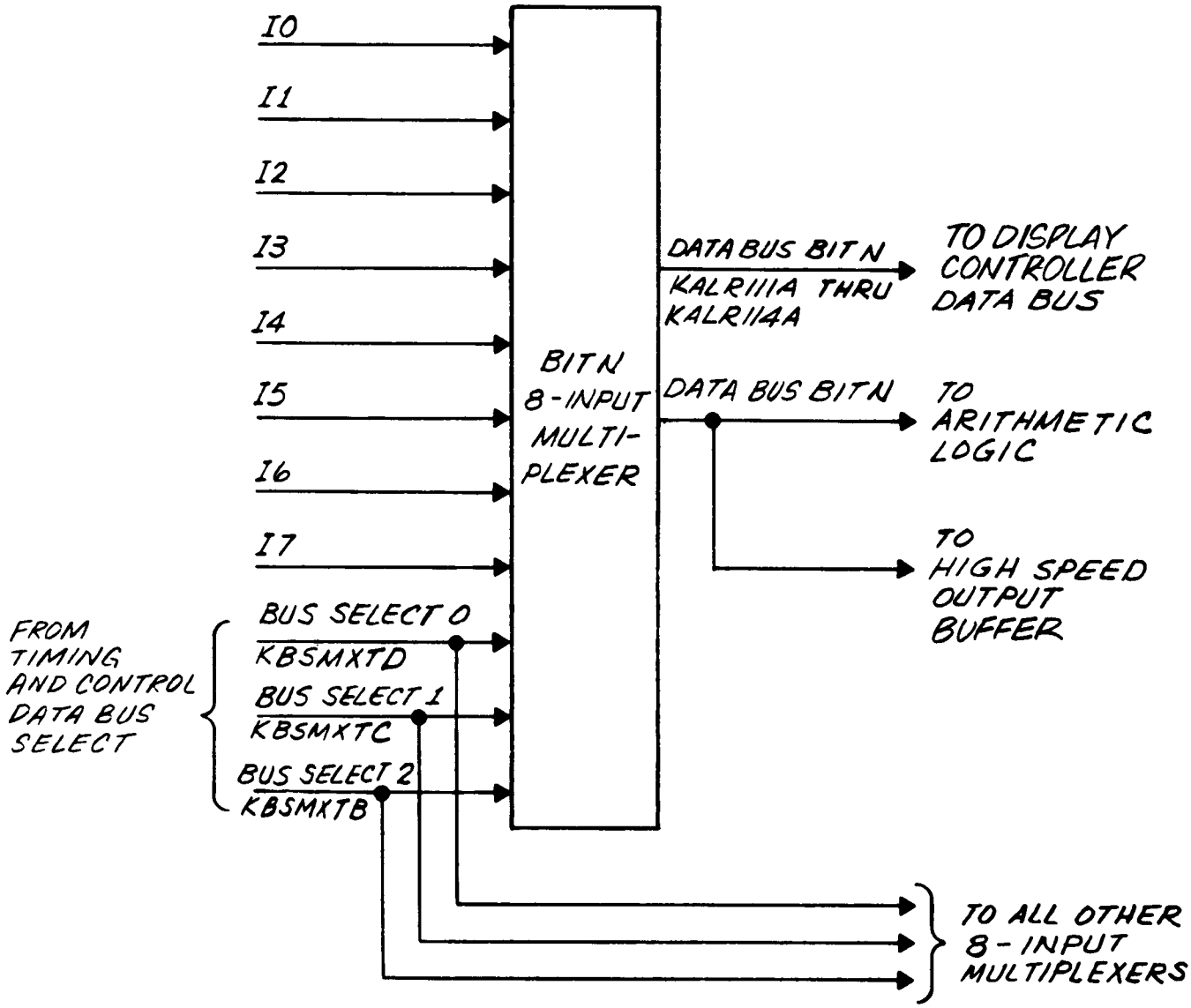


Figure 5-30. Data File Storage and Address Block Diagram



NOTE: INPUTS I0 THRU I7 ARE DESCRIBED IN TABLE 5-23.

Figure 5-31. 8-Input Multiplexer

Table 5-23. 8-Input Multiplexer Input Data Description

Input	N - bits	Signal Name	Mnemonic	Source
I0	0-15	ACCUM 0-15	KALRΔΔΔA	Arithmetic logic
I1	0-15	OPAND 0-15	KALRΔΔΔA	Arithmetic logic
I2	0	LOGIC 0	KDOCOCAV	
	1-2	No connection		
	3-13	COS 0-10	KSDPΔΔE	Serial-to-parallel buffer
	14	COS SIGN	KSDP33E	
	15	DATA STROBE	KSPCSJ	
I3	0-15	DB DATA 0-15	KDBOΔΔE	Display buffer read write memory and output register
I4	0-15	FILE DATA 0-15	KFDΔΔO	Data file storage and address logic
I5	0-9	CMD REG 0-9	KCRΔΔΔΔ	Program memory and command register
	12-15	12-15	KCRΔΔΔV	
	10,11	CMD REG 10,11		Command copy register
I6	0-9	A0-A9	KPACΔΔV	Program memory and command register
	10-15	No connection		
17	0	Logic 0	KDCOEAV	
	1-2	No connection		
	3-13	SIN 0-10	KSDPΔΔE	Serial-to-parallel buffer
	14	SIN SIGN	KSDPG3E	
	15	DATA STROBE	KSPCSJ	

NOTE: Δ indicates multiline mnemonic (0-15, A thru D, etc)

Transfer high decode
Copy file gate

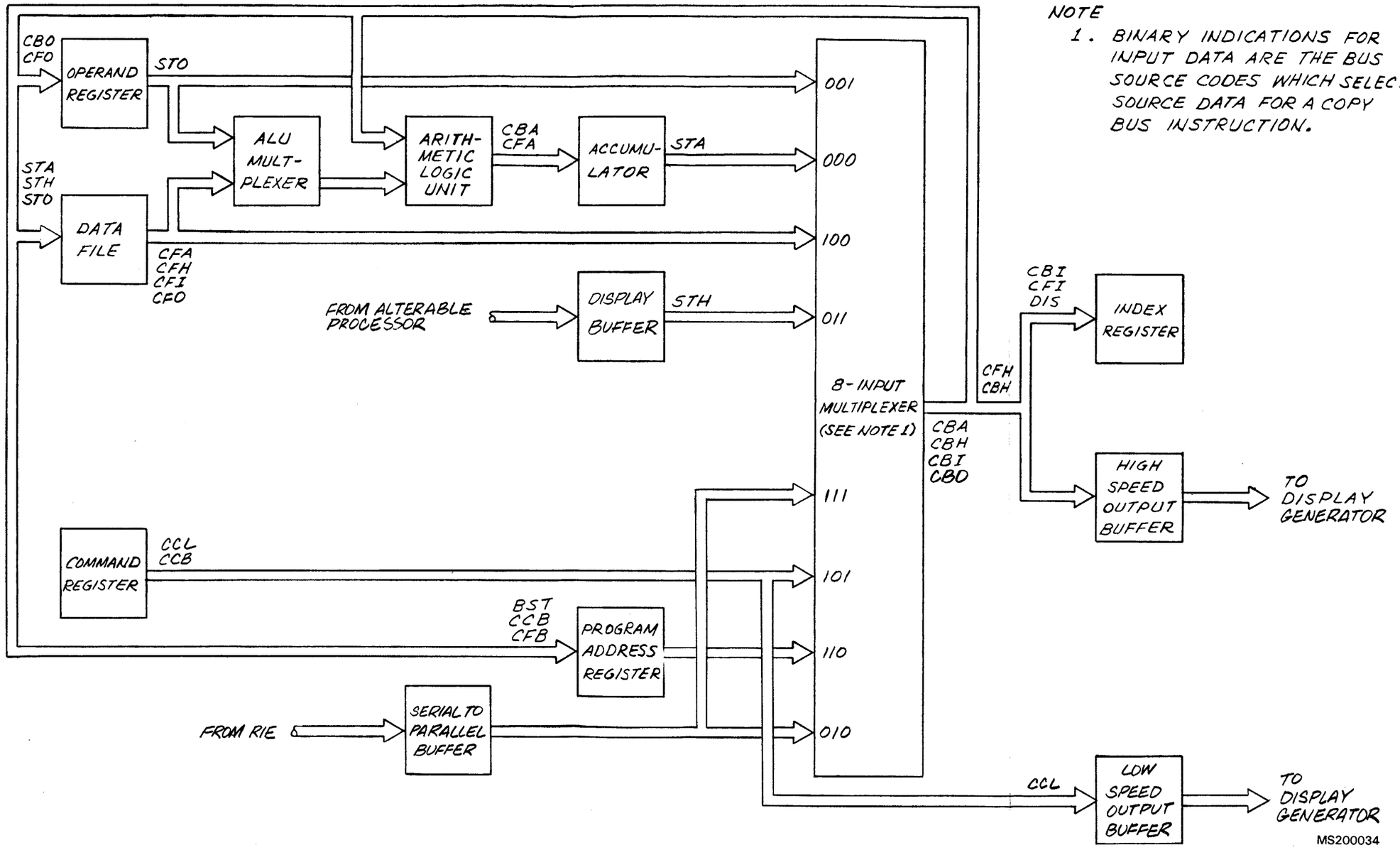
The program memory and command register provides the addressing, permanent storage, and temporary output storage for the command words. The command word storage is provided by a 1024 word X 16-bit PROM containing a repertoire of 30 preselected instructions. The particular instruction is determined by decoding bits 10 thru 14 of the command word as illustrated in table 5-24. Bit 15 is used during maintenance.

a. A 10-bit program address counter is utilized to select 1 of the 1024 instructions stored in the display memory. When the display console is initialized, the counter is cleared to all ZEROS. The counter can then be incremented by each advance command to sequentially address each of the 1024 storage locations. Branch instructions (CFB, CCB, and BST) require that the program address counter be branched to a new starting address. The presence of any one of these instructions generates the load signal at T1 valid time. The program address counter is then loaded with the 10 LSBs currently on the data bus. The program address counter is also incremented by any one of several skip routines or by the external signal, stored count ≠ 0. These instructions permit the program address counter to be incremented during an instruction cycle as well as at the end.

b. The program memory comprises two bipolar read/write memory PCBs, each capable of storing 512 8-bit bytes. Each board contains eight 512-bit bipolar PROM chips. The 5 LSBs of the program address counter are utilized to binarily select one of the sixty-four 8-bit bytes stored.

c. Program address bits 6 thru 8 are decoded to provide a unary modulo 64 signal which selects one of the eight PROM chips. The command input mux selects between the stored command word or a test word from the computer buffer/C-BIT logic. The output from the command input mux is loaded into the command register by the advance command signal. The command information from the command input mux and the command register is distributed to various DC logic for decoding and control signal applications.

d. Some initial decoding (transfer high speed required and copy file) is performed by the program



NOTE

1. BINARY INDICATIONS FOR INPUT DATA ARE THE BUS SOURCE CODES WHICH SELECT SOURCE DATA FOR A COPY BUS INSTRUCTION.

Figure 5-32. Display Controller Data Transmission Paths

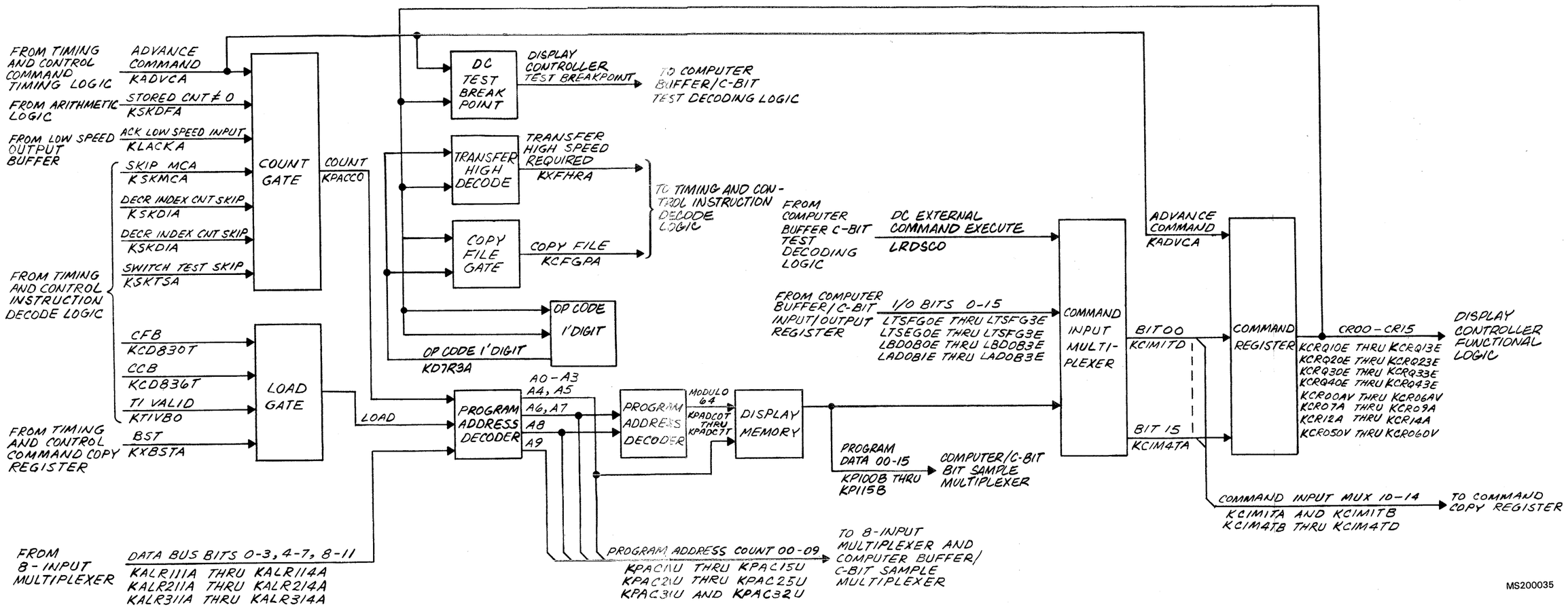


Figure 5-33. Program Memory and Command Register Block Diagram

Table 5-24. Instruction Decoding

	Command word bits							
Octal	15	14	13	12	11	10	Mnemonic	Instruction
00		0	0	0	0	0	SWS	Set sense switch
01		0	0	0	0	1	RSW	Reset sense switch
02		0	0	0	1	0	TSS	Test sense switch
03		0	0	0	1	1	CBI	Copy bus into index
04		0	0	1	0	0	CBA	Copy bus into accumulator
05		0	0	1	0	1	CBO	Copy but into operand
07		0	0	1	1	1	CBH	Copy bus into high speed
10		0	1	0	0	0	STA	Store accumulator
11		0	1	0	0	1	STO	Store operand
12		0	1	0	1	0	CCL	Copy command register to low speed
13		0	1	0	1	1	STH	Store high speed
14		0	1	1	0	0	CFA	Copy file to accumulator
15		0	1	1	0	1	CFO	Copy file to operand
17		0	1	1	1	1	CFH	Copy file to high speed
20		1	0	0	0	0	AND	AND
21		1	0	0	0	1	ORX	Exclusive OR
22		1	0	0	1	0	ORI	Inclusive OR
23		1	0	0	1	1	ESB	Examine selected bits
24		1	0	1	0	0	ADD	Add
25		1	0	1	0	1	SUB	Subtract
26		1	0	1	1	0	TXS OR TXH	Skip or hang
27		1	0	1	1	1	SHF OR NRM	Shift or normalize
30		1	1	0	0	0	CFB	Copy file and branch
31		1	1	0	0	1	MCS	Magnitude compare-skip
32		1	1	0	1	0	DFS	Decrement file-skip
33		1	1	0	1	1	CFI	Copy file into index
34		1	1	1	0	0	ESQ	Equality-skip
35		1	1	1	0	1	DIS	Decrement index and skip
36		1	1	1	1	0	CCB	Copy command register and branch
37		1	1	1	1	1	BST	Branch and store

memory and the command register logic. The equation ([CR10·CR11] + CR12) $\overline{CR13}\cdot\overline{CR14}$ defines the copy bus instructions 03, 04, 05, and 07 (see table 5-24). When source code bits CR07 thru CR09 are 110 (indicating the high speed output buffer), the transfer high speed required signal is generated. The source code bits are defined in paragraph 5-25. The equation CR12·CR13·CR14 defines copy file instructions 14, 15, and 17. Thus a CFA, CFO, or CFH instruction develops the copy file signal.

5-22. High Speed Output Buffer Detailed Description (fig. 5-34, FO-20). The high speed output buffer consists of the following elements:

Output buffer
Data driver
Character space control

The high speed output buffer provides temporary storage for high speed data (ASCII and symbol codes) being transmitted to the DG. High speed data transmission is initiated by a load signal from timing and control instruction decode. This load signal loads the information currently on the data bus into the output buffer. The output buffer then sends the 15 bits of high speed data to the data driver for transfer to the DG. The 15 bits of high speed data is also sent to the arithmetic logic which, when selected, is monitored by the computer buffer/C-BIT. The character space control monitors high speed data bits 8 thru 14 for ASCII code blanks. It also sends a character space control signal to the low speed output buffer, inhibiting the start of a character. The low speed output buffer sends a sweep intensity compensation signal to the data driver for control of bit 0 which allows the display generator to turn up the crt intensity.

5-23. Serial-to-Parallel Buffer Detailed Description (fig. 5-35, FO-21). The serial-to-parallel buffer consists of the following elements:

Receiver and driver circuit
Data strobe flip-flop
Serial buffer
Parallel buffer

The main function of the serial-to-parallel buffer is to receive serial radar sin/cosine position data from the RIE and convert the data to parallel form for transfer to the 8-input mux. The RIE sends 12 bits of sin and 12 bits of cosine radar data to the receiver and driver circuit for signal conditioning which is then clocked into the serial buffer. After the 24th bit has been clocked, in the RIE sweep data strobe enables the parallel buffer to allow a parallel transfer of sin/cosine sweep data. The sin/cosine data bits contained in the parallel buffer are now available to the 8-input mux. Since the data is radar sweep positional information, the data is constantly changing and always indicates the direction the radar antenna is pointing. The sweep data strobe is sent to the 8-input mux from the data strobe flip-flop which is reset after each data strobe.

5-24. Low Speed Output Buffer Detailed Description (fig. 5-36, FO-22). The low speed output buffer consists of the following elements:

Data least significant select
Low speed enable circuit
Data most significant select
Enable code gate
Start bit 0-3 circuit
Enable flip-flop
Output register
Output external code bits
Start of character set
Start of character flip-flop
Code strobe flip-flop
Video strobe circuit
Early deflection active circuit
Sweep intensity compensation gate
Driver circuit

The low speed output buffer provides control signals to the DG which identify the data being sent from the high speed output buffer. The CCL instruction (CR12 active) selects utility field data bits from the program memory and command register for distribution to the low speed output buffer circuitry. Upon receiving a low speed enable signal from the command copy register, the low speed enable circuit sends an active low speed enable signal to the enable flip-flop. The signal sets the enable flip-flop which allows the driver circuit to output the control signals and video strobe to the DG. On the next clock pulse, the low speed enable circuit resets the enable flip-flop which allows the external code bits (DG decoder functions) to be sent to the DG. The DC control channel output functions are shown in table 5-25 and the DG decoder functions are shown in table 5-26. The output register, start of character (SOC), and code strobe flip-flops are used to control the length of time the control signals are made available to the DG. Upon receiving a power on demand signal from the output register, the early deflection active circuit sends a deflection active to the sense switch logic. The early deflection active circuit is used to keep the DC active before the deflection amplifier has settled the beam. The sweep intensity compensation gate, upon receiving a compressor video signal from the range mark and azimuth generator and code bits representing a 010, supplies a sweep intensity compensation signal to the high speed output buffer. This signal is used by the DG to increase the crt intensity. The SOC is temporarily inhibited by a character space control signal from the high speed output buffer. The character space control signal represents an ASCII code 20 which allows a space between characters.

5-25. Timing and Control Detailed Description (fig. 5-37). Timing and control consists of the following elements:

Command copy register
Command timing logic
Sense switch logic

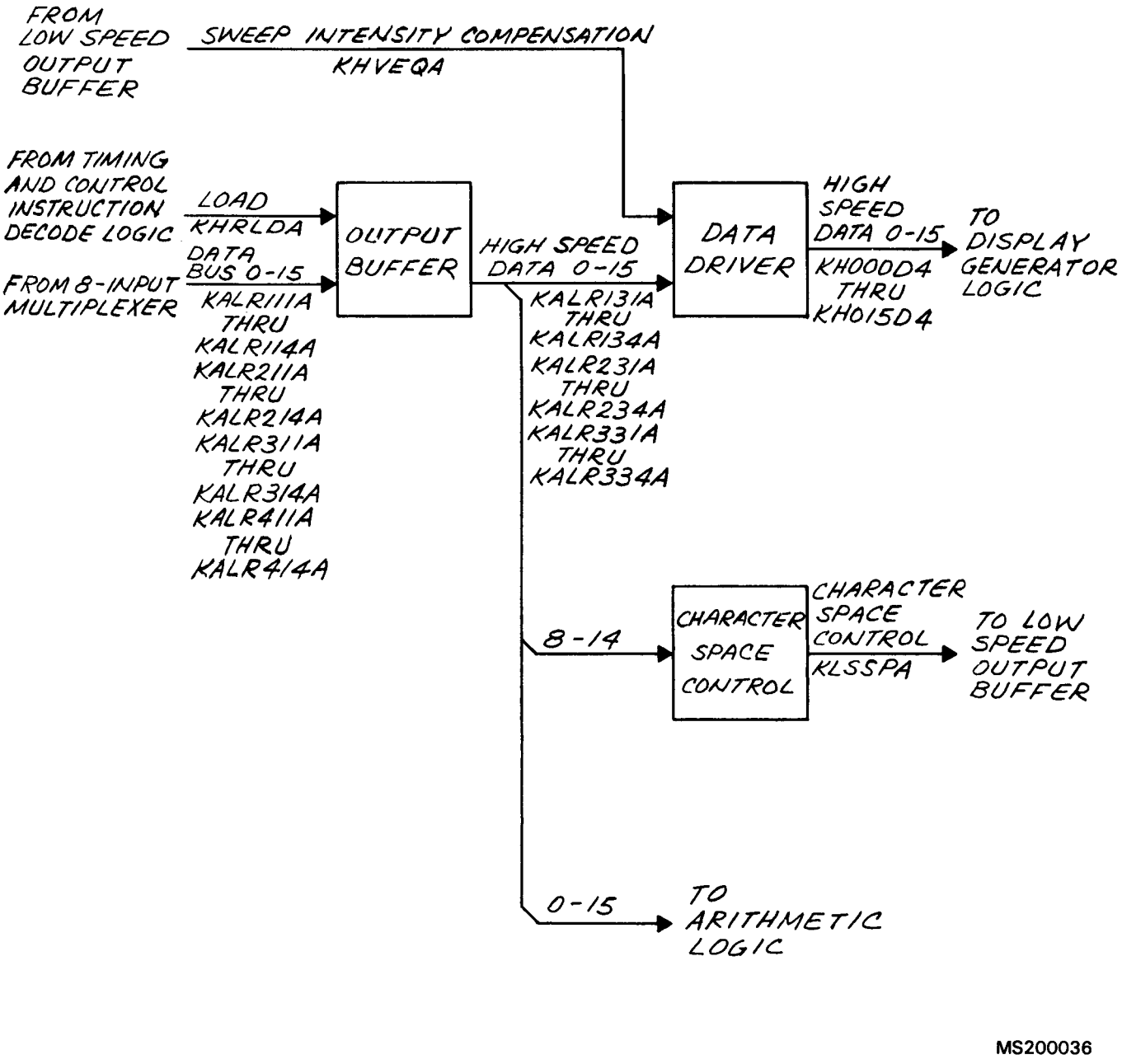


Figure 5-34. High Speed Output Buffer Block Diagram

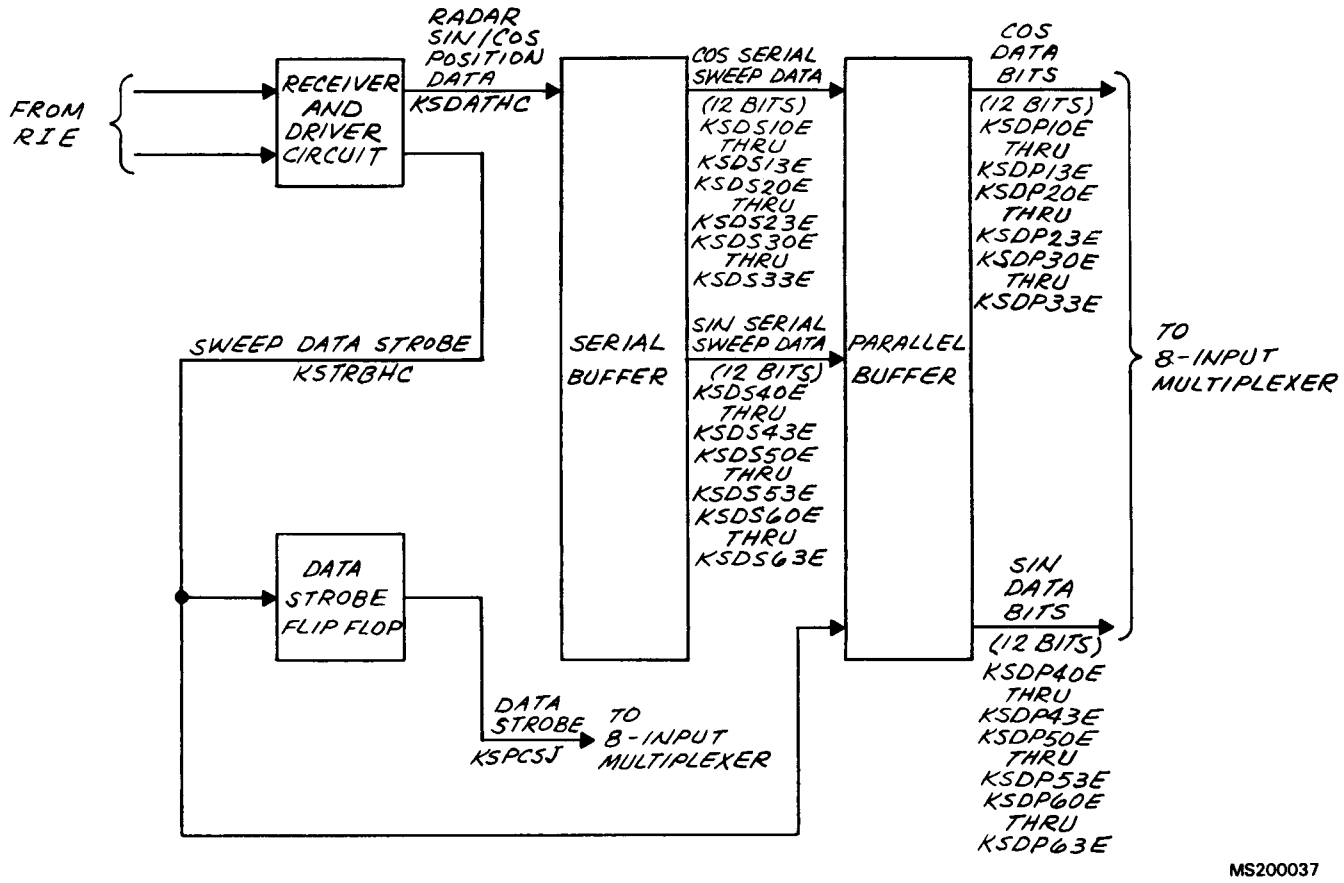


Figure 5-35. Serial-to-Parallel Buffer Block Diagram

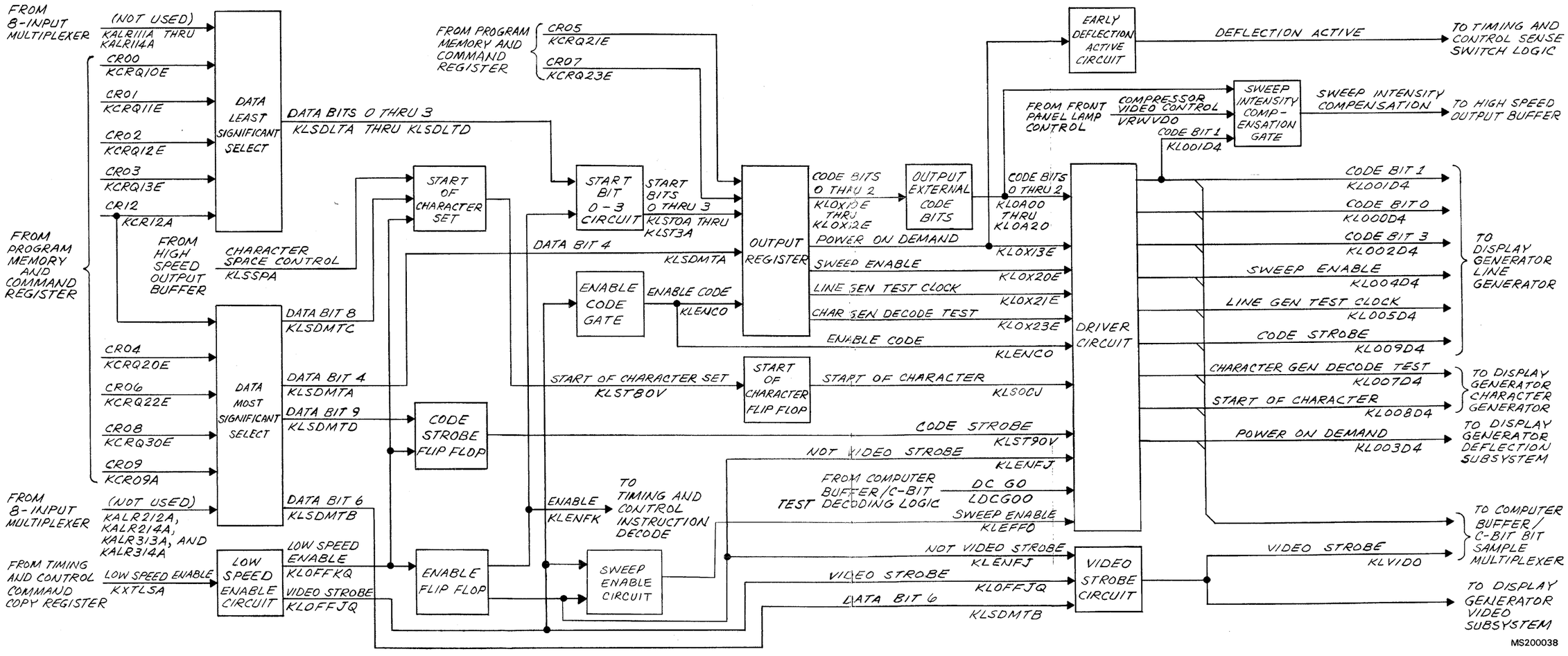


Figure 5-36. Low Speed Output Buffer Block Diagram

Table 5-25. DC Control Channel Output Functions

Signal	Function
KL000D4	Bit 0 command data to 1-of-8 (refer to table 5-26)
KL001D4	Bit 1 (refer to table 5-26)
KL002D4	Bit 2 (refer to table 5-26)
KL003D4	Deflection amplifier power-on-demand enable
KL004D4	Sweep enable strobe
KL005D4	Line generator test clock (GBIT control only)
KL007D4	Character generator decode test (GBIT control only)
KL008D4	SOC pulse
KL009D4	Center section decoder strobe (refer to table 5-26)

Table 5-26. DG Decoder Functions

Strobe	Bit 2	Bit 1	Bit 0	Function
1	*	*	*	No action
0	0	0	0	Load range/rate registers
0	0	0	1	Start-of-line (SOL) pulse
0	0	1	0	Load X register
0	0	1	1	Load Y register
0	1	0	0	Load length counter
0	1	0	1	SOC
0	1	1	0	Load X position counter
0	1	1	1	Load Y position counter

*Don't care

Instruction decode logic
Data bus select logic

Timing and control decodes the current command word to provide the various timing and control signals required by the DC to process the current instruction. Command word decoding is controlled by the advance command which indicates the termination of a current instruction cycle and the beginning of a new instruction cycle. The advance command signal instructs the program memory and command register to load the next instruction. The op code and utility field for this next instruction are supplied to timing and control. The advance command also loads the 5-bit op code into the command copy register. The command copy register provides supplementary storage for the op code in addition to supplementary instruction decoding (BST, CCL, CCB, and CBA). The command copy register also enables the low speed output buffer. The instruction decode logic is used for primary command word decoding and provides indications of the current instruction. Table 5-27 defines the command word utility field by instruction and op code. The instruction decode logic combines the indications with pertinent utility field bits and generates the control levels required to ensure that the proper data is processed in the proper sequence. The instruction decode logic also provides the majority of control signals required by the DC to transfer and manipulate data. The instruction decode logic, in conjunction with the command timing logic, generates phase T1, T2, and extend signals which permit the DC the discrete times required to process an instruction and to extend those times dependent upon the complexity of the instruction. The source for data derived from the data bus is dependent upon the actual instruction and, in some cases, the contents of the utility field. The data bus select logic utilizes the decoded instruction information and pertinent utility field bits to select one of eight potential data bus sources. Table 5-28 defines the eight data bus source codes. The sense switch logic, under control of the SSW and RSW instructions, stores various DC internal and external status indications and supplies these indications for testing by the TSS instruction. The sense switch logic also monitors the status of data transfer from the DB, VC, and DG.

a. *Command Copy Register (fig. 5-38, FO-23).* The command copy register provides supplementary storage for the 5-bit command word operational code and additional decoding for instructions. The 5-bit operational code is loaded into the command copy register from the same source and by the same advance command as for the command register. The outputs from the command copy register provide additional loading for the various decoding logic in the DC. Refer to table 5-24 for the significance of the various operational codes. Operational codes CCR10, CCR11, CR12, CR13, and CR14 enable the BST decode. When the MSB of the utility field (CR09) is a ZERO, the extend T1 for branch signal is supplied to the data file storage and address and instruction decode logic. Operational codes CCR10, CCR11, CR13, CR14, and the advance unless necessary signal define the CBA instruction and develop a control signal to the arithmetic logic. Operational codes CCR11, CR12, CR13, and CR14 define both the CCB and the BST instructions. However, the priority logic in the data bus select logic will utilize this CCB output only if the BST is inactive. Operational codes CCR10, CCR11, CR13, and CR14 define the CCL instruction and supply a low speed enable signal to the low speed output buffer for transfer of control signals to the DG. The low speed enable signal also enables program data file storage scratchpad write operation.

b. *Command Timing (fig. 5-39, FO-24).* Command timing generates the phase T1 and T2 control signal and extends these operation times to accommodate the current instruction. The operation of the command timing logic is dependent upon the number of operations or clock times required to implement the particular instruction. There are two basic phases: T1 and T2. Each can be extended for one additional clock time by the extend circuit. In addition, for more time-consuming instructions, an extend counter is provided to extend phase T2 by a predetermined number of clock times.

(1) Simple instructions (SSW, RSW, STA, and STO) require only phase T1. Phase T2 is utilized for more complex instructions such as NRM, SHF, or BST. The extend circuit is utilized for phase T1 and/or phase T2 primarily to permit memory address settling time when information is read from the data file. The extend counter is utilized to count the number of accumulator or operand shifts.

(2) Phase T1 and T2 timing states are illustrated in figure 5-40. Phase T1 and T2 generation logic is a free-running loop with the extend options determined by control signals from the instruction decode logic. When an instruction is completed, the advance command gate is enabled. The resultant advance command signal sets the T1 circuit and resets the T2 circuit, if required. The advance command signal to the program memory and command register increments the program address counter and loads the new command into the command register. The advance command signal is also distributed to various DC logic, indicating that a new instruction is about to be processed. As long as the current instruction is a single-step instruction and no extensions are required, the advance from the T1 signal again generates an advance command signal, and the DC proceeds to the next addressed command.

(3) Examination of the current instruction and its accompanying utility field by the instruction decode logic may dictate that phase T1 must be extended by one clock time. This is indicated by the extend T1 signal which sets the extend circuit. The extend T1 signal also inhibits the advance from T input, blocking the advance command and the T1 valid input, maintaining the phase counter in the T1 phase. The T1 not extended output now goes inactive and permits the program memory and command

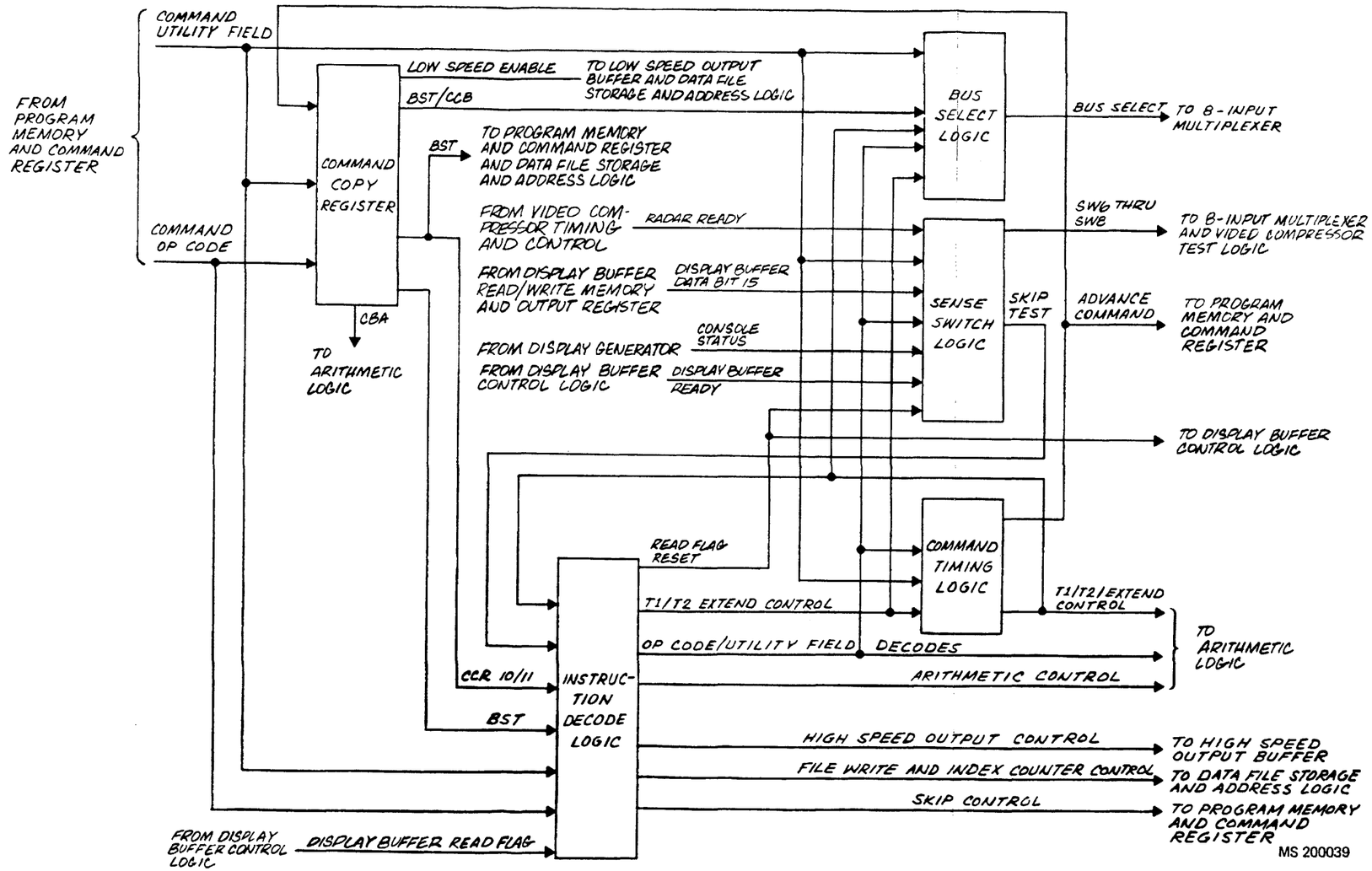


Figure 5-37. Timing and Control Block Diagram

Table 5-27. Command Set Description

OP code	Inst.	Command word utility field										Command description
		Index Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
00	SSW	(SW9)	SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW1	SW0	Set sense switches 0 thru 9. If bit is "1 ", corresponding switch is set.
01	RSW	(SW9)	SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW1	SW0	Reset sense switches 0 thru 9. If bit is "1", corresponding switch is reset.
02	TSS	(SW9)	SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW1	SW0	Test sense switch. Skip next instruction if any selected sense switch is not set.
03	CBI	SOURCE REG MSB	SOURCE REG 2 LSB	SOURCE REG LSB								Load 8 LSB contents of bus into index register. Bits 7 thru 9 specify source register to bus.
04	CBA	SOURCE	SOURCE	SOURCE		INVERT N OPTION						Load contents of bus into accumulator. Bits 7 thru 9 specify source register.
05	CBO	SOURCE	SOURCE	SOURCE								Load contents of bus into operand register. Bits 7 thru 9 specify source register.
06	Not used											
07	CBH	SOURCE REG MSB	SOURCE REG 2 LSB	SOURCE REG LSB								Copy bus to high speed interface output bits 7 thru 9. Specify source register.

Table 5-27. Command Set Description - Continued

OP code	Inst.	Command word utility field										Command description
		Index Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
10	STA	INDEX	Not used	MSB			FILE ADDRESS				LSB	Contents of accumulator is copied into file. File address may be modified by contents of index register.
11	STO	INDEX	Not used	MSB			FILE ADDRESS				LSB	Contents of operand register is copied into file. File address may be modified by contents of index register.
12	CCL	MSB	Not used	MSB			DC CONTROL CHANNEL INFORMATION				LSB	Contents of command register to low speed interface utility field contains control channel information.
13	STH	INDEX	Not used	MSB			FILE ADDRESS				LSB	Contents of high speed input register are copied into file. File address may be modified by contents of index register.
14	CFA	INDEX	Not used	MSB			FILE ADDRESS				LSB	Contents of file are copied into accumulator.
15	CFO	INDEX	Not used	MSB			FILE ADDRESS				LSB	Contents of file are copied into operand register..
16	Not used											
17	CFH	INDEX	Not used	MSB			FILE ADDRESS				LSB	Contents of file are copied into high speed output buffer.
20	AND	INDEX	1 = oprnd 0 = ACC				FILE ADDRESS					File is logically ANDed with contents of accumulator or operand register and result is stored in accumulator.
21	ORX	INDEX	1 = oprnd 0 = ACC				FILE ADDRESS					File is exclusive Ored with contents of accumulator or operand register and result is stored in accumulator.

Table 5-27. Command Set Description - Continued

OP code	Inst.	Command word utility field: Index Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Command description
22	ORI	INDEX	1 = oprnd 0 = ACC	FILE ADDRESS								File in inclusive Ored with contents of accumulator or operand register and result is stored in accumulator.
23	ESB	INDEX	1 = oprnd 0 = ACC	FILE ADDRESS								Contents of file are compared to ACC or operand register. Skip if bit in file is 0 corresponding to a "1" bit in ACC or operand.
24	ADD	INDEX	1 = oprnd 0 = ACC	FILE ADDRESS								File is added to contents of accumulator or operand and results are stored in accumulator.
25	SUB	INDEX	1 = oprnd	FILE ADDRESS								File is subtracted from contents of accumulator or operand register and result is stored in accumulator.
26	TXS OR TXH	(SW9)	SW8	SW7	SW6	SW5	SW4	SW3	SW2	Not used	0 = skip 1 = hang	For TXS, skip next instruction if sense switches 0 thru 9 are not set and bit 0 = 0. For TXH, hang next instruction if sense switches 0 thru 9 are set and bit 0 = 1.
27	SHF OR NRM	Not used	1 = norm-alize 0 = shift	1 = arith 0 = end around	Oprnd left	ACC left	ACC right (SHF only)	MSB	No. of shifts 1 less than number of positions through which data is shifted.		LSB	For SHF, content of register is shifted as specified by bits 4 thru 7. The number of places the data is to be shifted is specified in bits 0 thru 3. For NRM, content Of register is shifted as specified by bits 5 thru 8. The number of places the data is to be shifted is specified in bits 0 thru 3.
30	CFB	INDEX	Not used	MSB	FILE ADDRESS						LSB	Copy 10 LSBs of file into program add register and branch.
31	MCS	INDEX	Not used	MSB	FILE ADDRESS						LSB	Absolute magnitude compare of operand and contents of file. The next instruction is skipped if ABS value of operand ≤ file number (which must be POS).

Table 5-27. Command Set Description - Continued

OP code	Inst.	Command word utility field										Command description
		Index Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
32	DFS	INDEX	Not used	MSB ← FILE ADDRESS →							LSB	Decrement contents of file by 1 and skip next instruction if contents were 0
33	CFI	INDEX	Not used	MSB ← FILE ADDRESS →							LSB	Copy 8 LSB contents of file into index register.
34	EQS	INDEX	1 = Oprnd 0 = ACC	MSB ← FILE ADDRESS →							LSB	Equality of skip. The next instruction in sequence is skipped if the file does not equal operand or accumulator as specified by bit 8.
35	DIS	Not used	NOT USED									Decrement index register and skip next instruction if index register was 0.
36	CCB	MSB ← BRANCH ADDRESS →									LSB	Branch to program location specified by bits 0 thru 9. This is an unconditional branch.
37	BST	MSB ←									LSB	Branch to program location specified in bits 0 thru 9. Store present command register address.

register to access the next instruction. The T1 valid input going active indicates that all phase T1 conditions for the particular instruction have been satisfied. As long as the no advance command signal is generated at this time, the T1 valid signal resets the T1 circuit and sets the T2 circuit, initiating phase T2. Should no further extension be required for the current instruction, the active overflow and T2 FF signals enable the advance from T2 unless extended to generate the advance command signal, initiating a new instruction cycle. A shift command or NRM instruction and T2 FF signal will also enable the advance from T2 unless extended.

Table 5-28. Source Codes

Bit 9	Bit 8	Bit 7	Source register
0	0	0	Accumulator
0	0	1	Operand
0	1	0	Sine
0	1	1	High speed output
1	0	0	Data file
1	0	1	Command register
1	1	0	Program address register
1	1	1	Cos

(4) Several instructions may require the program memory address counter to be advanced, which requires one additional phase T2 clock time for the memory address to settle. This condition is indicated by an active extend T2 necessary signal, which inhibits the command advance signal and sets the extend circuit for one clock time. The escape gate is utilized to reinitialize the T1 and T2 circuits for a lockup in the reset condition at system turnon time.

(5) The extend counter is utilized during an SHF instruction to prolong phase T2. For an SHF instruction, the 4 LSBs (CR00 thru CR03) of the current utility field are routed through the extend counter select. These bits, which determine the number of places that the data will be shifted, are loaded into the extend counter by the T1 valid signal. Actually, the number of shifts generated is the shift count plus one. The counter is then incremented until the overflow signal generates the advance command signal, terminating the instruction cycle.

c. *Sense Switch Logic (fig. 5-41, FO-25).* The sense switch logic stores various DC external and internal status indications. The sense switches operate under control of the SSW, RSW, and TSS instruction to set, reset, and test the switches. The 10-bit utility field in the instruction command words determines which one or combination of sense switches are affected. Sense switch 9 is also controlled by signals from the DB and instruction decode logic.

(1) Each of the sense switches is involved with a specific DC function. The state of the sense switch at any particular time is dependent on the sequence of instructions being processed, the status of the associated information and, in the case of sense switch 9, the status of data transfer between the AP and the DC. The following are brief descriptions of the functions with which the 10 sense switches are involved:

SSW 0 - SKIP if ZERO or hang if ONE
SSW 1 - Remember delta X greater than ZERO
SSW 2 - Remember delta Y greater than ZERO
SSW 3 - Center section busy
SSW 4 - Center section not painting
SSW 5 - Center section deflection not active
SSW 6 - Display buffer input ready
SSW 7 - Sweep lost
SSW 8 - Open
SSW 9 - AP/DC message transfer status

An SSW instruction allows the 10-bit utility field to be routed to the 10 sense switches. A ONE in any one or combination of this field sets the associated sense switch. For an RSW instruction, a ONE in any one or combination of the utility field resets the associated sense switch. Sense switch 9 is also set by display buffer data bit 15 and a read flag reset signal from the instruction decode logic. The signals indicate that the DB is in the read mode and at the start of a new message.

(2) The console status logic stores and monitors, under control of the TXS instruction, the character, line, sweep, and deflection active signals from the DG for distribution to sense switch 2 thru 9 select. When CR 12 is active, sense switch information is transferred and when inactive, console status, radar ready, and DB information is transferred to sense switch sample gating. Sense switch sample gating continuously compares the states of the sense switches or console information with the current utility field. The switch test skip signal goes high when any one of the sense switches is reset or any of the console information signals are active when the corresponding utility field bit is a ONE. This output is utilized by the TSS instruction in the instruction decode logic.

d. *Instruction Decode (fig. 5-42, FO-26).* The instruction decode logic decodes the 5-bit operational code currently stored in the command register to determine which one of 30 instructions will be implemented during the current operation. The decoded instruction is then combined with various DC timing and control signals to ensure that the instruction is performed upon the proper data and in the designed sequence. The significance of the 5-bit operational code and 10-bit

utility field for each instruction is detailed in table 5-27. The significance of the source code bits is indicated in table 5-28. The operational codes are shown octally (00 thru 37) with each associated instruction. The attendant functions of each pertinent bit of the associated utility field is also indicated, in addition to a brief description of the instruction's logic functions. Table 5-27 should be referred to when analyzing each of the instruction decode functions. Command word bit 15 is used for maintenance.

(1) Command register bits 10 thru 14 are combined by a command decoder to develop an active level on one of 30 instruction output lines. The outputs from the decoder are distributed to logic elements in the instruction decode logic and other DC functional logic circuits. The command decoder octal outputs are used for groups of instructions that have common functional logic requirements.

(2) When either SSW or RSW goes active, a signal is supplied from the SSW/RSW gating to the sense switch logic to set or reset the sense switches as selected by the associated utility field. As long as the DC is in a go condition, and the skip test signal is active, a TSS instruction or TXS instruction to the switch test skip gate circuit generates the switch test skip signal which instructs the program memory and command register to skip the next instruction.

(3) Either an active STH instruction or a transfer high-speed required signal from the program memory and command register will result in a transfer high speed signal to the DB for resetting the read flag if T1 is not valid. An active CBH or CFH signal instructs the high speed output buffer to accept a word from the indicated source when a T1 extend and T1 wait condition does not exist. An active CFO or CBO instruction generates a load operand signal from the operand load circuit, which transfers the contents of the designated source into the arithmetic logic operand register at time T1. An active CBI or CFI instruction generates the index counter load signal from the index counter load circuit at time T1.

(4) An active BST to the file write circuit generates a file write enable signal to the data file storage and address logic at time T1. This instructs the data file storage and address logic to write the present command register address into the file and branch to the address specified by the current utility field. The CR12 and CD octal 1X inputs define instructions CFA, CFO, and CFH for which data from the file is stored in the designated register. These inputs also generate a file write enable at time T1. For a DFS instruction, a DFS file write enable signal is generated when command timing supplies an extend FF signal. The decremented file contents are then written back into the addressed file location.

(5) Several conditions will supply the accumulator load signal to the arithmetic logic. An active CBA or CFA will load the accumulator from the designated source at time T1. Instructions 20 thru 25 (octal 2X), 27, and DFS involve accumulator operations. The ESB command allows accumulator comparison; an SHF command with a bit 4 ONE (CR04 active) allows an accumulator shift. Since either of the above conditions prohibit disturbing the accumulator contents, they are used as inhibits to the accumulator load circuit. When the proper conditions are present, the T2 not extended signal generates the accumulator load signal.

(6) The bit/word test skip signal is generated at time T2 by an ESB or EQS instruction when the arithmetic logic indicates other than equality (ALU = ALL 1s) between the data being compared. The skip MCA signal is generated at time T2, during an MCS instruction, when the absolute value of the operand register is equal to or less than (MSB carry high) the value being compared. Some instructions and skip conditions require an extension of the T1 and/or T2 phases to complete. The extend T2 necessary signal is generated whenever a bit/word test skip, skip MCA, or DFS signal occurs.

(7) The STH involves the display buffer which must have a data word output available before the instruction can be implemented. An STH command develops the transfer high speed input. If the display buffer is not prepared to output data, the DB read flag signal inhibits the T1 GO signal and enables the T1 WAIT line. The inactive T1 GO signal prevents the file write enable from being generated. When the DB read flag signal goes inactive, the I/O wait condition is terminated and the instruction is processed.

(8) Various instructions and contingent conditions require that phase T1 be extended. For example, any instruction that involves transfer of information from the data file storage requires additional time for the memory address to settle.

(9) A TSS or TXS instruction directly enables the T1 extend circuit. The T1 extend circuit collects a group of instructions that may require extension of phase T1. The extend T1 for branch signal indicates a BST instruction or a ONE in index CR bit 9, either of which may require extension of phase T1 for the program address to settle. The decrement index skip signal is enabled whenever a DIS instruction is generated while the index register reflects all ZEROS (index TC active). The above conditions are combined with the CFI and CFR instructions in addition to the switch test skip and copy file signals to generate the extend T1 signal. The extend T1 signal is enabled by the above stated signals only when the logic is in the phase T1 go condition.

(10) The index count enable goes active when T1 GO is enabled and the DIS instruction or the index count normalize signal is active. The index count normalize signal is generated by the NRM circuit and is used to decrement the index counter for every T2 left shift of the operand or accumulator register during line painting.

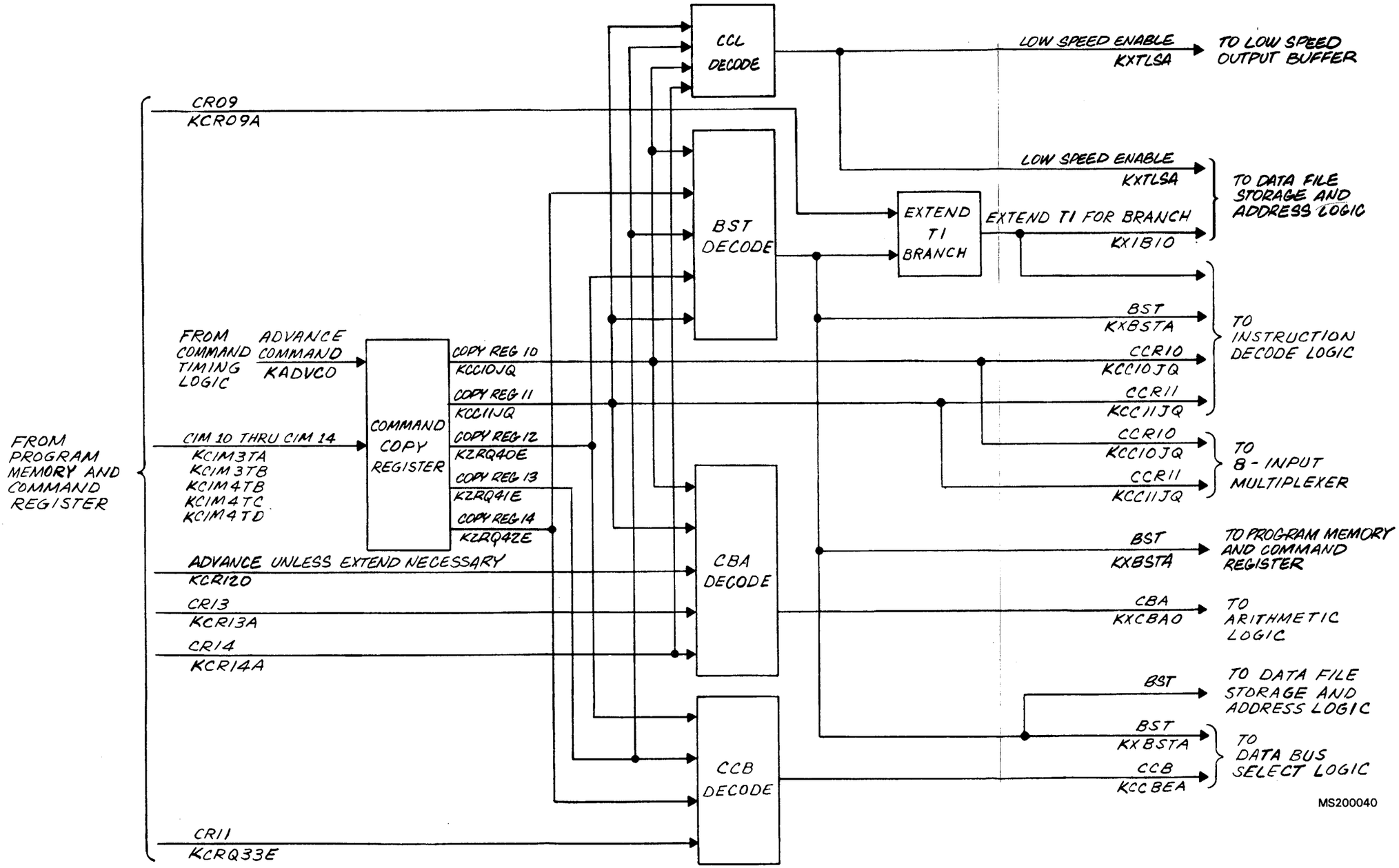


Figure 5-38. Timing and Control Command Copy Register Block Diagram

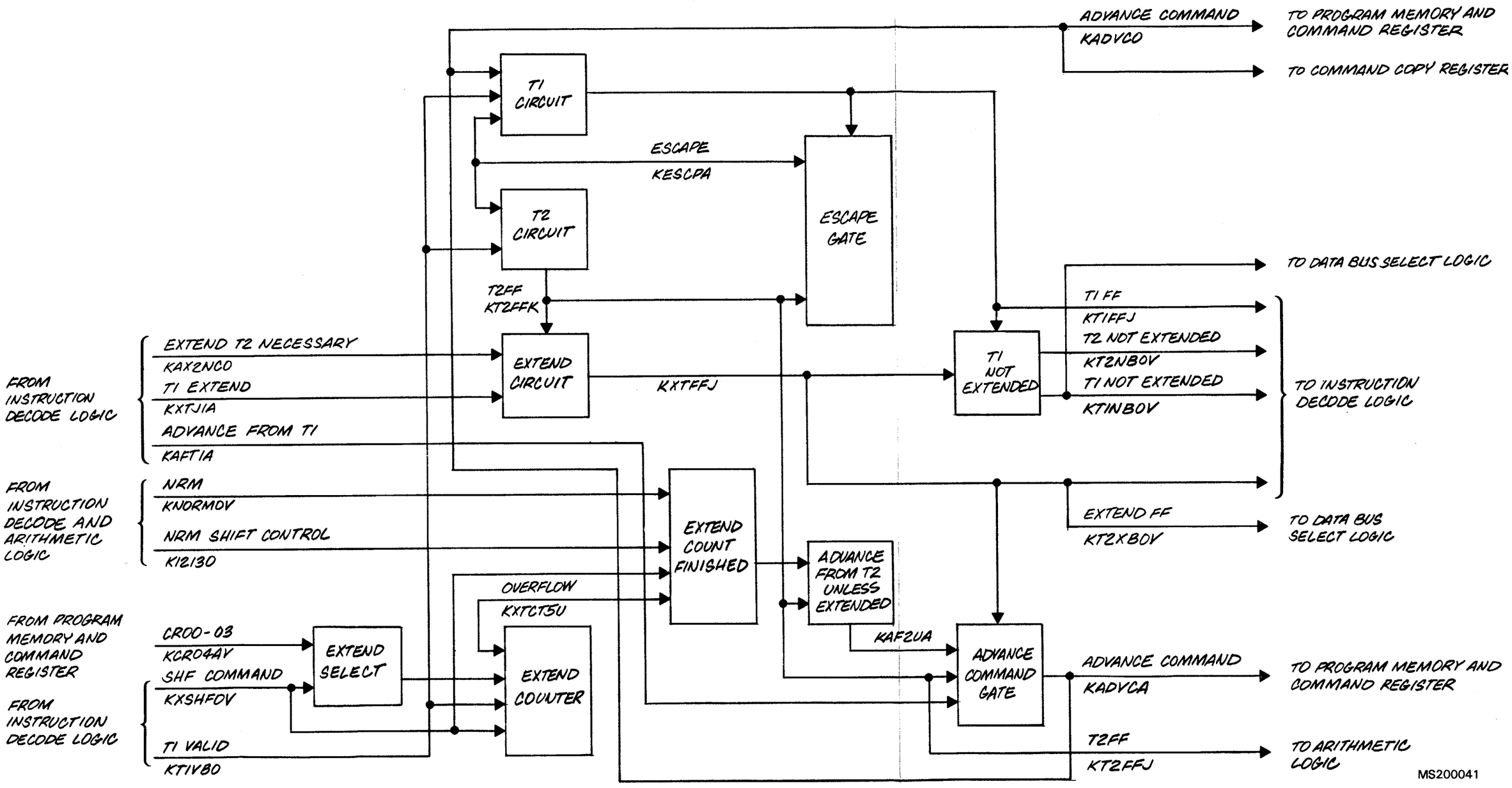


Figure 5-39. Timing and Control Command Timing Block Diagram

T1V = T1 VALID
ADVC = ADVANCE COMMAND

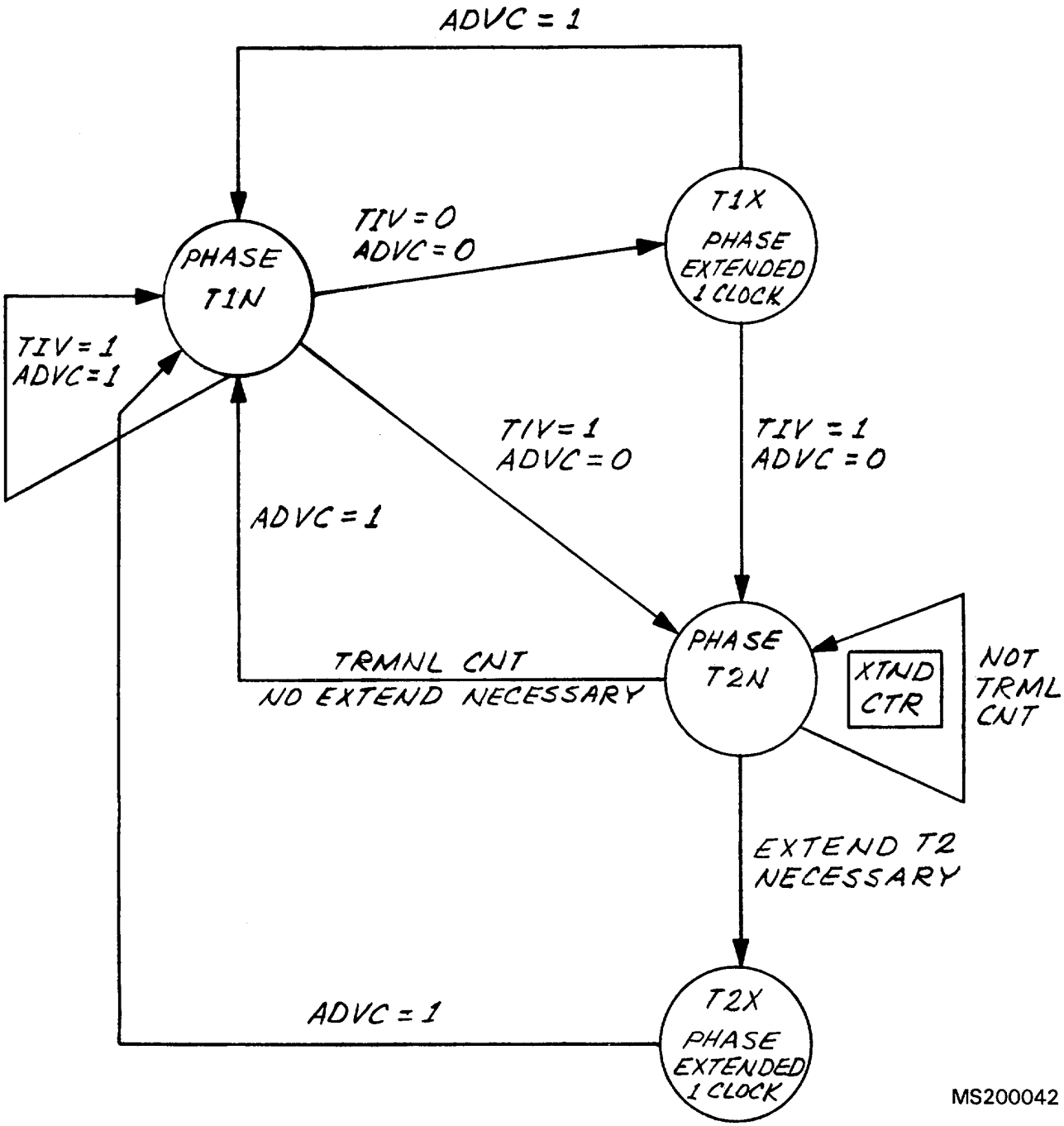


Figure 5-40. Phase T1/T2 Timing States

The NRM instruction is used to speed up the line painting process (scaling) from 128 μs to 64 μs for painting shorter lines on the crt.

(11) The T1 valid signal indicates that all preconditions for a particular instruction phase T1 operation are satisfied and that the T1 phase for that instruction can be terminated. These conditions are the absence of a T1 not extended, T1 wait, or extend TI signal and the active high speed transfer ready signal. The T1 not extended signal is enabled by the TXH instruction. The advance from the T1 signal is developed when, for a specific group of instructions, all conditions are satisfied to permit the logic to advance from T1 to the next instruction phase.

(12) A right side BIT sample enable signal is sent to the computer buffer/C-BIT BIT sample multiplexing when the DB is active and ready, T1 is in the wait condition, and the console video test signal is active. The signal indicates to the computer buffer/C-BIT that data is ready for testing.

e. *Data Bus Select (fig. 5-43, FO-27).* The data bus select utilizes current command word information to select the data bus source for a particular instruction. The bus select is controlled by the CD octal 80 signal from the instruction decode logic. When this signal goes low, indicating that the current instruction is one of octal 00 thru 07, the bus select chooses the CR07, CR08, and CR09 inputs for data bus selection. These three bits constitute the source code for copy instructions CBI, CBA, CBO, and CBH (refer to table 5-28). The bus select coding is identical to that for the source coding. For all other instructions which utilize the data bus, the CD octal 80 input is high. The operand register is selected for a group of instructions when utility bit CR08 is a ONE. These instructions are ESB and EQS and include instructions 20 thru 27 (CD octal 82 high) with the exception of NRM and SHF. The DB is selected by the STH instruction. The copy file instructions are defined by CD octal 81 and CR12 going high, selecting data file information. When phase T2 is extended, the data file source is selected by instructions CFB, MCS, DFS or CFI (CD octal 83 and CR12 high). The command register is utilized as the bus data source for a CCB or BST command. The T1 not extended signal, which indicates that the timing and control is in phase T1, permits the BST instruction to select the program address counter as the data bus source.

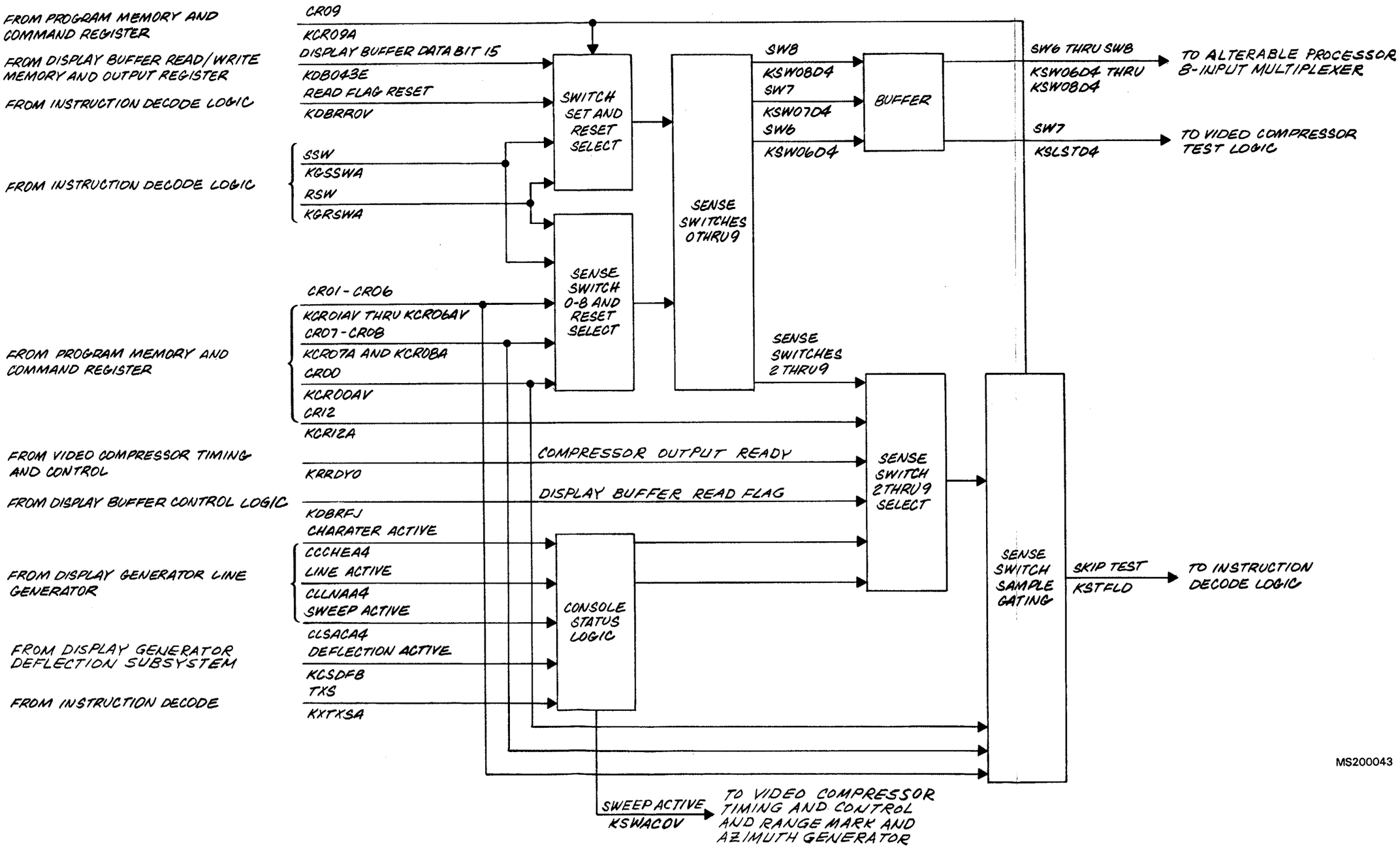


Figure 5-41. Timing and Control Sense Switch Logic Block Diagram

5-295/(5-296 blank)

Figure 5-42. Timing and Control Instruction Decode Block Diagram (Sheet 1 of 2)

5-297/(5-298 blank)

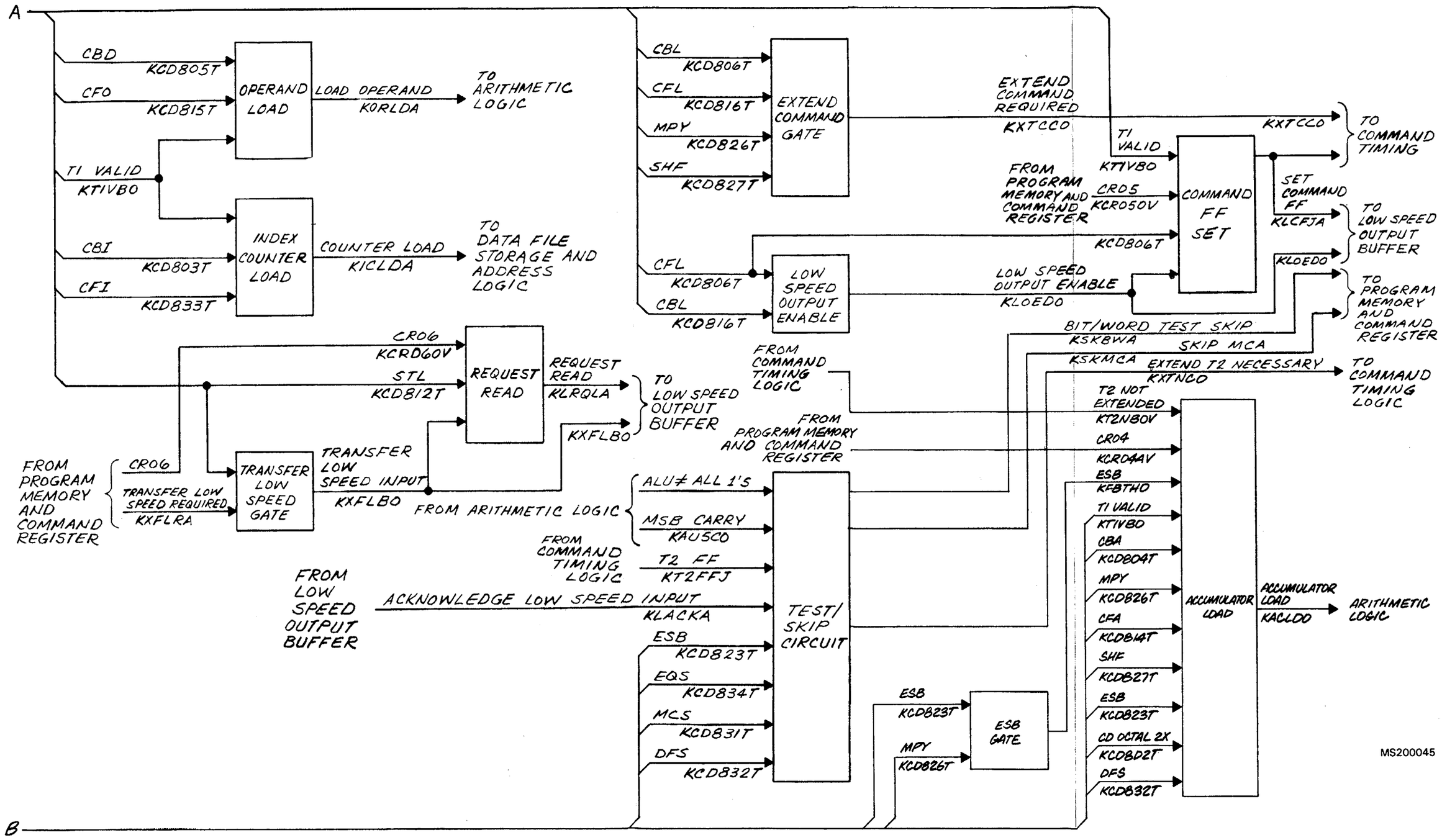


Figure 5-42. Timing and Control Instruction Decode Block Diagram (Sheet 2 of 2)

5-299/(5-300 blank)

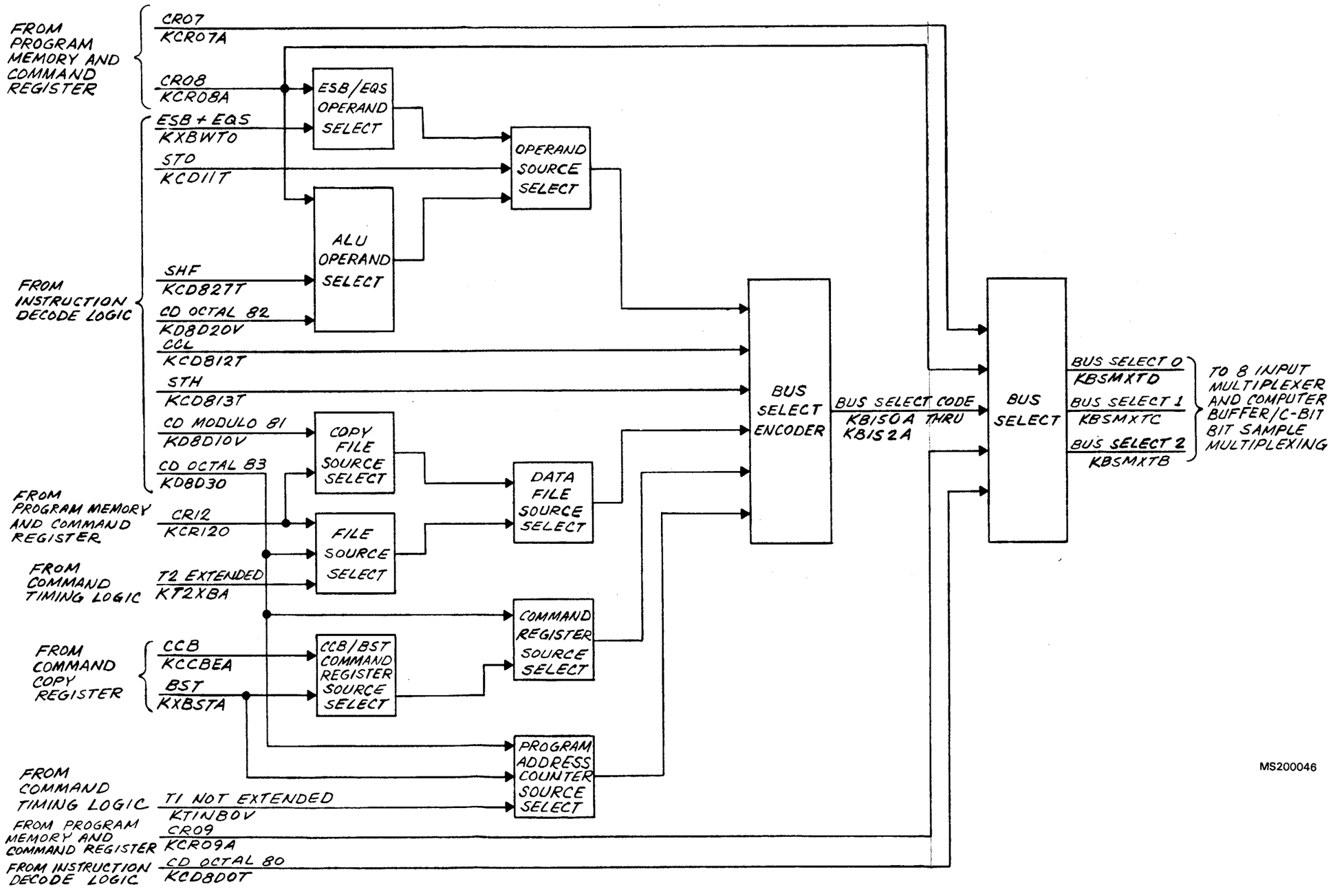


Figure 5-43. Timing and Control Data Bus Select Block Diagram

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Section V. DISPLAY BUFFER

5-26. General (fig. 5-44). The DB provides temporary storage for the synthetic video being transferred from the AP to the DC. The DB operates in a read or write mode. The read mode is initiated by the DC and the write mode is initiated by the AP. The DB consists of three sections: control logic, read/write address counter, and read/write memory and output register.

a. *Control Logic*. The control logic monitors and directs the read and write operation within the DB. The write mode is initiated by an AP high speed output ready signal to the control logic. The control logic then returns an acknowledge signal to the AP to initiate the write mode and to the read/write address counter to increment the write address counter to the next memory location. The control logic also sends an active signal to the DC indicating that the DB is busy. After signal exchange between the AP and DC, the control logic supplies a write enable signal to the read/write memory and output register. Upon preparing to enter the read mode, the control logic sends a not reading and read flag signal to the DC. Upon receiving the signals, the DC supplies a read flag reset signal to the control logic initiating the read mode. The control logic then sends a set read flag signal to the read/write address counter and to the read/write memory and output register. The control logic ensures that the input data is not written into a storage location containing unprocessed data. When the write address approaches an unprocessed storage location, the write mode is inhibited until the pertinent data is read and supplied to the DC. The DB loop signal from the computer buffer/C-BIT is used during testing and is covered under the computer buffer/C-BIT description.

b. *Read/Write Address Counter*. The read/write address counter generates read and write addresses and forwards the addresses to the read/write memory and output register. During the write mode, an acknowledge signal is sent from the control logic which allows the write address counter to be incremented to the next memory location. The presence of a read/write address select signal routes the 10-bit write memory address to the read/write memory and output register. In the read mode, the control logic sends a set read flag signal to the read/write address counter, which increments the read address counter. Upon the absence of the read/write select signal, the read/write address counter routes the new read memory address to the read/write memory and output register.

c. *Read/Write Memory and Output Register.* The read/write memory and output register is used to store words from the AP and then supply the words to the DC. In the write mode, the DB input select signal from the computer buffer/C-BIT determines whether C-BIT data or high speed data will be stored in the read/write memory. The control logic write enable signal transfers the 16-bit word from the AP to the memory location specified by the memory address from the read/write address counter. During the read mode, the control logic set read flag signal allows the memory location specified by the read/write address counter to be accessed by the DC.

5-27. Control Logic Detailed Description (fig. 5-45, FO-28). The control logic consists of the following elements:

Write/read capacity counter
Overflow circuit
Write data ready
Acknowledge circuit
Write enable
Select write address
Active circuit
Not reading circuit
Test control
Bit test loop
Read flag
Read active

The control logic generates the proper sequence of DB memory read and write mode enables. It also monitors the read and write address counters to ensure that input data is not written over unprocessed memory data. Figure 5-46 illustrates the input and output timing for the primary control logic elements.

a. The control logic functions in two modes: read and write. The two modes are functionally independent but are logically interlocked, on a first come-first served basis, from occurring simultaneously. The write mode is initiated by a high speed output ready signal from the AP high speed output buffer. When the read mode is not in progress, the high speed output ready signal activates the write data ready circuit. The write data ready signal temporarily inhibits the read active circuit, preventing initiation of a read mode. The acknowledge signal allows the write address counter to be incremented and also informs the AP that the write operation is in progress. The write data ready and the acknowledge signals also allow the selection of the new write address (read/write address select), write the AP data into memory (write enable), and inform the DC that the DB is performing a read or write operation (active). The write data ready and acknowledge circuits are then prepared to respond to the next command from the AP.

b. In the read mode, read flag signals are generated by the read flag circuit to inform the DC that the control logic is prepared to enter the read mode as long as no write mode is currently in progress. When the DC inputs data, a read flag reset signal is sent to the read flag circuit which activates the read active circuit. The resultant read flag signal allows the read address counter

to be incremented and the addressed data to be loaded into the output register.

c. The write/read capacity counter ensures that the input data is not stored in a memory location before the previously stored data is supplied to the DC. Each time a read or write mode occurs, the active signal allows the counter to be incremented for each read mode. When the counter indicates (count 900) that the write address counter is approaching a storage location containing unprocessed data, the overflow circuit inhibits the write data ready circuit.

d. The BIT test loop and test control provide test data functions and are discussed under the computer buffer/C-BIT description.

5-28. Read/Write Address Counter Detailed Description (fig. 5-47, FO-29). The read/write address counter consists of the following elements:

Read address counter
Write address counter
Address select

The read/write address counter generates the binary read and write addresses and forwards the selected address to the read/write memory and output register. The read and write 10-bit binary counters are used to store the write and read memory addresses. For each read mode operation by the control logic, the read address counter is incremented (read counter enable) and, for each write mode, the write address counter is incremented (write counter enable). The address select signal determines which address is routed through the address select to the read/write memory and output register. The 10-bit address is used to select one of 1024 memory locations.

5-29. Read/Write Memory and Output Register Detailed Description (fig. 5-48, FO-30). The read/write memory and output register consists of the following elements:

Input data select
Read/write memory
Output data circuit
Output register

The read/write memory and output register stores the 16-bit words from the AP and supplies the words to the DC. The input data select, under control of the C-BIT enable from the computer buffer/C-BIT, selects the test C-BIT data or, under normal operation, the 16-bit word from the AP high speed output buffer. The 10-bit memory address from the read/write address counter selects one of 1024 memory locations. The write function is generated by an acknowledge signal from the control logic which transfers the 16-bit word from the input data select to the addressed memory location. The read function is generated by a set read flag signal, which transfers the addressed word from the read/write memory through the output data circuit to the output register. The 16-bit word is made available to the DC 8-input mux and the computer buffer/C-BIT BIT sample multiplexing.

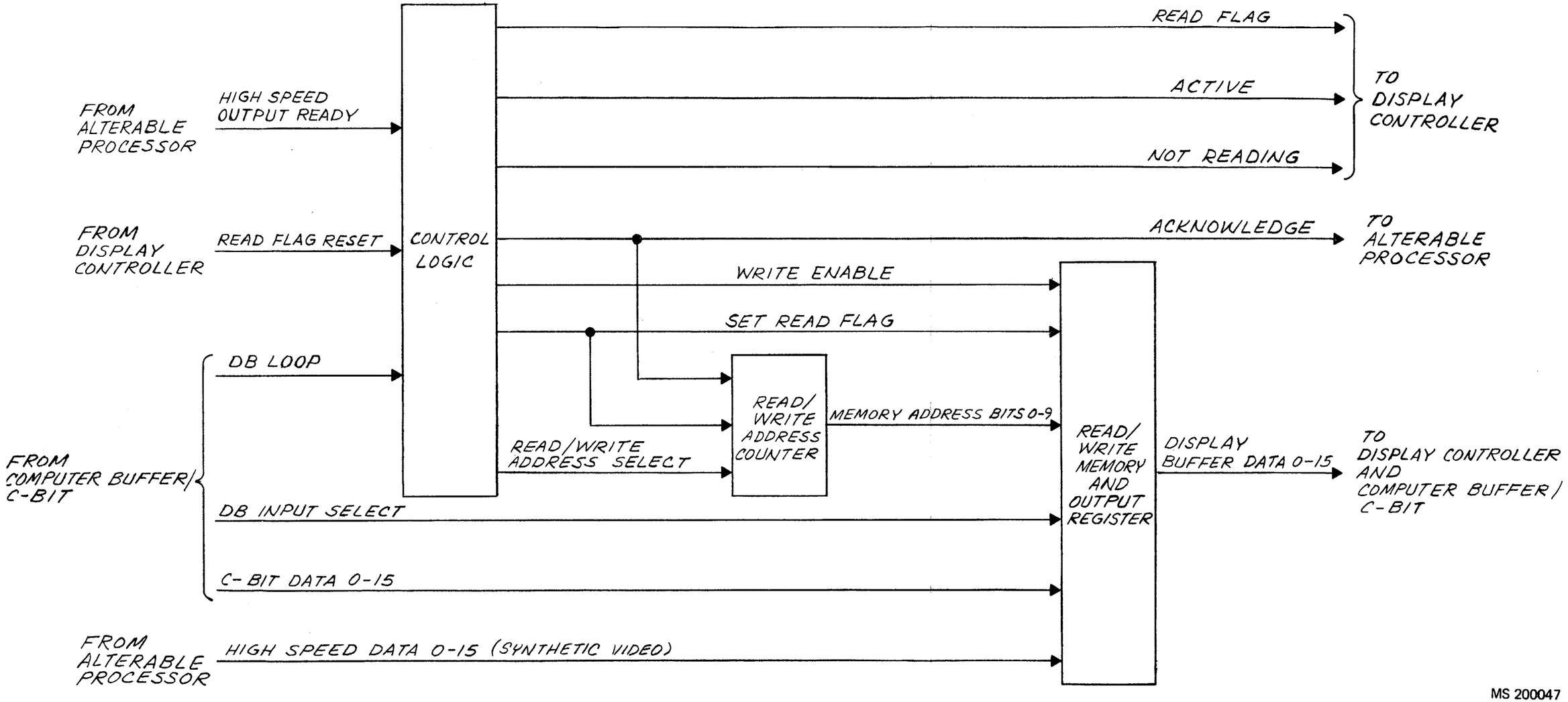


Figure 5-44. Display Buffer Block Diagram

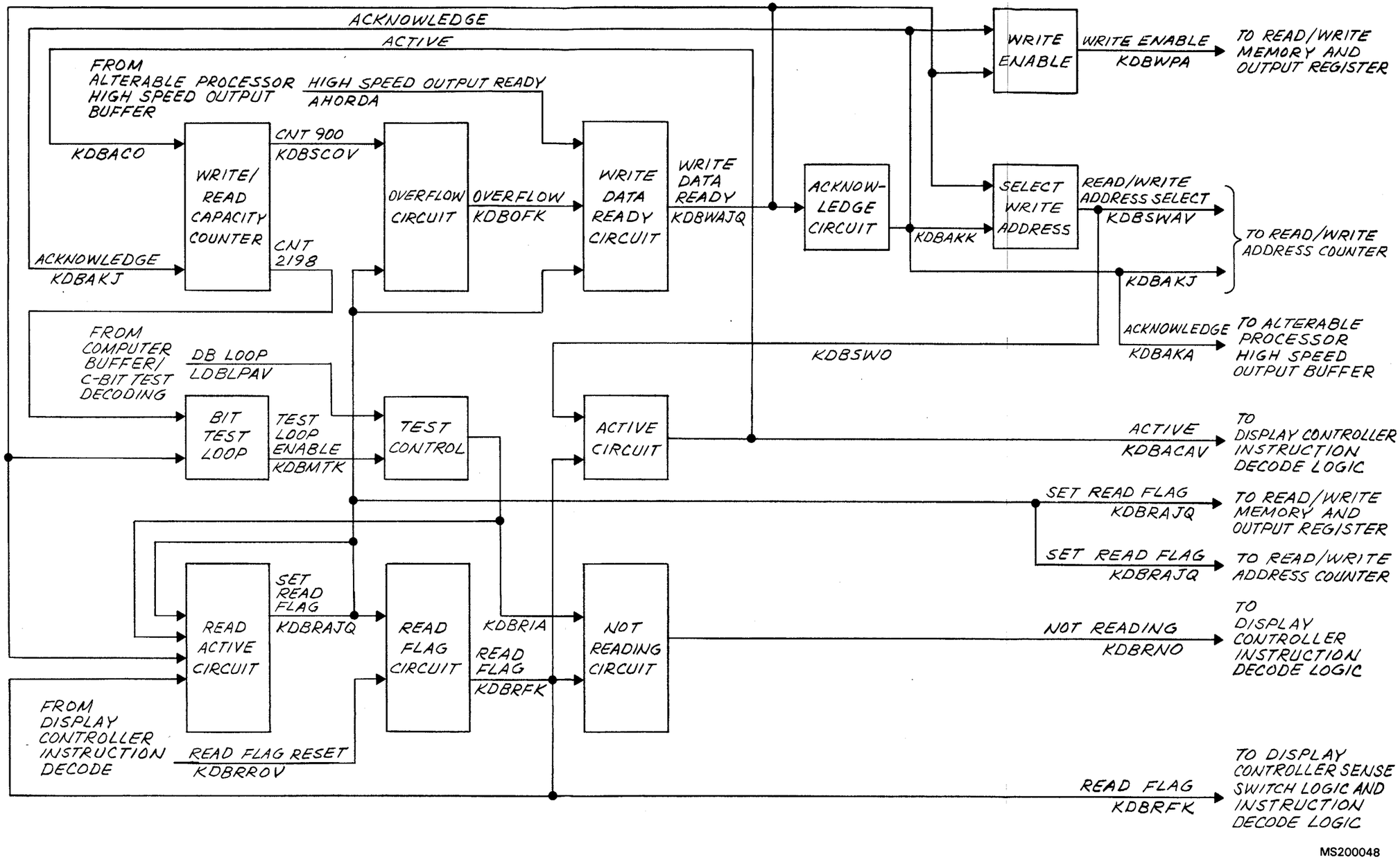


Figure 5-45. Control Logic Block Diagram

5-307/(5-308 blank)

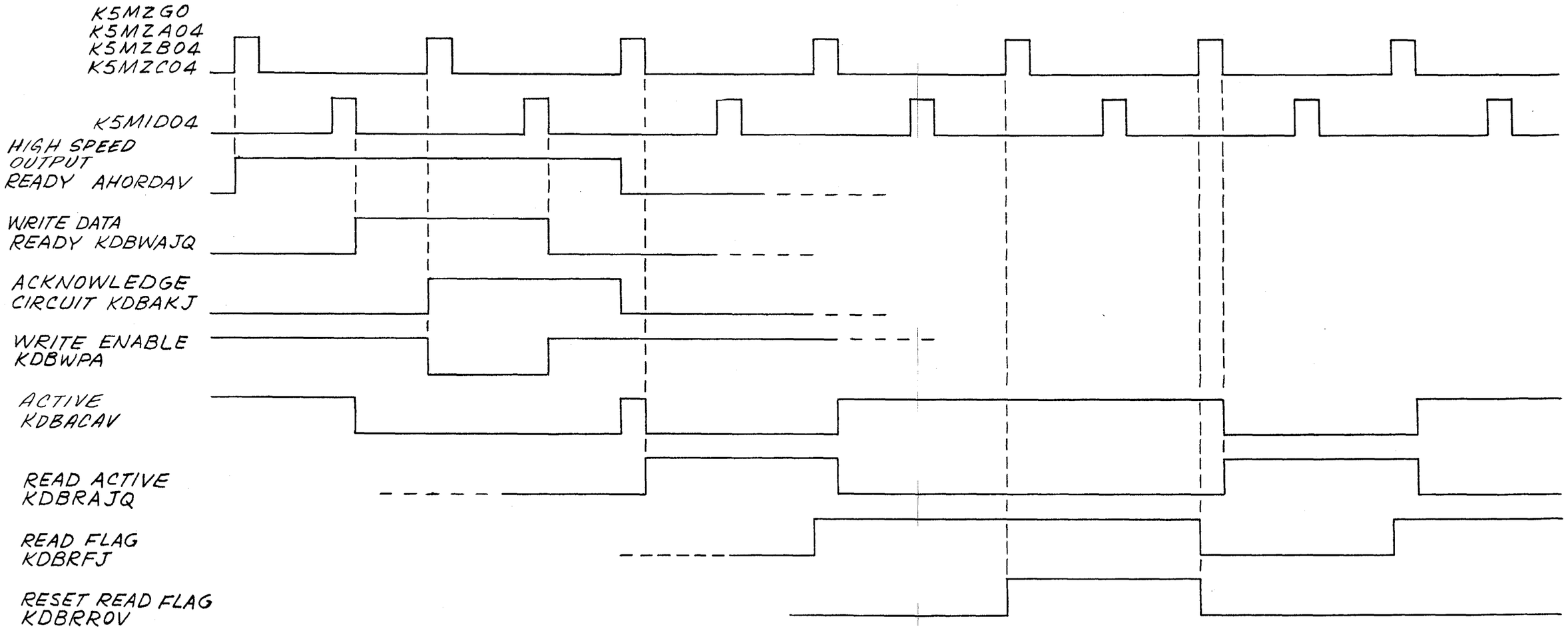


Figure 5-46. Control Logic Write and Read Mode Timing

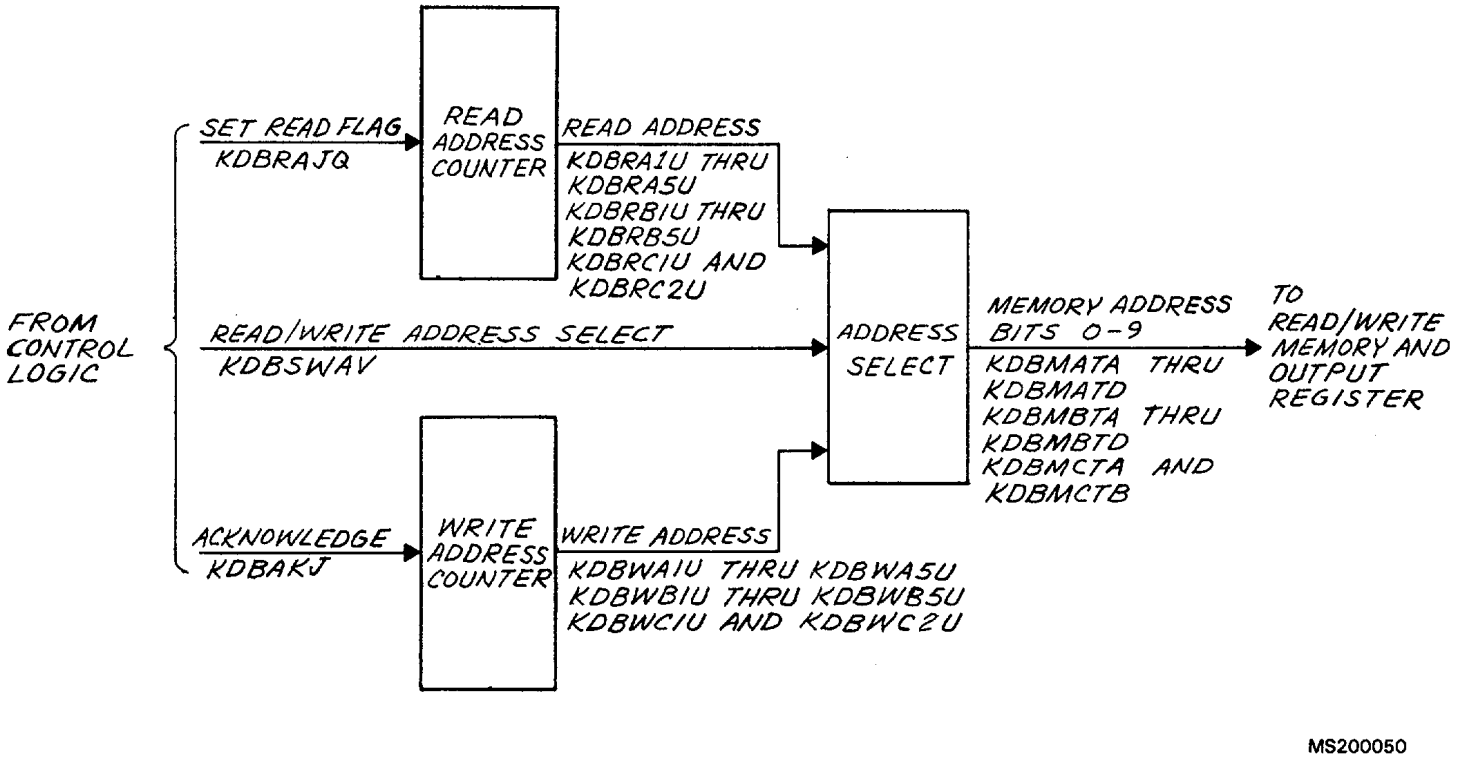


Figure 5-47. Read/write Address Counter Block Diagram

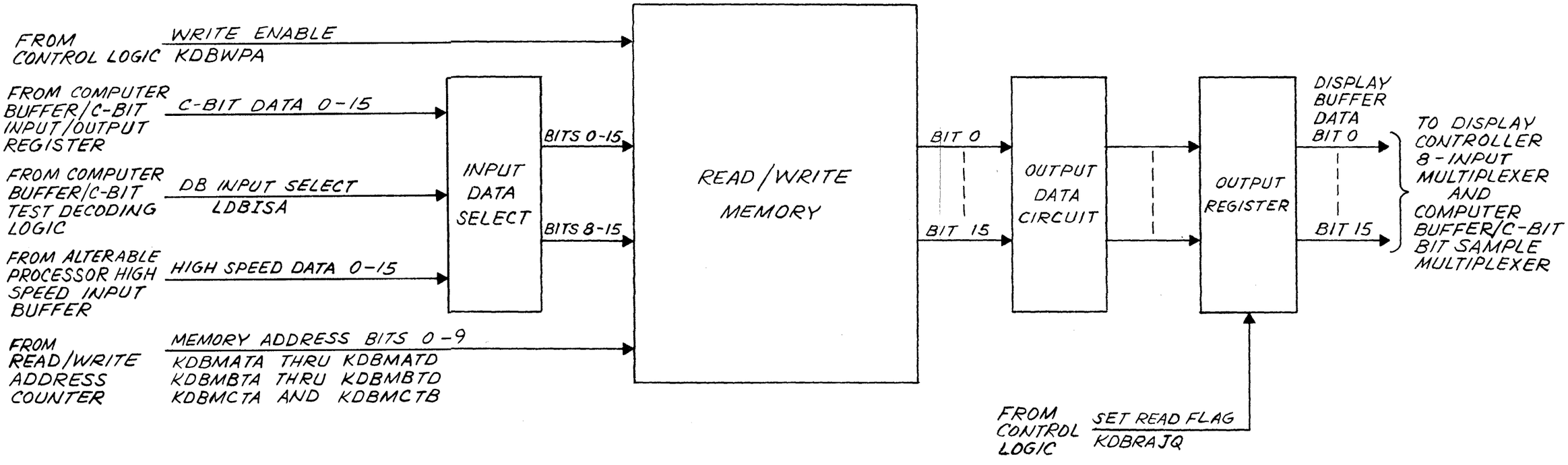


Figure 5-48. Read/Write Memory and Output Register Block Diagram

Section VI. VIDEO COMPRESSOR

5-30. General (fig. 5-49). The VC provides transmission frequency compression of RIE video data to be supplied to the DG. The VC comprises six primary functional logic circuits:

Radar video mixer
I/O logic
Memory
Range mark and azimuth generator
Test logic
Timing and control

a. *Radar Video Mixer.* This circuit combines the input RIE video and range and angle mark video with brightness control information from the front panel. This develops a weighted binary code indicative of the desired brightness for any one or combination of selected video channels. During the maintenance mode, channel selection is under control of the test logic. The 7-bit binary weighted code is forwarded to the I/O logic.

b. *I/O Logic.* The I/O logic receives the composite binary weighted coded video from the radar video mixer and converts the 7-bit unary code into a 3-bit binary code. The binary coded video is then either sent to memory to be stored for subsequent compression (compressed mode of operation) or sent directly to the DG (noncompressed mode of operation). When the VC operates in the compressed mode of operation, the I/O logic delivers the data to the DG at a rate five times greater than the input rate. Loading of the binary weighted video into the I/O logic is controlled by timing and control. When operating in the compressed mode, timing and control allows the video data to be loaded into memory. When operating in the noncompressed mode, front panel lamp control (through the range mark and azimuth generator) enables direct readout of the noncompressed binary coded video to the DG.

c. *Memory.* The memory is a two-channel storage device that temporarily stores data which is read out at a five times faster, or compressed, rate. The data received by memory is radar sweep display information consisting of binary weighted video from the I/O logic and a control line from timing and control. This input data is returned to the same elements at the compressed rate.

(1) *Storage channels.* The two storage channels of the memory are identical and alternately receive the radar sweep information. When radar sweep data is transferred into one channel at the normal (real time) rate, data for the preceding radar sweep is read out from the other channel at the compressed rate.

(2) *Storage capacity.* The memory storage capacity is sufficient to accommodate the data required for maximum radar range distance. When radar is used with shorter range distances, correspondingly smaller portions of memory storage capacity are selected. The memory receives radar range data signals from timing and control which select and enable the corresponding portion of memory capacity required for the radar range distance being used.

d. *Range Mark and Azimuth Generator*. The range mark and azimuth generator generates range and angle marks for input into the eighth channel of the radar video mixer. The range and angle marks are generated in accordance with dead time and azimuth signals from the RIE, instruction enabling signals (10-mile range, 20-kilometer range, angle marks, and compressor video control) from front panel lamp control, and control signals from timing and control. The range mark and azimuth generator also provides compressor video data signals to timing and control, the I/O logic, the DG, and the DC. Various test signals are received from and delivered to the test logic.

e. *Test Logic*. The test logic tests the operating function of the radar video mixer and the memory in accordance with test instructions received from the computer buffer/C-BIT. When test instructions are received from the computer buffer/C-BIT, corresponding test input signals are sent to the radar video mixer and memory. These test input signals initiate the generation of known test values which are sent to the radar video mixer and memory. The outputs from the elements being tested are sent to the test logic where the output data is compared with known reference values. The results of the comparison are delivered to the computer buffer/C-BIT for transmission to the IOX. Three categories of test instructions are sent from the computer buffer/C-BIT to the test logic. These categories are no-test (for periods of normal operation of the VC), radar video mixer output test, and memory output test.

f. *Timing and Control*. Timing and control generates the sequence of control and clock signals required to store RIE video data and output the compressed video data to the DG. Timing and control incorporates functionally identical circuits for memory channels A and B. Each circuit is mechanized to provide four modes: memory input sequence, memory shift sequence, memory wait, and memory output sequence. During the memory sequence (which is initiated by the RIE range zero signal), the selected channel logic provides the control signals which step the RIE input data and the control bit into the memory logic at a 1-MHz sample rate. During the memory shift sequence (which is initiated by the RIE dead time indication), the memory data is shifted to the output memory location at a 5-MHz rate. The logic then notifies the DC that video data is ready and waits for a response. When the sweep lost is received, the memory output sequence transfers the compressed video data to

the DG at a 5-MHz rate. Timing and control also accepts and stores new radar range data from the front panel and informs the memory which portion of memory is required to process the video sweep data.

5-31. Radar Video Mixer Detailed Description (fig. 5-50, FO-31.) The radar video mixer consists of the following elements:

Video brightness controls
Channel select
Test channel select
Test reference voltage generator
Channel gain scaling
Summing circuit
Mixer code generator

The radar video mixer, under control of the front panel VIDEO BRIGHTNESS and VIDEO SELECTIONS controls, processes selected input video signals to develop a weighted binary code representative of the desired brightness for the selected channels. This circuit also provides simulated video signals for each channel during the maintenance mode.

a. *Normal Operation*. During normal operation, the mixer inhibit level from the test logic is low, enabling the channel select. Any one or combination of seven front panel enables, corresponding to the seven channels of video inputs from the RIE, may be active. The range and angle mark video input is hard-wire selected and therefore continuously processed. When a channel is selected, the weighted brightness code generates a channel gain-scaled signal whose amplitude is proportional to the video input and the selected brightness. All selected channel gain-scaled signals and the range and angle mark video are combined in a summing circuit to provide a composite video signal, which is applied to the mixer code generator. The circuit comprises seven comparators, each of which is enabled by 0.5v increments of the 0 to 4.0v composite video. The output, which is a weighted binary code proportional to the composite video, is forwarded to the I/O logic.

b. *Maintenance Mode*. During the maintenance mode, the mixer inhibit level goes high, disabling the channel select. The maintenance mode routine sequentially enables each of the nine test inputs to the test channel select. For channels 1 thru 8, a test reference voltage is applied to the associated channel gain scaling circuit, developing the composite video signal which is processed as previously described. When the mixer check input is activated, the channel gain scaling circuit is disabled, effectively developing a quiescent output.

5-32. Input/Output Logic Detailed Description (fig. 5-51, FO-32). The I/O logic consists of the following elements:

Sampling register
Priority encoder
Memory A input circuit
Bypass enable
Memory B input circuit

The sampling register samples the 7-bit binary weighted mixer output from the radar video mixer at a constant rate. Sample register clock A or B from timing and control clock the mixer output. The priority encoder then converts the binary weighted video from the sampling register into a 3-bit binary coded video output. The I/O logic operates in two modes, noncompressed and compressed, each of which is described below.

a. *Noncompressed Mode*. In the noncompressed mode, the bypass enable circuit is activated by a compressor video signal from the range mark and azimuth generator which supplies the binary coded video output from the priority encoder directly to the output register. The output register clocks out the binary coded video to the DG video subsystem at the same rate that the priority encoder is generating the coded video.

b. *Compressed Mode.* In the compressed mode, the I/O logic alternately delivers the binary coded video data, at a normal rate, to memory channels A and B. Timing and control provides alternating channel A and B load enable signals to memory channels A and B to allow the input of successive sets of data, corresponding to full display sweeps. The successive sets of data are alternately loaded into and stored in one memory channel at a time. The I/O logic also retrieves the same information that it had stored in memory and sends the information to the output register at a compressed rate (five times greater than the normal memory input rate). The information is alternatively retrieved in reverse sequence from the order of input. When a full sweep of data is supplied at a noncompressed rate into one memory channel, a full sweep of data is being retrieved at a compressed rate from the other memory channel. The successive sets of 3-bit binary coded video data (corresponding to full sweeps) received by the output register circuit are
clocked out to the DG video subsystem at a compressed rate.

5-33. Memory Detailed Description (fig. 5-52, FO-33). The memory consists of two identical channels, A and B, which consist of the following elements:

Radar range select
A and B input data gating
A and B 384-mile memory
A and B 256-mile memory
A and B 128-mile memory

The memory provides two channels of serial shift storage for the binary coded video from the input logic. The portion of the 4608/bit-per-line memory used to store the input sweep data is dependent upon the radar range (384, 256, or 128 mile) currently selected. The operation of both channels is identical; therefore, only channel A is described. The memory is apportioned into three stages of 1536 bits each. The number of stages utilized is dependent upon the radar range inputs from timing and

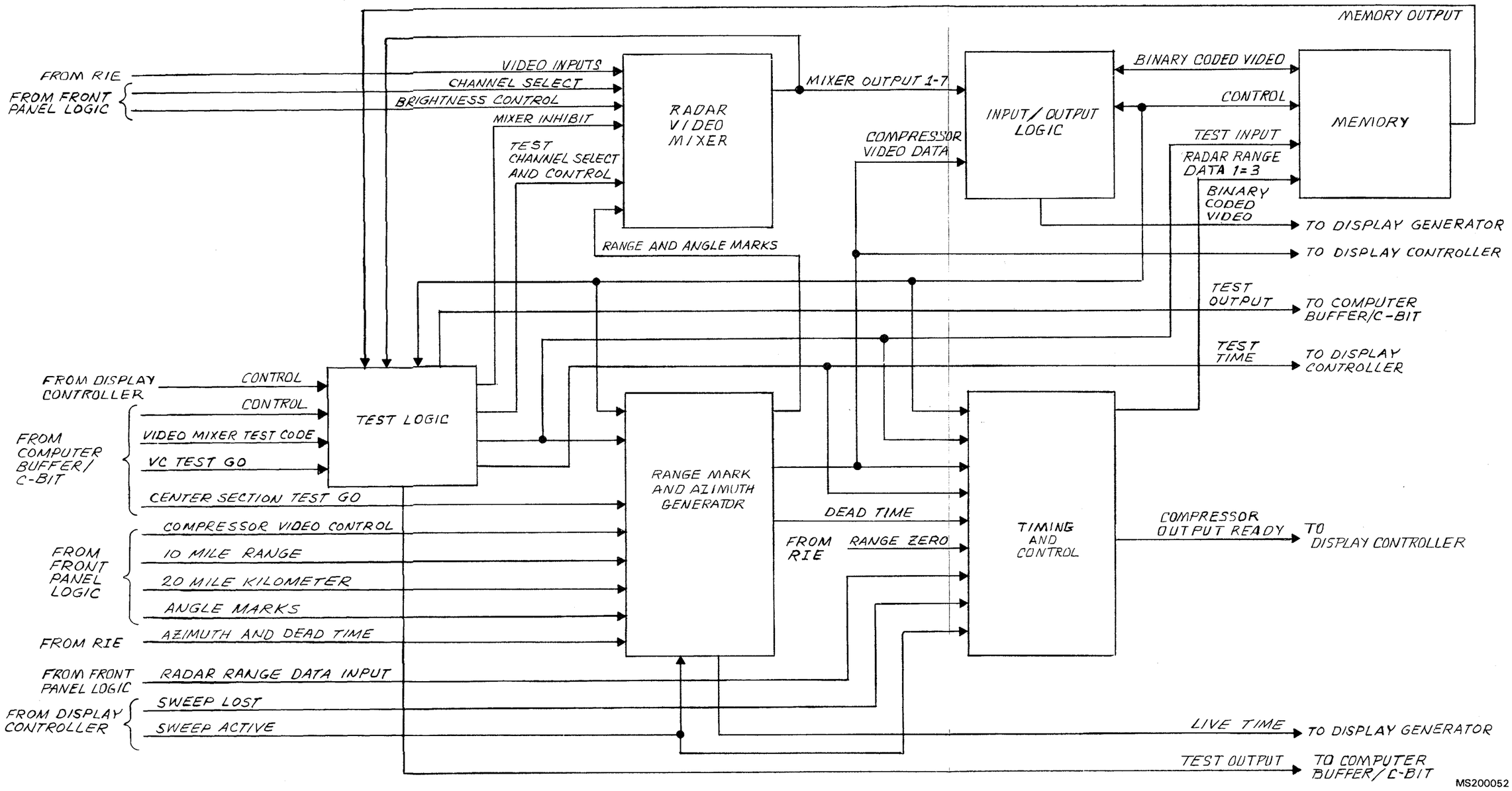


Figure 5-49. Video Compressor Block Diagram

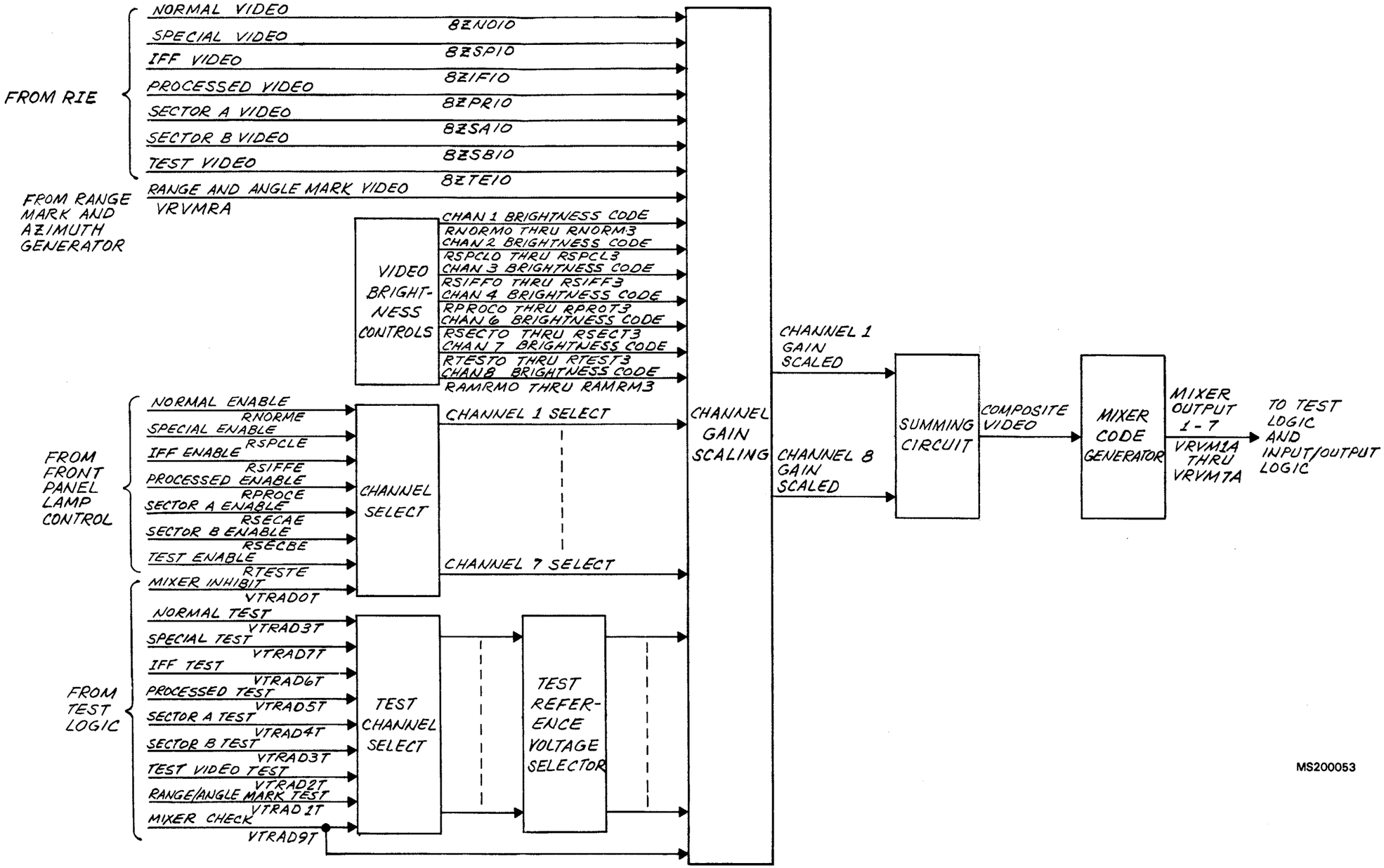


Figure 5-50. Radar Video Mixer

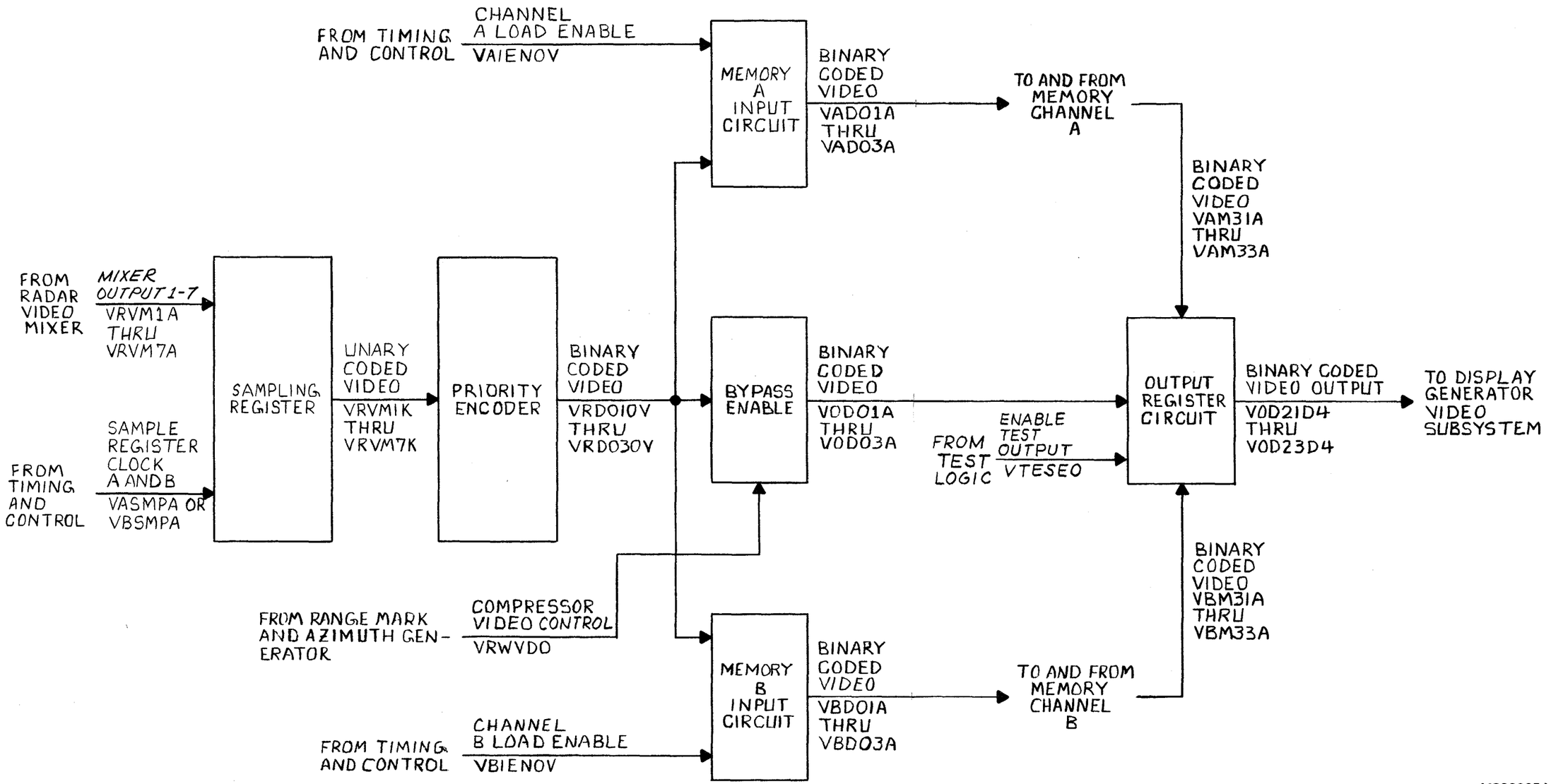


Figure 5-51. Input/Output Logic Block Diagram

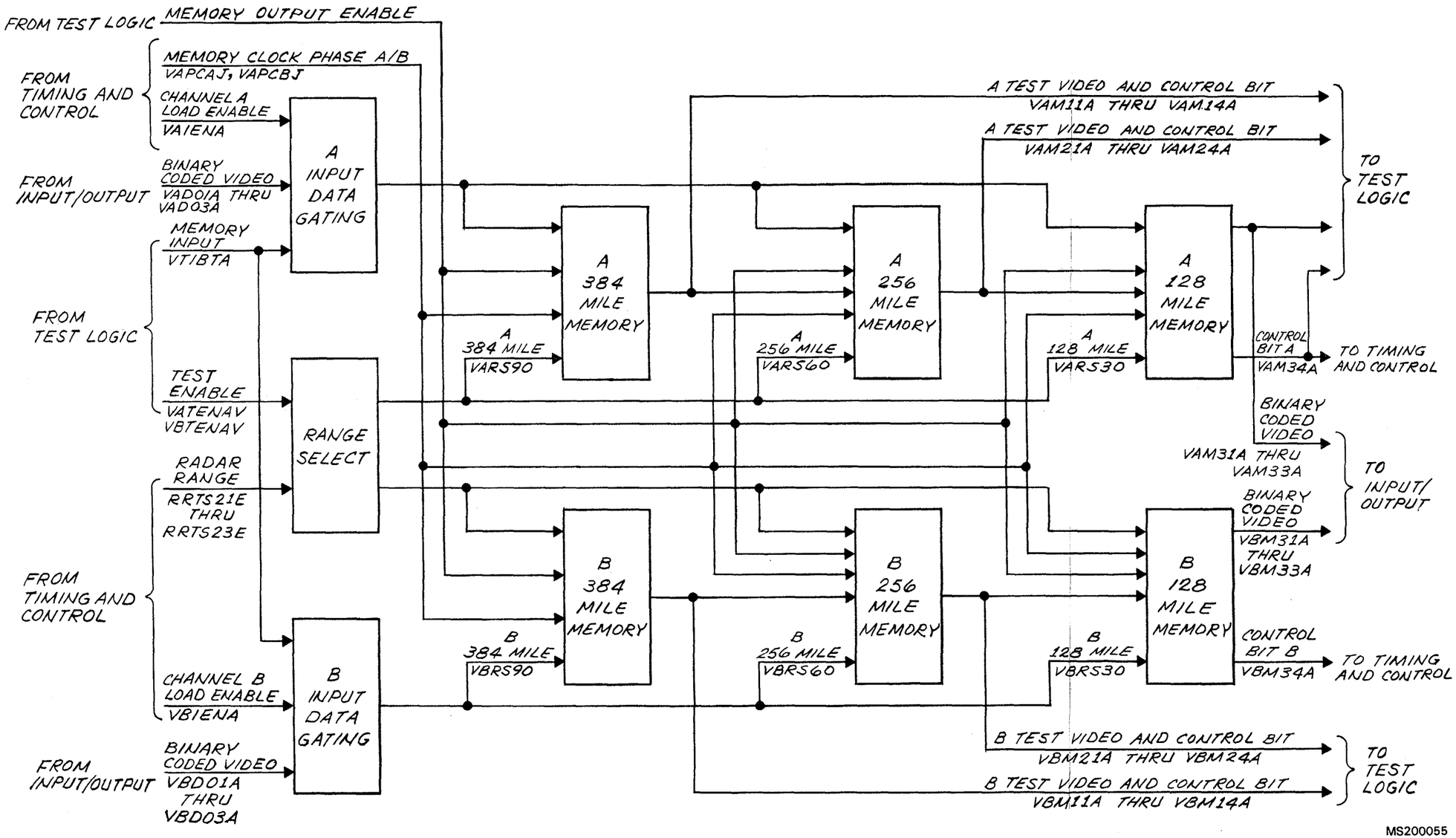


Figure 5-52. Memory Block Diagram

control. For a 128-mile range, only the last stage is utilized; for a 256-mile range, the last two stages of 3072 bits are utilized; for a 384-mile range, the full 4096-bit memory is utilized. Upon receipt of the RIE range zero signal, indicating that a radar sweep of data is to be transmitted, the timing and control activates the load enable line. This signal will supply the control bit to line 4 of the channel memory. The control bit, when shifted through the memory, indicates when radar sweep data is prepared for output. The timing and control then forwards a train of 1-MHz memory clock pulses which shift the input binary-coded video into and through the memory. The radar sweep data is shifted until the control bit is detected in the final memory location. When the DG is prepared to receive radar video, the timing and control supplies a 5-MHz clock train to shift the sweep data out of memory. During the maintenance mode, the radar range select is disabled and the full 4096 memory is utilized to process the input test data.

5-34. Range Mark and Azimuth Generator Detailed Description (fig. 5-53, FO-34). The range mark and azimuth generator consists of the following elements:

DC interface circuit
Live time input
Live time output
Range mark counter
Clear circuit
Tracking counter
Mixer intensity circuit
Clock gate

The range mark and azimuth generator receives four operator-selected inputs from the front panel lamp control. The selected inputs are 10-mile range mark, 20-km range mark, angle marks, and compressor video control.

a. *Live Time Output.* The live time output delivers a live time signal to the DG upon receiving the following: compressor video control from lamp control; a sweep active signal from the DC; a test disable signal from test logic; and a radar dead time signal from dead time input. The live time output will also send a live time signal to the line generator upon receiving channel A and B output time signals from timing and control.

b. *DC Interface Circuit.* The DC interface circuit receives dead time and azimuth signals from the RIE. The azimuth input signal denotes an angle mark sweep and remains active during the duration of the sweep. The DC interface circuit supplies the azimuth signal for readout when an angle marks signal from the front panel lamp control is received. The azimuth signal is then sent to the mixer intensity circuit to enable angle mark displays.

c. *Dead Time Input Circuit.* The dead time input circuit receives a dead radar time signal from the DC interface circuit and outputs the corresponding dead time enabling signals to the live time output, the tracking counter, the clear circuit, and timing and control.

d. *Range Mark Counter.* The range mark counter, upon receiving a selected 10-mile range of 20-km signal from the front panel lamp control and an enable signal from the test logic, starts counting from ZERO up to a preset value. The counter is clocked by range mark counter clock signals received from timing and control through a clock gate. The clock gate supplies a counter increment signal to the range mark counter and the test logic. When the preset count value is reached, the RMC range mark enable signal is sent to the mixer intensity circuit and the clear circuit. During the counting cycle, the range mark counter sends range mark counter test signals to the test logic for memory testing. The clear circuit, upon receiving RMC range mark enable and range mark counter clear signals, sends a count signal to the tracking counter and a counter clear signal to the range mark counter. As a result, the tracking counter advances one count from ZERO, towards a preset value, and the range mark counter is reset to ZERO count. The range mark counter continues the same count-reset cycle until the tracking counter reaches its preset value and sends a TC range mark enable signal to the mixer intensity circuit. The mixer intensity circuit then provides a range and angle marks video signal to the radar video mixer representing a range mark display indication.

e. *Mixer Intensity Circuit.* The mixer intensity circuit provides three levels of output video in accordance with range and angle mark signals: no output for standby periods, medium intensity output, and high intensity output. When the angle mark and range mark input signals are inactive, the output is at a low standby level. When only the angle mark signal is active, the output is at a medium intensity level (for the entire sweep). When only the range mark input (both TC and RMC range mark signals) is active, the output is at a high intensity level. Thus, when both range and angle mark displays are selected, the mixer intensity circuit output will be at a continuous medium intensity level with periodic high intensity spikes for sweeps denoting angle marks, and at a continuous very low level with periodic high intensity spikes for intervening nonangle marked sweeps.

5-35. Test Logic Detailed Description (fig. 5-54, FO-35). The test logic consists of the following elements:

Test input decode
Memory test initiate
Mixer test comparator
Test counter
Test start/stop circuit
Reference data generator
Test output control
Memory test comparator
Test output enable
Test latch
Test output select

Three categories of video mixer test codes are sent from the computer buffer/C-BIT to the test logic. These test code categories are no-test, video mixer output test, and memory output test. The video mixer test codes are sent in binary coded form to the test input select.

a. When the no-test code is received, the test input decode sends a low mixer inhibit signal to the radar video mixer and the VC performs its normal processing function. When the video mixer output test code is received by the test input select, one of eight test channel select signals is sent to the radar video mixer, and the VC interrupts normal operation to test the video mixer output. When the memory output test code is received, the test input decode sends a low mixer check signal to the radar video mixer, which inhibits the channel gain scaling operation. The VC then tests the memory for proper operation.

b. Each of the eight radar video mixer channels is sequentially selected and tested by the test logic. The test instruction code pertaining to a radar video mixer channel is sent to the test input decode. The test input decode is a binary-to-unary converter. The test input decode sends the test channel select signal to the radar video mixer. Normal video inputs are inhibited and a known test signal is placed into the selected video processing channel. The output from this channel is sent to the mixer test comparator. The mixer output signal is compared with a reference value signal received from the test input select. The results of the comparison are sent to the test output select. The computer buffer/C-BIT provides select instruction signals to extract the comparison data from the test output select and determines the operating status of the radar video mixer channel being tested.

c. The memory is tested by placing a series of consecutive known data words into the input of each memory channel and comparing the memory output words with reference values. The range mark counter in the range mark and azimuth generator and the test logic test counter are used to control the intervals at which known values are fed into memory. The range mark counter is a continuous repeat cycle counter and the count values are sent to the reference data generator and test counter.

d. To test the memory operation, the computer buffer/C-BIT sends a memory test code to the test input select, a center section test go signal to the test start/stop circuit, and a VC test mode signal to the memory test initiate. The test input select responds by sending a low mixer check signal to the radar video mixer, which inhibits normal RIE channel input processing. The memory test initiate responds by sending a test enable signal to the following: range mark and azimuth, to inhibit live time and video output signals; memory, to enable the input of known test words into each of the memory channels; timing and control, which selects the clocking frequency for the memory input; and test latch, which enables the latching circuit. The test start/stop circuit responds by sending the following: a counter enable signal to the test counter, which enables the test counter to receive incrementing signals from the range mark counter; a test time signal to the DC timing and control sense switch logic; a memory output enable signal to the memory, to enable test data readout from each memory channel; a memory input signal to the memory, which designates that the initial set of words fed into memory shall be of ZERO value (256 words of 0000); and a test time signal to timing and control, which enables clocking signals for the range mark counter. The reference data generator responds by sending a reference data signal to the memory test comparator, which is used as comparison reference words when the test words are sent from memory.

e. The memory test comparator receives 4-bit reference words (1111) that will be compared with the test words from memory. The test output enable is inhibited, which prevents comparison data from being sent' to the test latch.

f. When the range mark counter reaches a count of 256, the test start/stop circuit sends a memory input signal to memory. As a result, a second set of consecutive inverted BIT test words (1111) are placed into memory. The memory will output the test words in inverted form (0000).

g. When the range mark counter reaches a count of 308, the memory outputs the first test word. The test word is compared with the reference words in the memory test comparator. Since the test output enable is inhibited, no action will occur.

h. At a range mark counter count of 512, test output control sends an enable test output signal to the test output enable, which allows the memory test comparator output data to be sent to the test latch. The test latch will detect and hold any fault condition indicated in the memory test comparator output data. The comparator test status data is sent to the test output select for output in accordance with mux select signals received from the computer buffer/C-BIT bit sample mux.

i. When the range mark counter reaches a count of 563, the first word of the next set of inverted BIT test words reaches the output of memory. At this time, the reference data generator sends inverted BIT reference words to the memory test comparator for comparison testing of the second set of test words from memory. The second set of test words continues to be test compared and monitored in the same manner as the first set until the range mark counter reaches a count of 768. At this time, the test time signal from the test start/stop circuit to timing and control is inhibited; this in turn stops the clocking signals to the range mark counter.

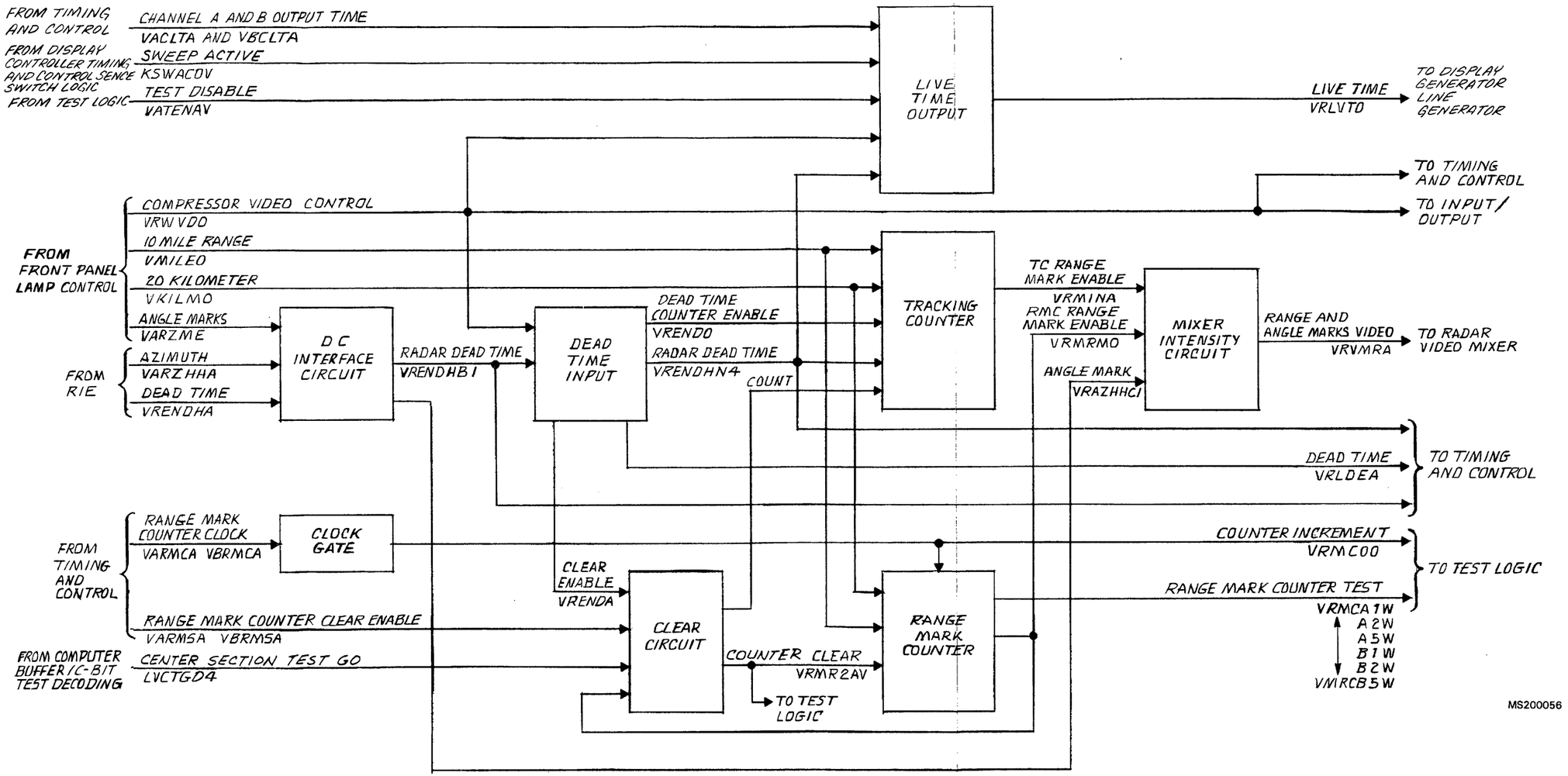


Figure 5-53. Range Mark and Azimuth Register Block Diagram

5-327/(5-328 blank)

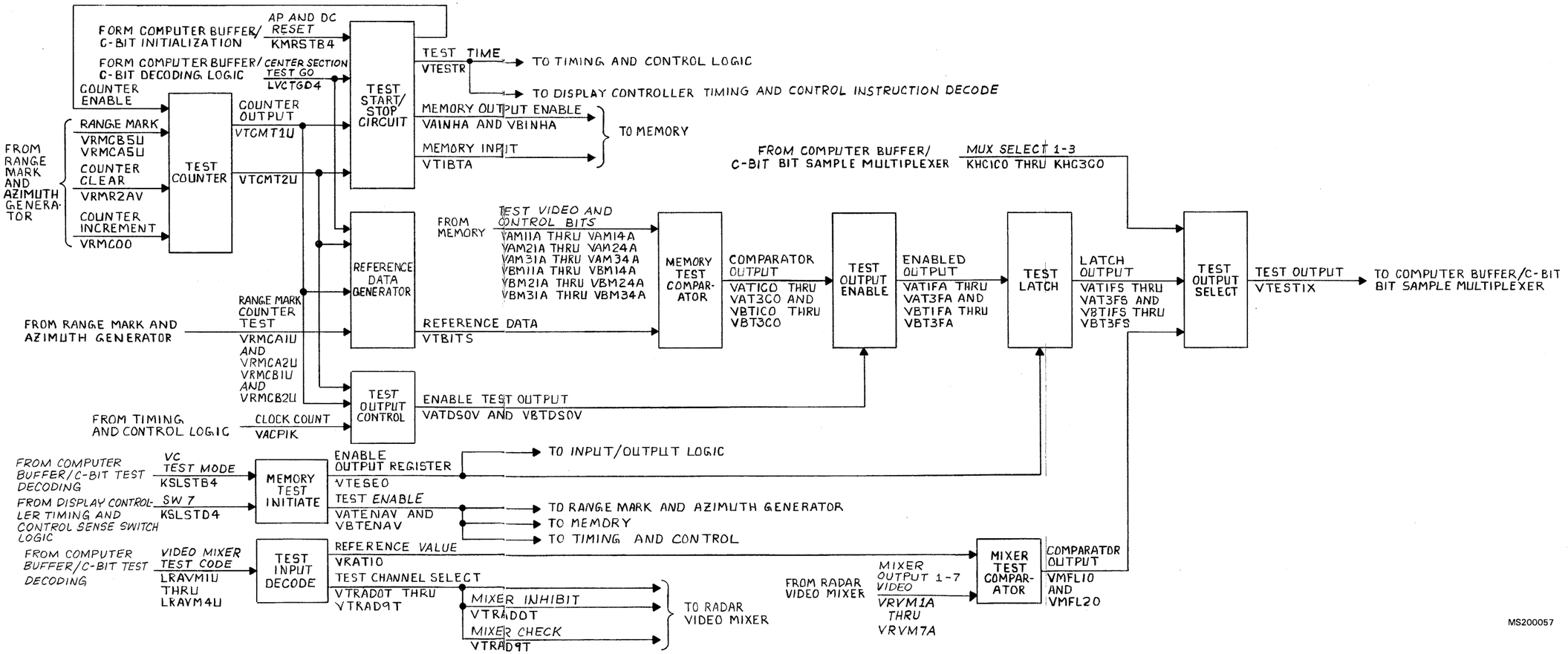


Figure 5-54. Test Logic Block Diagram

5-36. Timing and Control Detailed Description (fig. 5-55, FO-36). The timing and control consists of the following elements:

Radar range comparator
Hold register load
Line receiver
Range zero control
Channel select
Control bit B
Compressor bypass
Master reset
Output ready
Channel A and B live time enable
Reset counter enable latch
Channel A and B load radar
Clock counter enable latch
Range mark counter control
5 clock counter
Set data output
Data shift enable
Channel A and B data shift latch
Channel A and B data output
5-MHz clock circuit
1-MHz clock decode
Clock frequency circuit
Memory clock
Sample register clock A and B
Range mark counter clear enable
Range mark counter clock

The timing and control timing diagram is shown in figure 5-56.

a. Timing and control accepts and stores the radar range select bits from the front panel. When a new sweep range is selected at the front panel, the radar range shift enable to the radar range comparator is active for 12 clock times. The radar range shift enable is accompanied by a 12-bit chain of data (radar range serial input) to the radar range comparator. When the enable goes inactive, the last 4 bits of the serial data, representing the sweep range, are stored. The radar range comparator generates a single pulse at the trailing edge of the shift enable. This tests the comparison between the newly-stored range data and the range data previously stored. When the two values differ, a hold register load signal is generated, transferring the range code to the load register. The 3-bit unary code, representing maximum sweep ranges of 128, 256, or 384 miles is supplied to the memory to determine the length of memory required to store the input range video data. New sweep range selection also enables the master reset. This initializes required timing and control logic for the next video data input operation. The master reset is also enabled by reset signals from the computer buffer/C-BIT initialization and the test logic.

b. The VC alternately utilizes two channels to input, store, and output video data. Channel selection is initiated by the range zero input which indicates that the RIE is prepared to supply a radar sweep of video data. Channel select, which is toggled by each range zero input, alternately provides the required enables to the channel A and B live time enable circuit, reset counter enable latch, and data shift enable.

c. The functional operation of both channel A and B timing and control is identical; therefore, only channel B is described. The range zero input, in conjunction with an active channel B select, generates the channel B live time enable, which sets the channel B load. The channel B load permits the channel B memory logic to accept the input video data. This output also provides the control bit for line four of the 4-line memory. This control bit, when shifted through to the last memory location, will indicate that the video data is ready to be supplied to the DG. The live time enable signal also sets the clock counter latch which starts a . 5 clock counter, initializing the memory input sequence portion of the operation. The counter divides the 5-MHz clock input by five, providing five iterative time slots and the l-MHz clock at which the input video is sampled and stored. The counter is designed to produce a nonlinear binary count of 1, 3, 7, 6, 0 which can be conveniently decoded into the required time slots.

d. During the memory input sequence, the clock frequency circuit is conditioned to pass the output of the 1-MHz clock decode. In conjunction with the clock counter outputs and load enables, the clock develops the various timing signals required to process the video data and drive the range mark counter in the range mark and azimuth generator. At time slot 3, a signal is supplied to the 1/0, transferring the current binary weighted data to a sample register. The memory clock generates a dual-phase memory clock, at 0.5-MHz per line, which provides the combined l-MHz clock required to shift the data into and through the memory. The range mark counter clock increments the range counter on each output negative-going edge. The range mark counter clear enable tests the output of the counter for the required maximum count. This operation continues as long as data is being supplied from the RIE.

e. When all data for the current radar video sweep has been input, the radar dead time signal resets the channel B load radar and the clock counter enable latch. The channel B load enable signal to memory is then removed and the ÷5 clock counter is cleared and inhibited. This terminates the l-MHz pulses to the memory and the range mark and azimuth generator. The memory input sequence is now complete and the memory shift sequence is initiated.

f. The radar dead time signal allows the data shift enable to set the channel B data output. The data shift output enables the 5-MHz clock circuit. The clock frequency circuit then permits the memory clock to be driven by a 5-MHz clock. The memory clock now generates a dual-phase memory clock at 2.5-MHz per line. This provides the combined 5-MHz clock required to step the video data through the memory.

g. When the control bit is stepped into the final stage of the memory, the associated input is inactive, terminating the memory shift sequence and initiating memory wait time. The control bit B signal generates the compressor output ready signal to the DC. The control bit B signal also resets the channel B data shift latch, temporarily terminating the 5-MHz memory clock. Timing and control now waits for the DC to indicate that the stored radar video sweep data may be output to the DG.

h. The sweep active signal initiates the memory output sequence. This signal sets the channel B data output, enabling the 5-MHz clock circuit. The channel output enable and the channel A output time inform the memory and the range mark and azimuth generator, respectively, that an output sequence is in progress. The memory clock then generates the dual-phase, 5-MHz clock required to transfer the compressed video data through the memory and to the DG. The memory output sequence is terminated when the control bit line resets the channel B data output and the 5-MHz clock circuit. The 5-MHz memory clocks are now terminated and timing and control is prepared for the next channel B input operation.

i. In the compressor bypass mode, the load enable signal and memory clocks to the memory are inhibited. In this mode, the memory is bypassed and data is supplied directly to the output summing gates.

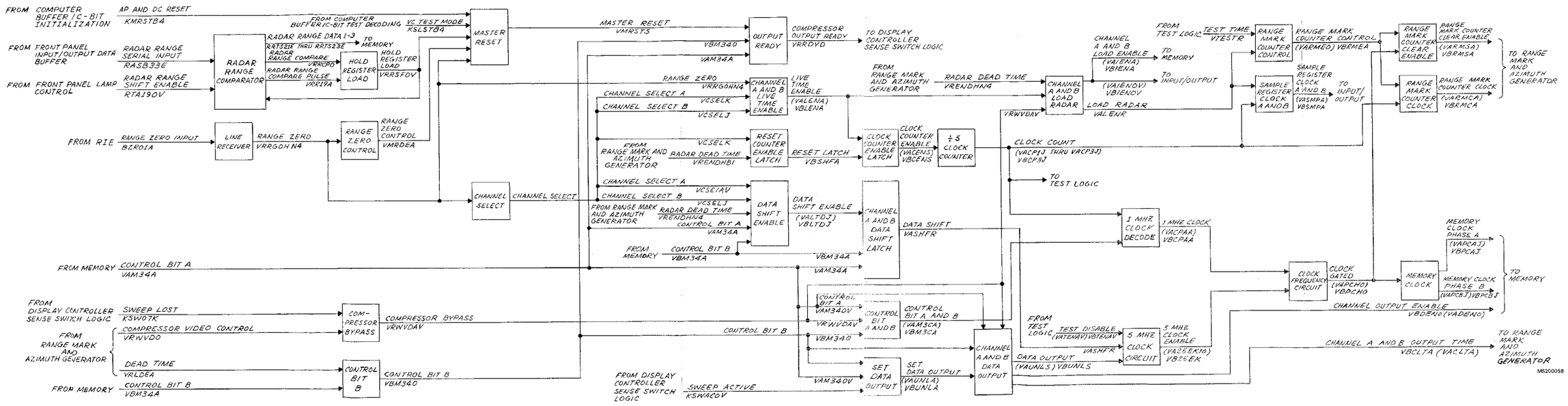


Figure 5-55. Timing and Control Block Diagram

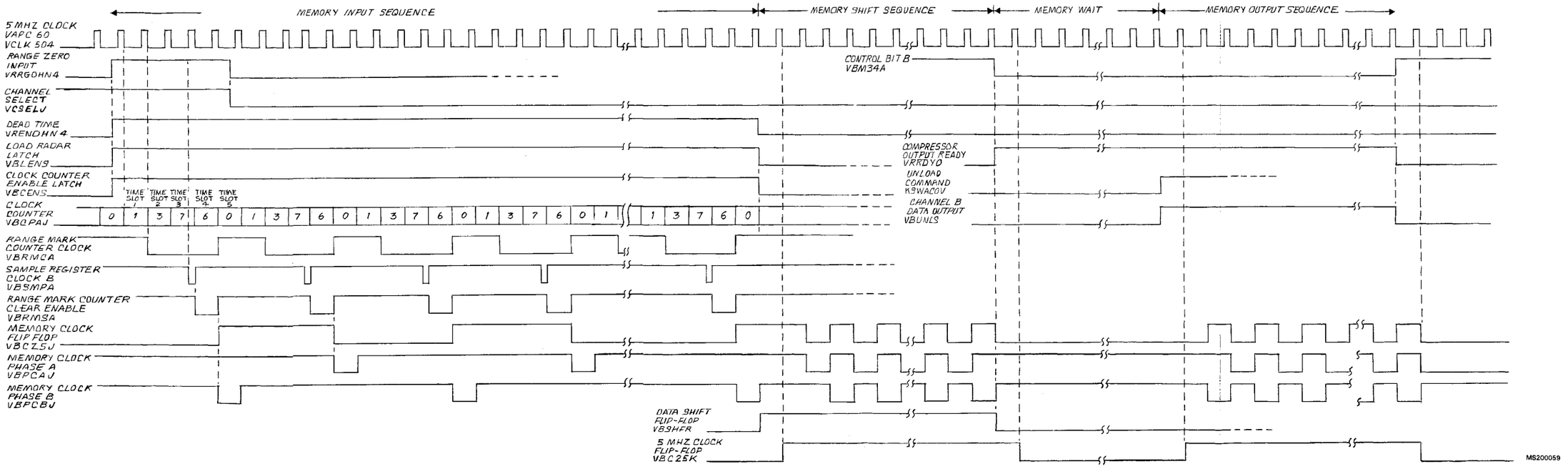


Figure 5-56. Timing and Control Timing Diagram

Section VII. DISPLAY GENERATOR

5-37. General (fig. 5-57). The main function of the DG is painting lines, symbols, characters. radar, and IFF video on the display console crt in accordance with signals received from the DC, VC, and front panel logic. (Another function, which is to interface with the computer buffer/C-BIT circuitry for test control data, is discussed under the computer buffer/C-BIT description.) The DG consists of four sections: line generator, character generator, video subsystem, and deflection subsystem. These are described in subparagraphs a thru d below.

a. *Line Generator.* The function of the line generator is X and Y crt beam positioning and painting lines and radar video on the crt. Digital information supplied by the DC high speed output buffer to the line generator consists of X and Y position and line and sweep data. This data, which is sent over a 16-bit data bus, consists of 12 bits for sweep rate and 4 bits for sweep range. Data from the high speed buffer to the line generator is controlled by signals from the DC low speed output buffer. The control signals consist of load display data, start of line, sweep enable, and tab start. After the digital information has been loaded into the line generator, the line generator processes and converts the data to analog deflection signals for the deflection subsystem and to digital video enable signals for the video subsystem. The line generator also generates a sweep compensation bit that is sent to the video subsystem to compensate for the writing rate difference between compressed and non-compressed radar video. A live time signal is sent to the line generator from the video compressor to initiate and terminate the sweep painting process on the crt. When video or lines are being painted on the crt, a sweep active signal is sent back to the DC by the line generator.

b. C*haracter Generator.* The character generator generates character and symbol information for display on the crt. The DC high speed output buffer data bus supplies a 7-bit ASCII code and a library symbol code to the character generator. The character generator converts each code into image writing instructions that paint the designated character or symbol on the crt by a successive number of small, straight-line, painted strokes. The DC low speed output buffer sends a start-of character (SOC) signal to the character generator which starts the character generator processing at the same time the ASCII code appears on the data bus. After the SOC signal is received, the character generator sends back to the DC (through the line generator) a tab or character active signal, indicating that the character is being painted on the crt. The character generator, upon completing a stroke of a character or symbol, sends an analog deflection signal to the deflection subsystem, and a character enable signal to the video subsystem. Once the character is completed, the tab or character active signal to the DC is inhibited.

c. Video Subsystem. The video subsystem displays video on the crt. The DC high speed data bus supplies nine channels of data to the video subsystem for processing. Synthetic data is contained on eight channels and radar video is contained on one channel. Synthetic data and radar video intensity is varied from front panel selected controls. The DC also generates a synthetic data control word over the high speed data bus which consists of 16 data bits: 9 bits for channel select, 4 bits for compensation, 2 bits for fault detection, and 1 bit for dash-line control. The video subsystem accepts the control word when a load control word is sent from the DC low speed output buffer. Radar video information received from the VC is a 3-bit digital signal representing eight intensity levels. When a radar sweep is present on the crt, the video subsystem sums the sweep and radar video inputs. Three video enable inputs arc provided from the line and character generators. The video enable signals arc converted by the video subsystem to analog output signals to drive the crt cathode.

d. *Deflection Subsystem.* The deflection subsystem sums and amplifies the X and Y analog information from the line and character generators and displays the result on the crt. The deflection subsystem also performs linearity correction to compensate for distortion on the crt.

5-38. Line Generator Detailed Description (fig. 5-58, FO-37) The line generator consists of the following elements:

Sweep range register
Radar clock rate multiplier
Control decode
Line/sweep clock control logic
Length counter
Line active control logic
Line/sweep video control logic
X and Y rate multipliers
X and Y range rate multipliers
X and Y position counters
X and Y digilog
Compensation counter
Tabular clock enable logic
X and Y tab counter and enable logic
X and Y clock gates

a. During the line-painting function, the line generator receives three types of data lines from the DC high speed data bus: start of line position data, which is loaded into the X and Y position counters; line direction data, which is loaded into the X and Y rate multipliers; and length of line data, which is loaded into the length counter. After the line data is loaded, the active control

logic receives a start of line signal through the control decoder. The line active control logic, upon receiving the start of line signal, outputs a video enable signal to the line/sweep video control logic, a start length count signal to the length counter, and a live clock rate multiplier enable signal to the X and Y rate multiplier. The video enable signal allows the video subsystem to turn on the crt beam, and the live clock rate multiplier cnabic signal allows the line clock, from the line/sweep clock control logic, to start incrementing the X and Y rate multipliers. The X and Y rate multipliers multiply the incoming line clock (approximately 20 MHz) to submultiple frequencies, with plus or minus sign, and produce the X and Y rate clocks to drive the X and Y position counters. The changing values on the X and Y position counters are applied to the X and Y digilogs for analog conversion. The X and Y digilogs send the analog X and Y signals to the deflection subsystem, starting a line to be painted across the crt. During the line painting function, the range rate multipliers have no effect on the X and Y rate clock frequencies. As a line is being painted on the crt, the length counter designates when the line has reached proper length and sends back to the line active control logic a length count complete signal. The line active control logic then inhibits both the video enable signal to the video subsystem and the line clock, which completes the line painting function.

b. During the radar video painting function, the line generator receives radar video data from the DC high speed data bus. The radar video data represents: start of line position data (the origin), which is loaded into the X and Y position counters; line direction data, which is loaded into the X and Y rate multipliers; range selection data, which is loaded into the sweep range register; clock rate multiplier data, which is loaded into the radar clock rate multiplier; and I compensation data bit, which is loaded into the compensation counter. The compensation data bit and video compressed/non-compressed compensation signals, from the line/sweep clock control logic and control decoder, are used to provide sweep compensation to the video subsystem. After the radar video data is loaded, the range selection data is transferred from the sweep range register and stored in the X and Y range rate multipliers.

c. The line/sweep clock control logic receives sweep enable signals from the DC and live time signals from the VC. After the signals are received, the line/sweep control logic selects the sweep rate clock frequency for the line clock and sends a sweep active signal to the DC. The sweep rate clock frequency is a 10-MHz clock signal that is frequency-multiplied by the radar clock rate multiplier to the particular submultiple frequency required by the line clock. The line/sweep control logic then sends a live time sweep active signal to the line active control logic, which enables the line clock to drive the X and Y position counters through the X and Y rate and range rate multipliers. The X and Y range rate multipliers multiply the line frequency to submultiple rate clock frequencies. The X and Y position counters then output X and Y position data to the X and Y digilogs for analog conversion. The X and Y digilogs send the analog signals to the deflection subsystem, starting painting of radar video. On receiving the live time sweep active signal, the line active control logic also sends a video enable signal through the line/sweep video control logic to the video subsystem. The video enable signal turns on the crt beam.

d. The line/sweep video control logic monitors the position counters and automatically inhibits the video enable signal when the position counters reach the full count value. The inhibited video enable signal turns off the crt beam. When the live time signal is terminated by the VC, the X and Y position counters arc inhibited. This action terminates the sweep active signal to the DC, completing the radar video painting function.

e. When the line generator performs the tabular positioning function (tabular A/N spacing), the X and Y position counters are directly incremented by a clock control signal from the tabular clock enable logic. The tabular positioning function starts with the X and Y position counters already positioned at certain values. Count data corresponding to tabular incremental X and Y crt relocation is then loaded into the X and Y tab counters. Upon receiving a start tab signal from the DC, the tabular clock enable logic is enabled; however, the tabular clock enable logic will remain inhibited as long as the character active signal is present. Once the character active signal terminates, the X and Y tab counters are enabled and serve as timers by counting towards the previously loaded preset count values. When the X and Y tab counters are counting, the associated X and Y clock gates enable the clock frequency to increment the X and Y position counters. As the tab counters reach the preset count, the counters shut down and the X and Y clock gates inhibit the position counter from being incremented. The position counters will now be at a new tab position value. When the character active signal is present or the line generator is being placed at a new tabular position, a tab/character active signal will be sent to the DC.

5-39. Character Generator Detailed Description (fig 5-59, FO-38). The character generator consists of the following elements:
Address decoder
Stroke counter
Stroke data word memory
X and Y enable and range decoder
Buffer register
Character enable and reset logic
Modulo 3 counter
Range counter
Clock decoder
Z-axis delay
X and Y axis clock decoder

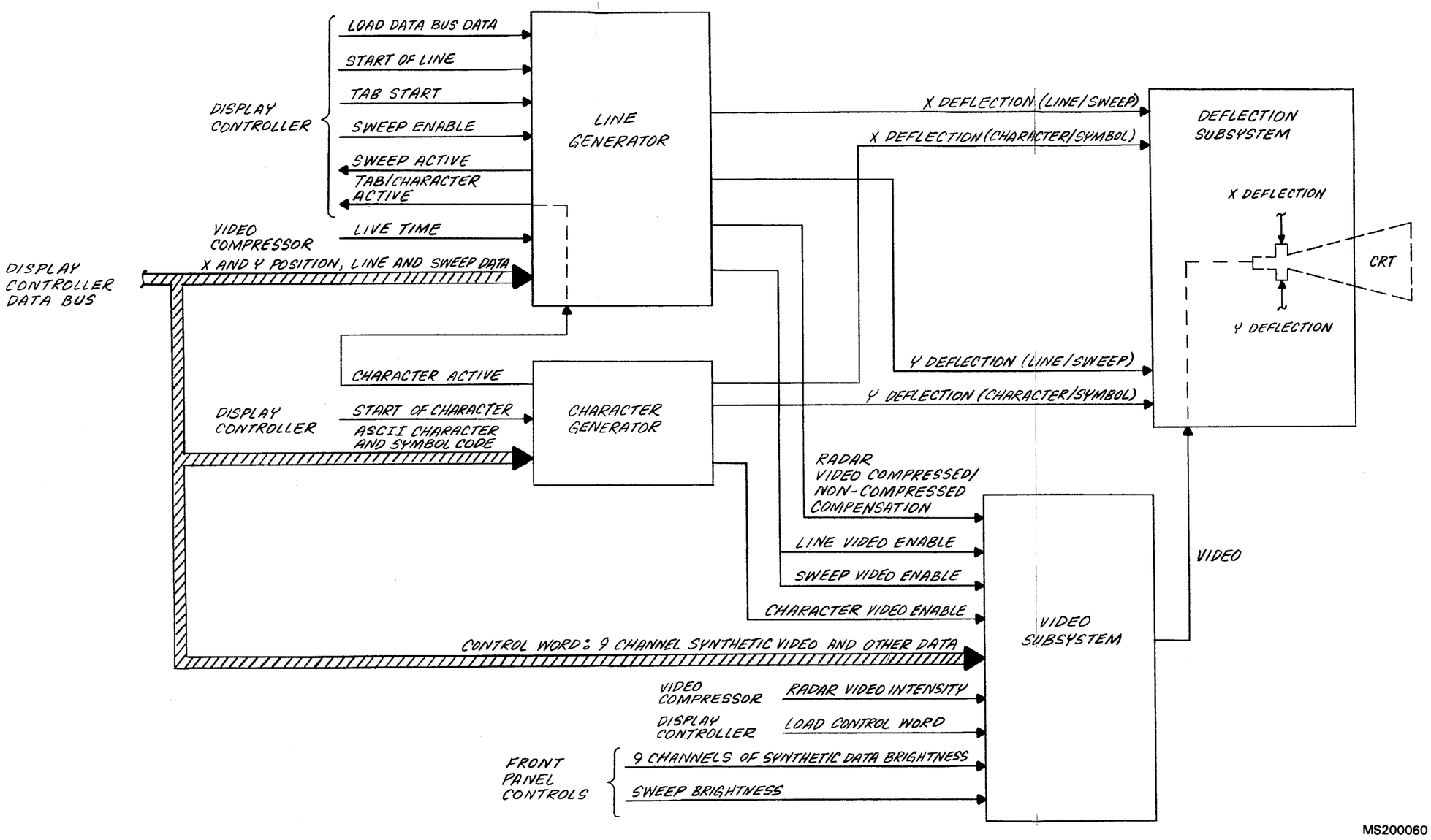


Figure 5-57. Display Generator Block Diagram

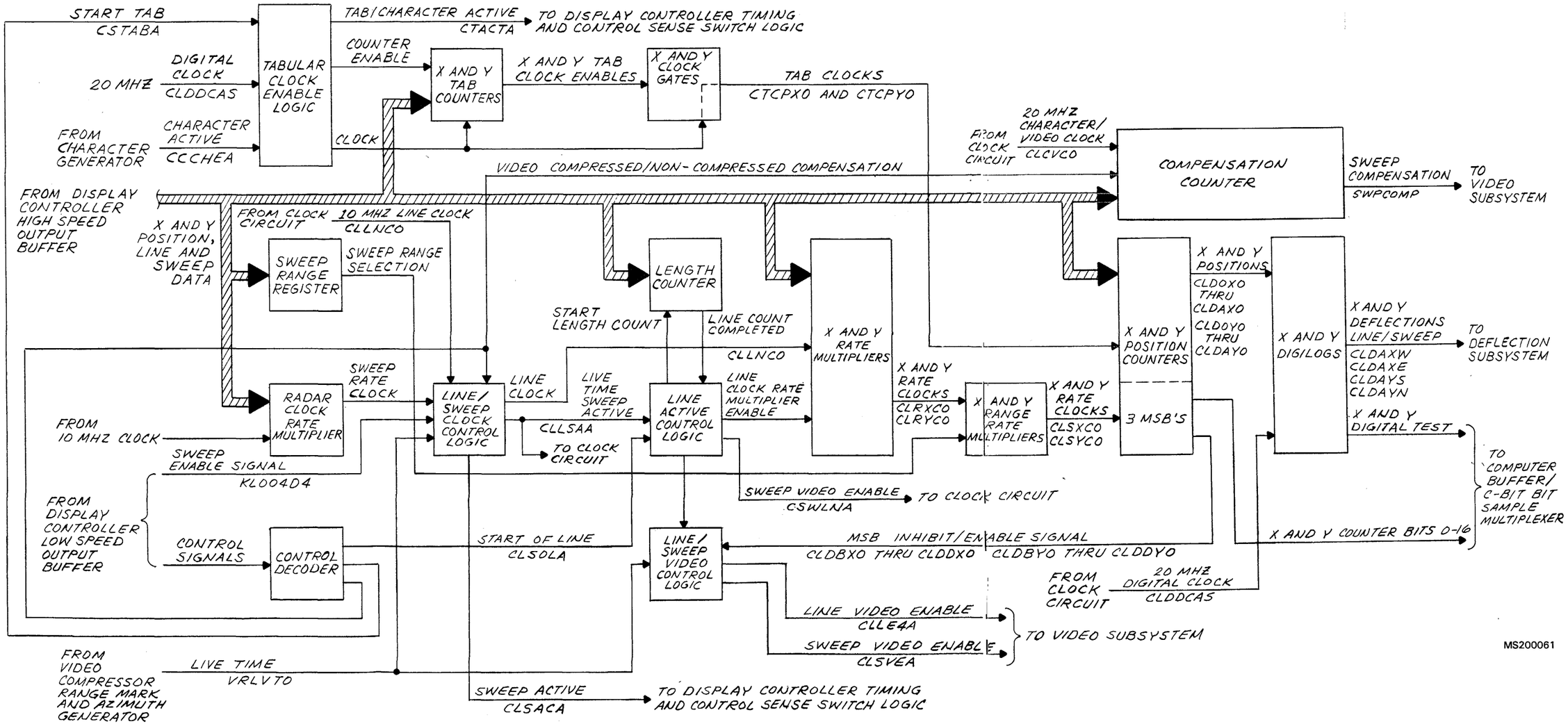


Figure 5-58. Line Generator Block Diagram

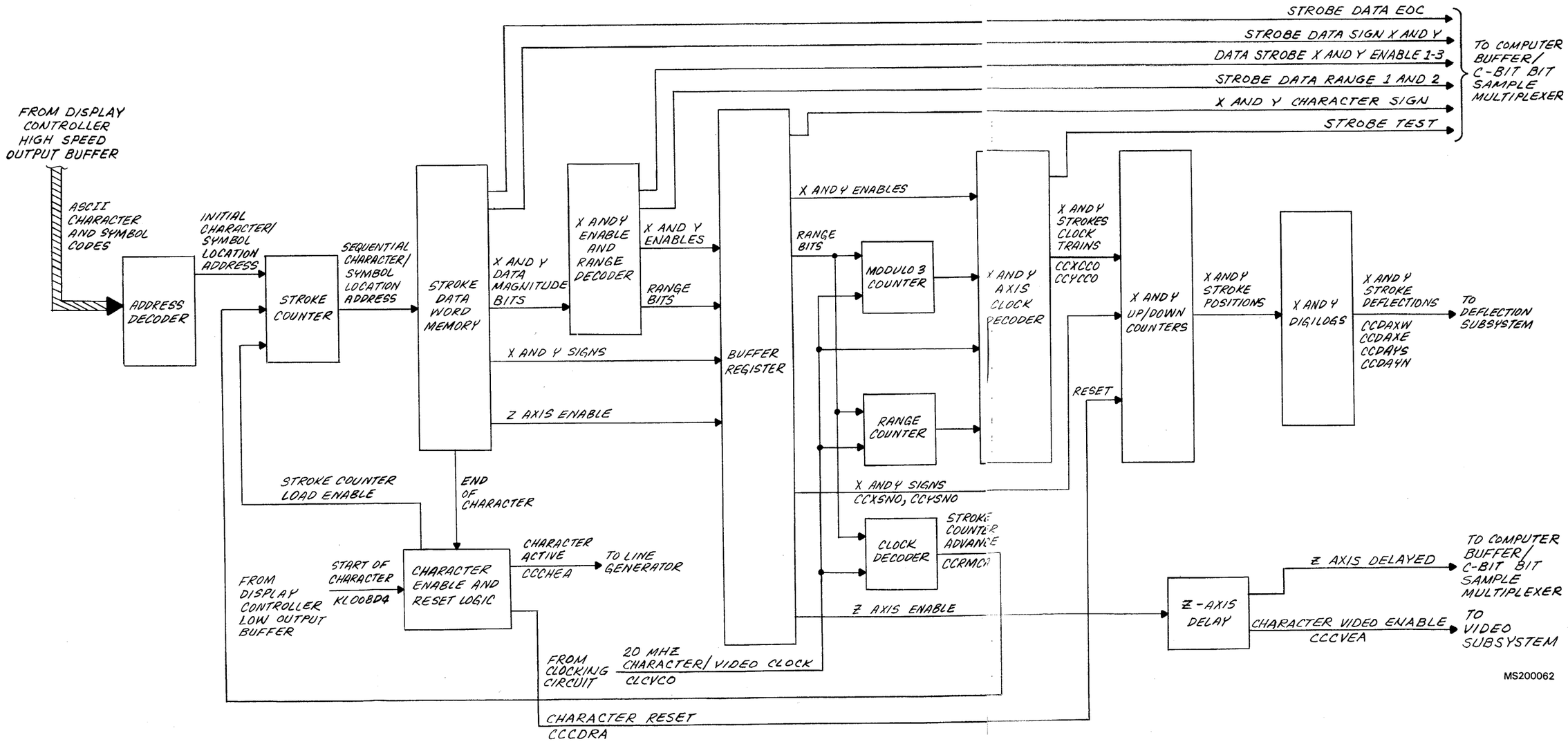


Figure 5-59. Character Generator Block Diagram

X and Y up/down counters
X and Y digilogs

a. The character/symbol painting function begins when the character enable and reset logic receives an SOC signal from the DC low speed output buffer. After receiving the signal, the character enable and reset logic sends a load enable signal to the stroke counter and a character active signal to the line generator. Upon receiving the load enable signal, the stroke counter loads the character/symbol location address from the address decoder and increments through each stroke of a given character or symbol. The address decoder is used to translate incoming ASCII or library codes, from the high-speed data bus, into a character/symbol location address, which determines the location of the first stroke of each character or symbol in the stroke data memory. Each location in the stroke data memory consists of an 8-bit stroke data word, which contains the following: X magnitude bits X1 and X2; Y magnitude bits Y1 and Y2; X and Y sign bits; Z-axis enable bit; and an end of character (EOC) bit. Figure 5-60 illustrates the stroke data word writing instruction format for characters A, B, C, and D. As an example, the character A has seven strokes that correspond to seven consecutive stroke data words listed. The X and Y magnitude bits (X1, X2, Y1, and Y2) in each stroke data word are converted by the X and Y enable and range decoder into X and Y enables and range bits. The X and Y enables and range bits (after decoding) represent the required X and Y displacement of the crt beam for a given stroke. The X and Y enables and range bits, along with the X and Y sign bits and Z-axis bit, are stored in the buffer register. The EOC bit is sent to the character enable and reset logic to wait until the last stroke data word is accessed from the stroke data word memory. The X and Y enables and range bits are decoded into clock trains by the modulo 3 counter, range counter, and X and Y axis clock decoder. The X and Y stroke clock trains and X and Y sign bits are used to increment the X and Y up/down counter, which starts the crt beam painting the first stroke. Table 5-29 identifies the decoding of the X_2, X_1, Y_2, and Y_1 bits into the maximum number of clocks for each range and includes the proper number of clocks for each of the 16 stroke combinations. The analog voltage for the X and Y axis varies as the X or Y up/down counter is incremented. Figure 5-61 illustrates the variations for clock ranges 4, 8, and 12. During the clock train generation process, the Z-axis bit is clocked through the Z-axis delay to generate a character video enable (video inhibit) signal to the video subsystem, which turns on the crt beam for the first stroke duration. The video enable signal must be delayed 50 ns to compensate for inherent delays in the deflection subsystem. The clock decoder, upon detecting the end of a clock train cycle (stroke), sends a stroke counter advance signal to the stroke counter. The stroke counter then sends the next character/symbol location address to the stroke data word memory.

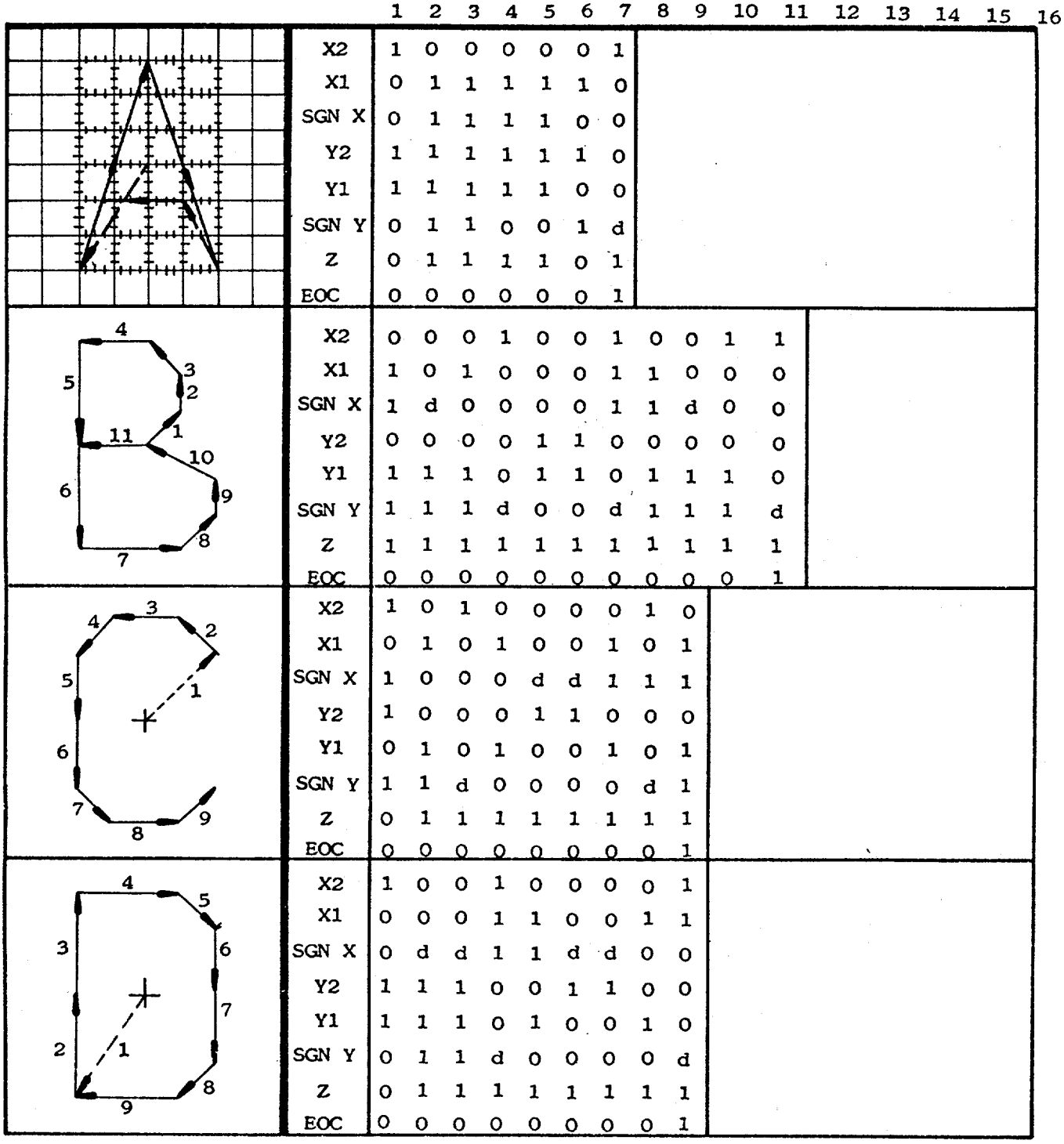
b. The digital values set in the X and Y counters are constantly monitored by the X and Y digilogs. The X and Y digilogs convert the X and Y counter digital data into analog signals that drive the deflection subsystem. The deflection subsystem uses the sum of both the line generator and the character generator output analog signals to position the crt beam.

c. After the first word is processed, the character generator continues to process each data word in the same manner as the first until the last required stroke of a character or symbol is painted on the crt. At the completion of a character or symbol, the character enable and reset logic detects that the EOC bit has been set and the character generation process has stopped. Upon receiving the EOC bit, the character enable and reset logic inhibits the character active signal to the line generator and sends a character reset signal to the X and Y up/down counters. The video enable signal to the video subsystem is also turned off, ending the character/symbol generation process.

5-40. Video Subsystem Detailed Description (fig. 5-62, FO-39). The video subsystem consists of the following elements:

Video enable logic
Radar data buffer gates
Radar D/A converter
Summing amplifier
Amplitude and offset controls
Video amplifier
Buffer amplifier
Voltage multiplier
Video compensation D/A converter
Video select switch
Input register

The video subsystem is a nine-channel video multiplexer that selects, conditions, and amplifies video input data to drive the cathode of the crt. Video selection is accomplished by means of a 16-bit control word and enable signals from the line and character generators. The 16-bit control word is loaded from the DC high speed data bus into the input register. The control word consists of the following: 9 bits for video channel select; 4 bits for writing rate compensation; I bit for dash line control; and 2 bits for fault detection. The input register delivers 9-bit video channel select data to the video select switch which selects one of the nine intensity controlled video inputs from the front panel. Each of the video inputs is a source voltage that is intensity controlled to a certain voltage level by a 10-position, manually-operated thumbwheel voltage divider on the front panel. The nine intensity controlled video inputs correspond to eight synthetic video channels and one radar sweep channel. The video select switch also receives a signal from the line generator that compensates for time differences between compressed and noncompressed radar video.



d = Don't care

MS200063

Figure 5-60. Stroke Data Word Writing Instruction Format

Table 5-29. Stroke Information Decode

	X_2	X_1	Y_2	Y_1	XE_1	XE_2	XE_3	YE_1	YE_2	YE_3	R_1	R_2	Range counter		X Clock range	Y Clock range
0	0	0	0	0	0	d	0	0	d	0	0	0	4	clocks	0/4	0/4
1	0	0	0	1	0	d	0	0[d]	d	1	0	0	4		0/4	0/4
2	0	0	1	0	0	d	0	0[d]	d	1	0	1	8		0/8	8/8
3	0	0	1	1	0	0	0	0[d]	1	1	1	0	12		0/12	12/12
4	0	1	0	0	0[d]	d	1	0	d	0	0	0	4		4/4	0/4
5	0	1	0	1	0[d]	d	1	0[d]	d	1	0	0	4		4/4	4/4
6	0	1	1	0	1	d	0	0[d]	d	1	0	1	8		4/8	8/8
7	0	1	1	1	0	1	0	0[d]	1	1	1	0	12		4/12	12/12
8	1	0	0	0	0[d]	d	1	0	d	0	0	1	8		8/8	0/8
9	1	0	0	1	0[d]	d	1	1	d	0	0	1	8		8/8	4/8
10	1	0	1	0	0[d]	d	1	0[d]	d	1	0	1	8		8/8	8/8
11	1	0	1	1	0	0	1	0[d]	1	1	1	0	12		8/12	12/12
12	1	1	0	0	0[d]	1	1	0	0	0	1	0	12		12/12	0/12
13	1	1	0	1	0[d]	1	1	0	1	0	1	0	12		12/12	4/12
14	1	1	1	0	0[d]	1	1	0	0	1	1	0	12		12/12	8/12
15	1	1	1	1	0[d]	1	1	0[d]	1	1	1	0	12	clocks	12/12	12/12

d = Don't care

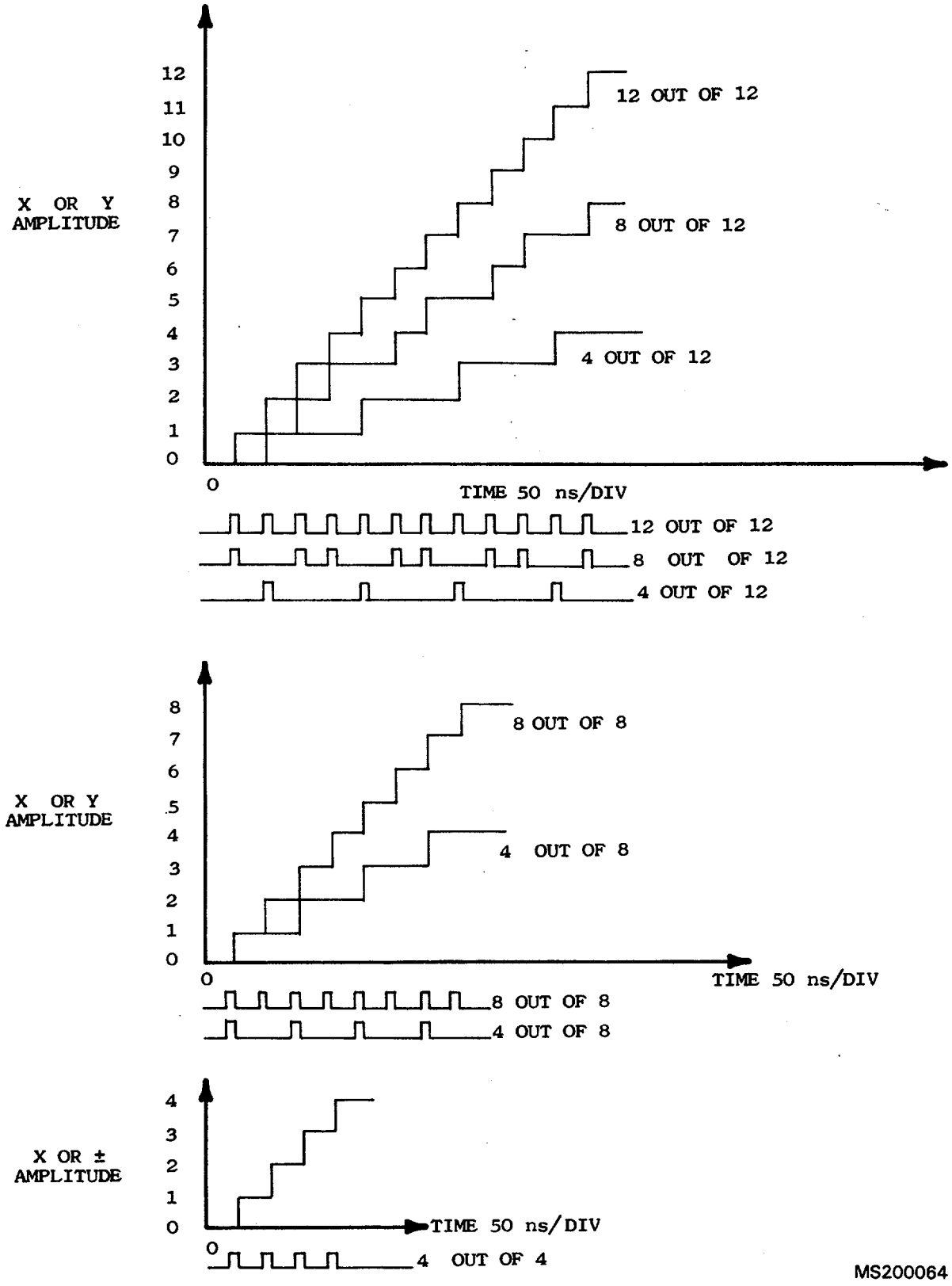


Figure 5-61. X/Y Amplitude

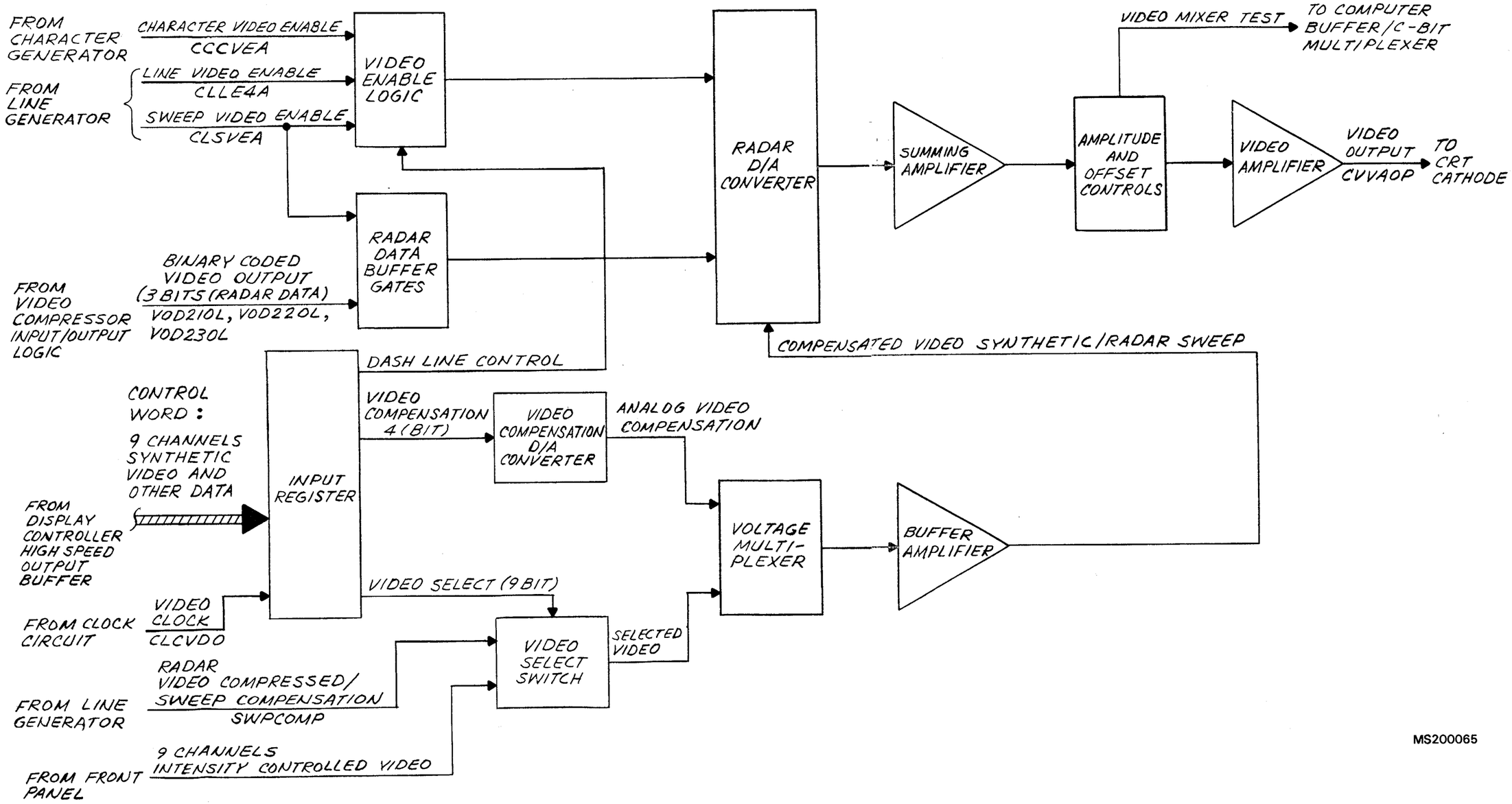


Figure 5-62. Video Subsystem Block Diagram

a. The intensity controlled video input selected by the video select switch is fed to the voltage mux, which is controlled by the video compensation digital-to-analog (D/A) converter. The control word 4-bit compensation data, which was stored in the input register, is converted into analog form by the video compensation D/A converter for controlling the voltage multiplier. The voltage multiplier output is applied through a buffer amplifier and is used to vary the current source of the radar D/A converter MSB to provide intensity adjust- ment and compensation for the video signal. The radar D/A converter is controlled by enable signals received by the video enable logic and, when applicable, the 3 bits of incoming radar data sampled by the radar data buffer gates. During the processing of radar sweep data, the sweep intensity-controlled video input is selected for processing. The sweep enable signal is applied to the video enable logic and the radar data buffer gates. The radar buffer gates, upon receiving the sweep enable signal, allow the 3 bits of radar data from the VC to be fed into the radar D/A converter. The 3 bits of radar data are converted by the radar D/A converter into eight radar video intensity levels. The summing amplifier sums and amplifies the output signals from the radar D/A converter into a composite video signal. The video signal is then adjusted by the amplitude and offset controls for the proper magnitude and offset, amplified by the video amplifier, and fed to the crt cathode.

b. Synthetic video data is processed similar to radar sweep data, with the following exceptions: the control word selects one of the eight synthetic intensity-controlled video inputs for processing; either a line enable or a character video enable signal is received by the video enable logic; and the binary coded video output (3 bits of radar data) are inhibited from being fed to the radar D/A converter.

c. Dashed lines are created on the crt by a control word dash line control bit, which is sent to the video enable logic from the input register. After the video enable logic has received a line enable signal from the line generator, the dash line control bit periodically inhibits the video enable logic, causing a dashed line to be painted on the crt.

5-41. Deflection Subsystem Detailed Description (fig. 5-63, FO-40). The deflection subsystem consists of the following elements:

Gain switch data buffer register
Y offset data buffer register
X summation amplifier
Y summation amplifier
Linearity corrector
X deflection amplifier
Y deflection amplifier

a. *X and Y Summation Amplifiers.* The X and Y summation amplifiers sum and amplify the analog voltages from the line and character generators. The X and Y summation amplifier outputs drive the X and Y deflection amplifiers. The hook marker gain increase and ARO Y offset enable signals from the DC are stored in the gain switch data buffer and the Y offset data buffer registers. The enable signals, when supplied to the X and Y summation amplifiers, change the amplifiers' gain and offset adjustment. Gain changing is performed in the X and Y summation amplifiers to paint a hook marker on the crt. Upon receiving the hook marker gain increase enable signal, the X and Y summation amplifiers switch from low gain to high gain, causing a larger hook marker symbol to be painted. The ARO Y offset enable signal causes an offset adjustment in the Y summation amplifier only. The purpose of the offset adjustment is to offset the Y-axis beam position to the alphanumeric readout (ARO) on the crt. The X and Y summation amplifiers use a linearity correction feedback loop to compensate for the pincushion distortion characteristic of the crt. The feedback loop processes the summation amplifier outputs through $X(X^2 + Y^2)$ and $Y(X^2 + Y^2)$ functions to achieve vector linearity and reduce pincushion distortion.

b. *X and Y Deflection Amplifiers.* The X and Y deflection amplifiers convert the X and Y summation amplifier voltage outputs into current levels required by the crt yoke to position the beam at a corresponding location on the crt. The X and Y deflection amplifiers maintain linear small signal response, offsetting the beam on the crt. The amplifiers also automatically switch to higher power supply voltages to ensure that large beam movements will take place at a rapid rate. The X and Y deflection amplifiers provide a deflection active signal to the DC. The deflection active signal indicates the time required to assume a new output value before system operation continues.

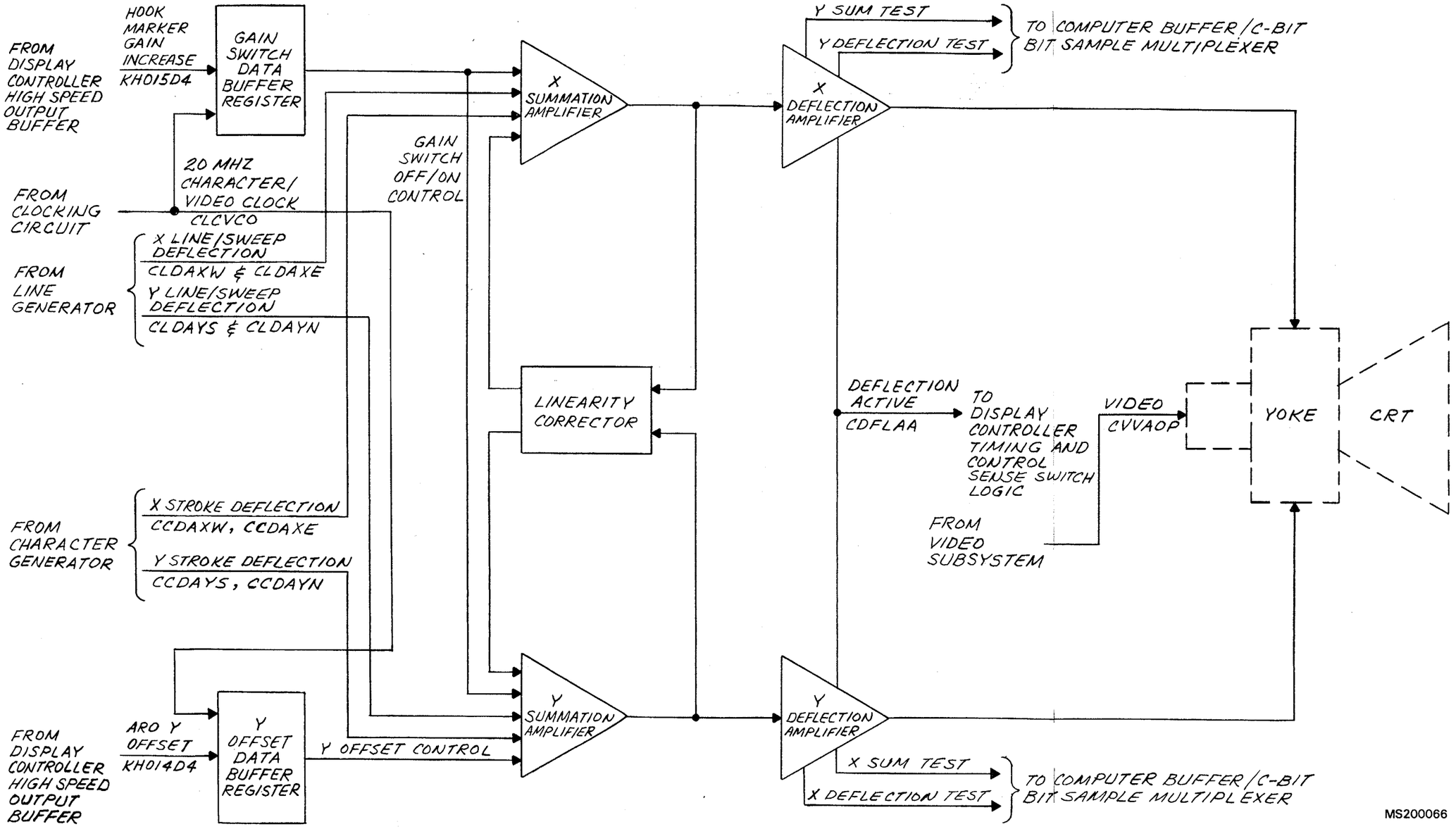


Figure 5-63. Deflection Subsystem Block Diagram

Section VIII. FRONT PANEL LOGIC

5-42. General (fig. 5-64). The main function of the front panel logic is to sense front panel operator actions and process the interchange of control signals and data between the AP, VC, and DC. Six categories of data are processed by the front panel: force stick deflection, variable scale setting, AN keyboard selection, time-to-go setting, switch action, and lamp lighting. The front panel logic operates in an input or output mode which is controlled by the AP. The front panel logic consists of six sections: lamp control, I/O control, AP data select, switch coding, data multiplexing, and I/O data buffer register. These are described in subparagraphs a thru f.

a. *Lamp Control.* The function of lamp control is to process current lamp data, update interfacing signals to the VC and DC, and light or turn off the appropriate indicators on the display console front panels. During the input mode, lamp control receives command word data from the I/O data buffer register which prepares lamp control to output lamp serial data to the AP data select. Upon receiving a control signal from the I/O control, lamp control outputs the lamp serial data. Lamp control also lights or turns off appropriate display console front panel indicators and updates the enable, timing and control, and range control signals to the VC and a range control signal to the DC. During the output mode, lamp control also receives command word data from the I/O data buffer register, and upon receiving a control signal from the I/O control, stores current lamp serial data.

b. *I/O Control.* I/O control performs the transfer of data words between the front panel logic and the AP. During the input mode, two successive command signals are received by I/O control. These command signals allow the I/O control to initiate control signals to the I/O data buffer register, lamp control, switch coding, or data multiplexing for selection of data to be transferred. After receiving the command signals from the AP, the I/O control sends a request signal to the AP indicating that data is ready to be sent. Upon receiving the request signal, the AP accepts the data and sends an enable signal back to I/O control placing the I/O control in a standby condition, thereby terminating the request signal. In the output mode, the I/O control receives a command signal from the AP which is for lamp data transfer. Upon receiving the command signal, the I/O control sends a control signal to lamp control. The command signal prepares lamp control to receive lamp data. After lamp control has been prepared, the I/O control sends a request signal to the AP indicating that the front panel logic is ready to receive lamp data. Upon receiving the request signal, the AP sends an enable signal back to the I/O control, terminating the request signal and placing the I/O control in a standby condition.

c. *AP Data Select.* The function of AP data select is to select one of six data sources from lamp control, switch coding, or data multiplexing, and transfer the panel selected serial data into the I/O data buffer register. The AP data select only operates in the input mode of operation. When the AP data select receives command word data from the I/O data buffer register and a control signal from the I/O control, lamp serial data is selected to be sent to the I/O data register. If no lamp serial data is to be sent to the AP data select, the AP data select sends preselected switch, force stick, variable scale, AN keyboard, or time-to-go serial data to the I/O data buffer register from switch coding or data multiplexing.

d. *Switch Coding.* The switch coding function is used to determine whether a switch is pressed and outputs the switch serial data corresponding to that switch to the AP. Switch coding only operates in the input mode of operation. During the input mode of operation, I/O control sends a control signal to switch coding requesting switch data to be sent to the AP. Upon receiving the control signal, switch coding outputs the switch serial data to the AP data select. When switch serial data is sent to the AP data select, data multiplexing inhibits the AN keyboard serial data.

e. *Data Multiplexing.* Data multiplexing generates serial data words for the force stick, variable scale, AN keyboard, and time-to-go data sources. Data multiplexing only operates in the input mode of operation. During the input mode of operation, data multiplexing receives a control signal from I/O control requesting force stick, variable scale, AN keyboard, or time-to-go serial data to be sent to AP data select for output to the alterable processor. The AN keyboard serial data can only be sent to AP data select if no switch serial data is being sent from switch coding.

f. *I/O Data Buffer Register.* The function of the I/O data buffer register is to receive incoming command words from the AP and, after command word front panel processing, send or receive a data word to or from the AP. The command and data words are transferred over a 16-bit data bus. The command word, which is sent from the AP prior to the transfer to data, is used to designate the mode of operation and the type of serial data to be transferred. In the input mode, panel selected serial data or lamp status information is loaded into the I/O data register from the AP data select by a control signal from the I/O control. After the data is loaded, the data is read out in parallel on the 16-bit data bus to the AP. In the output mode, lamp data from the AP is loaded into the I/O data register in parallel from the 16-bit data bus by a control signal from the I/O control. After loading of lamp data, the lamp data is serially transferred to lamp control and data is transferred to the VC.

5-43. Lamp Control Detailed Description (fig. 5-65, FO-41). Lamp control consists of the following elements:
Lamp register
Input enable circuit
Output select
Select code
Decode circuit
Lamp decode
Lamp driver circuit
Data register
Front panel indicators

a. *Input Mode.* During the input mode, lamp control receives command word lamp group bits 9 thru 13 (inverted and noninverted) from the I/O data buffer register. The lamp group bits designate which 12-bit lamp data word is to be sent to output select from the lamp register and recirculated back into the lamp register. The lamp group bits are loaded into the select code by a mode enable signal from I/O control. The select code receives a select signal from I/O control which designates the input mode of operation. After receiving the select signal, the select code sends a data signal to the input enable circuit. The data signal designates the input mode with recirculation of the lamp data word. The input enable circuit inhibits the reading of a serial new lamp data word during the input mode. The select code then sends a lamp register selection code and a code enable signal to the decode circuit. The lamp register selection code designates which one of eighteen 12-bit lamp data words is to be shifted out of the lamp register and also if a timing and control signal is sent to the VC from the decode circuit. The decode circuit, after receiving the lamp register selection code and code enable signal, sends a shift enable signal to the lamp register. The shift enable signal allows the lamp register to shift out a 12-bit lamp data word to output select, and recirculate the lamp data word back into the lamp register through the input enable circuit. When the output select receives an enable and select code signal from select code, the output select transfers the lamp data word to AP data select. Lamp data sent to the output select is also used to light or turn off front panel indicators. Task function indicator data is decoded and amplified by the lamp decode and lamp drive circuit for output to the task function indicators. When the selection code selects one of the eighteen 12-bit lamp data words which contains 4 bits of DC and VC data, the data bits are sent to the data register. Upon receiving a load signal from the decode circuit, the data register will output the data. The selection code may also select one of the eighteen 12-bit data words which contains 7 bits of channel select VC data. The 7 bits of data is sent to the VC from the lamp register when a shift enable signal is received from the decode circuit. Upon receiving an inhibit signal from data multiplexing, the select code resets a part of the selection code to the decode circuit which inhibits the shifting of the lamp register.

b *Output Mode.* During the output mode, lamp control again receives command word lamp group bits 9 thru 13 from the I/O data buffer register which are loaded into select code by the mode enable signal from I/O control. In the output mode, the select signal from I/O control is inactive which designates the output mode. The select code sends a data signal to the input enable circuit which designates the output mode and inhibits the recirculation of the lamp data word. The select code then sends a selection code and a code enable signal to the decode circuit. In the output mode, the selection code selects which one of eighteen 12-bit storage areas in the lamp register the current lamp data will fill. The decode circuit then sends a shift enable signal to the lamp register which shifts in the current lamp data. Data multiplexing sends an inhibit signal to the select code, which resets a part of the selection code to the decode circuit and inhibits the shifting of the, lamp register.

5-44. Input/Output Control Detailed Description (fig. 5-66, FO-42). The I/O control consists of the following elements:
Command control
Output mode circuit
Request control
Input mode circuit

The I/O control accepts two control signals from the AP, the command signal and the enable signal, and sends two control signals to the AP, the request signal and the indicator signal. The interchange of these signals is shown in figure 5-67 for both the input and output mode. Prior to the interchange of control signals, command control receives a command bit I signal from the I/O data buffer register which enables the I/O control for data word I/O mode processing.

a. *Control Input Mode.* Command bit 15 from the I/O data buffer register enables the input mode circuit. Command bit 15 designates data word readout from all data sources except the lamp data sources. (Refer to paragraph 5-48, I/O data register detailed description, for command control formats.) When command control receives the first command signal from the AP, a mode enable signal is sent to the input mode circuit, which allows the input mode circuit to output a load enable signal, an enable data select signal, and an input mode signal. The load enable signal is supplied as follows: to data multiplexing for AN keyboard and switch selection; to switch coding for starting the switch coding process; and to AP data select for loading the data source select code (command word bits 9, 10, and 11). The enable data select signal is supplied to AP data select for input selection. The input mode signal is supplied to data multiplexing for initializing the data word count sequence. Upon receiving a second command signal from the AP, command control again sends a mode enable to the input mode control which transfers an input mode request signal to request control. The input mode request signal prepares request control for transferring a request

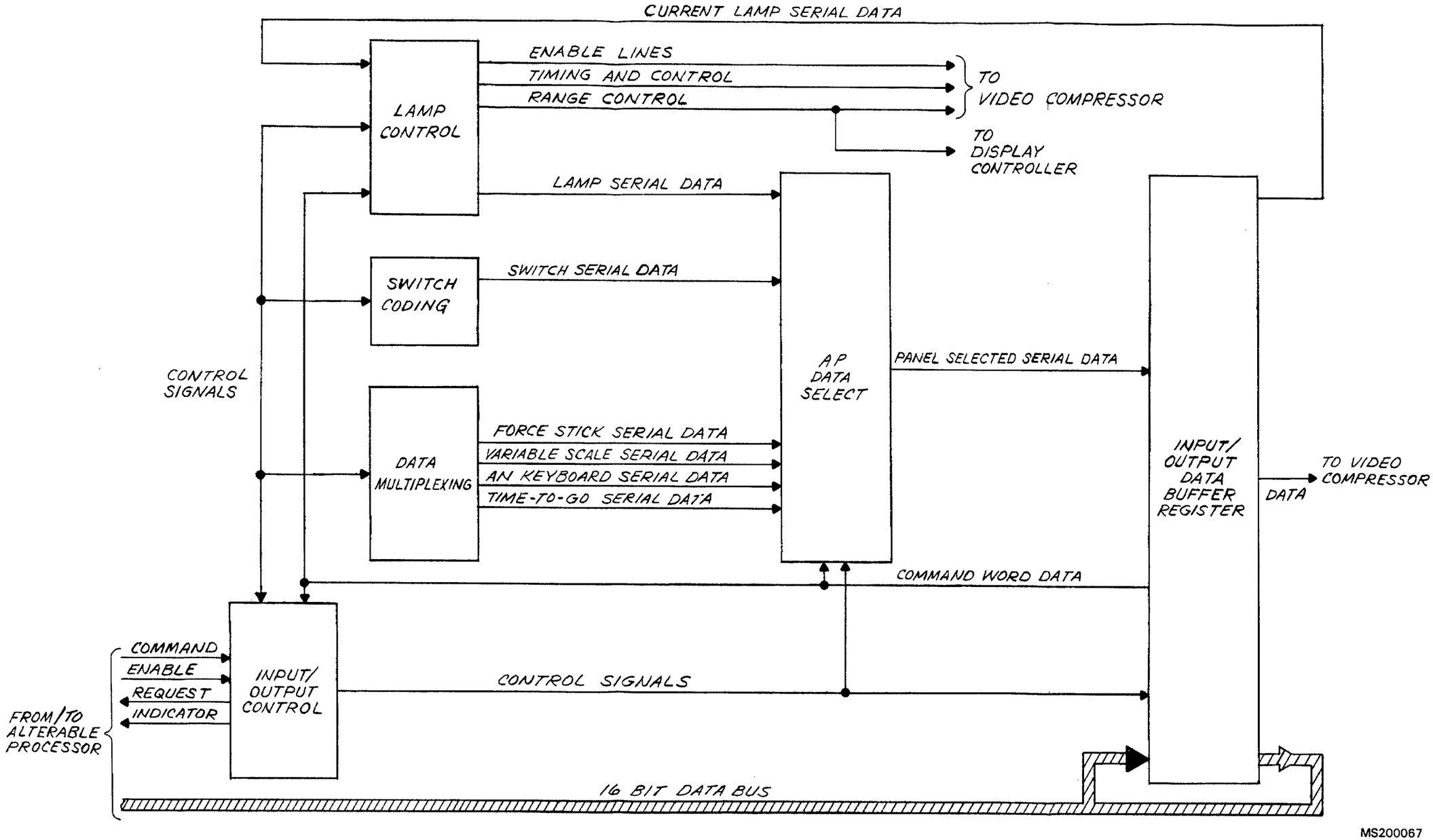


Figure 5-64. Front Panel Block Diagram

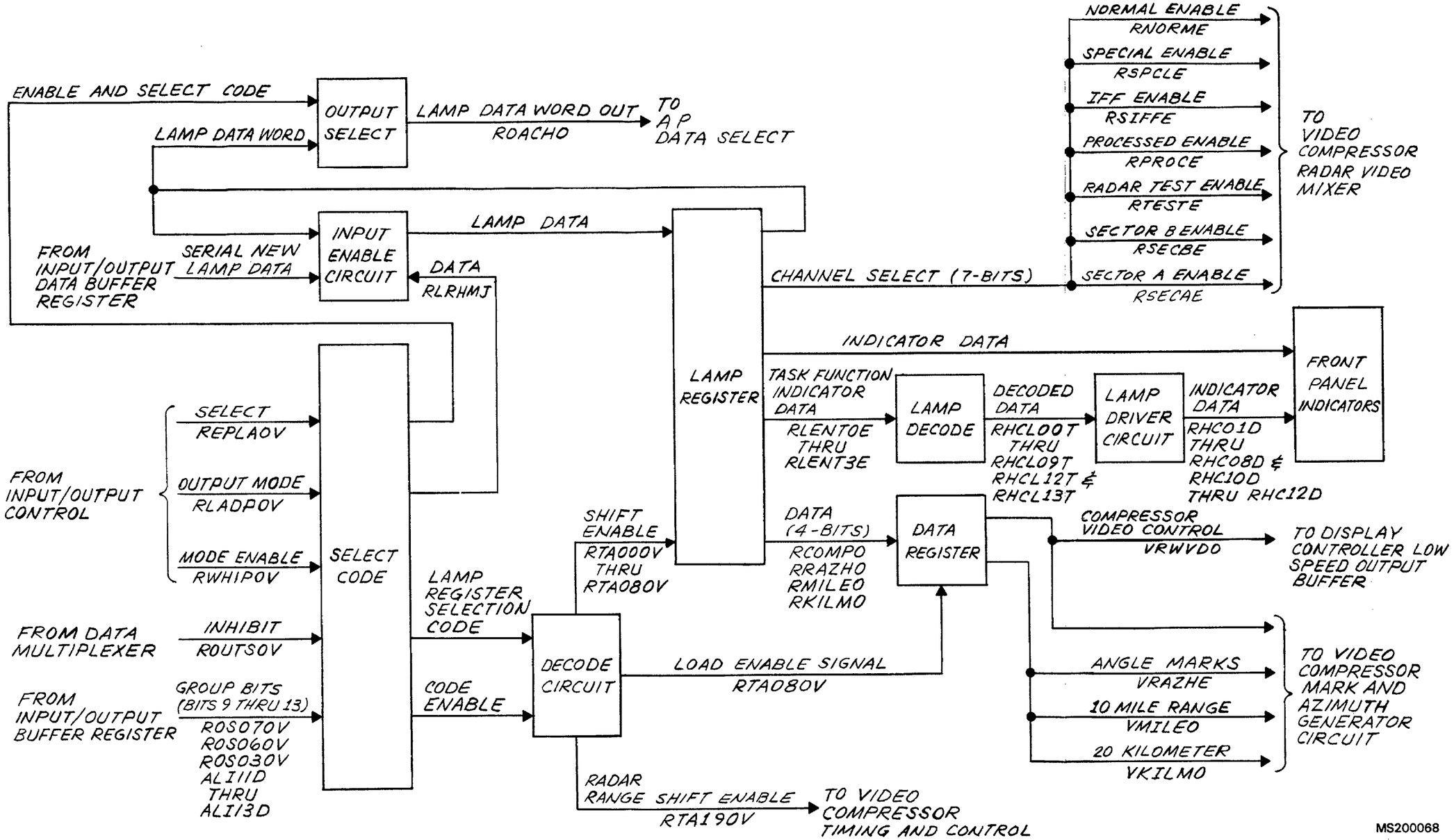


Figure 5-65. Lamp Control Block Diagram

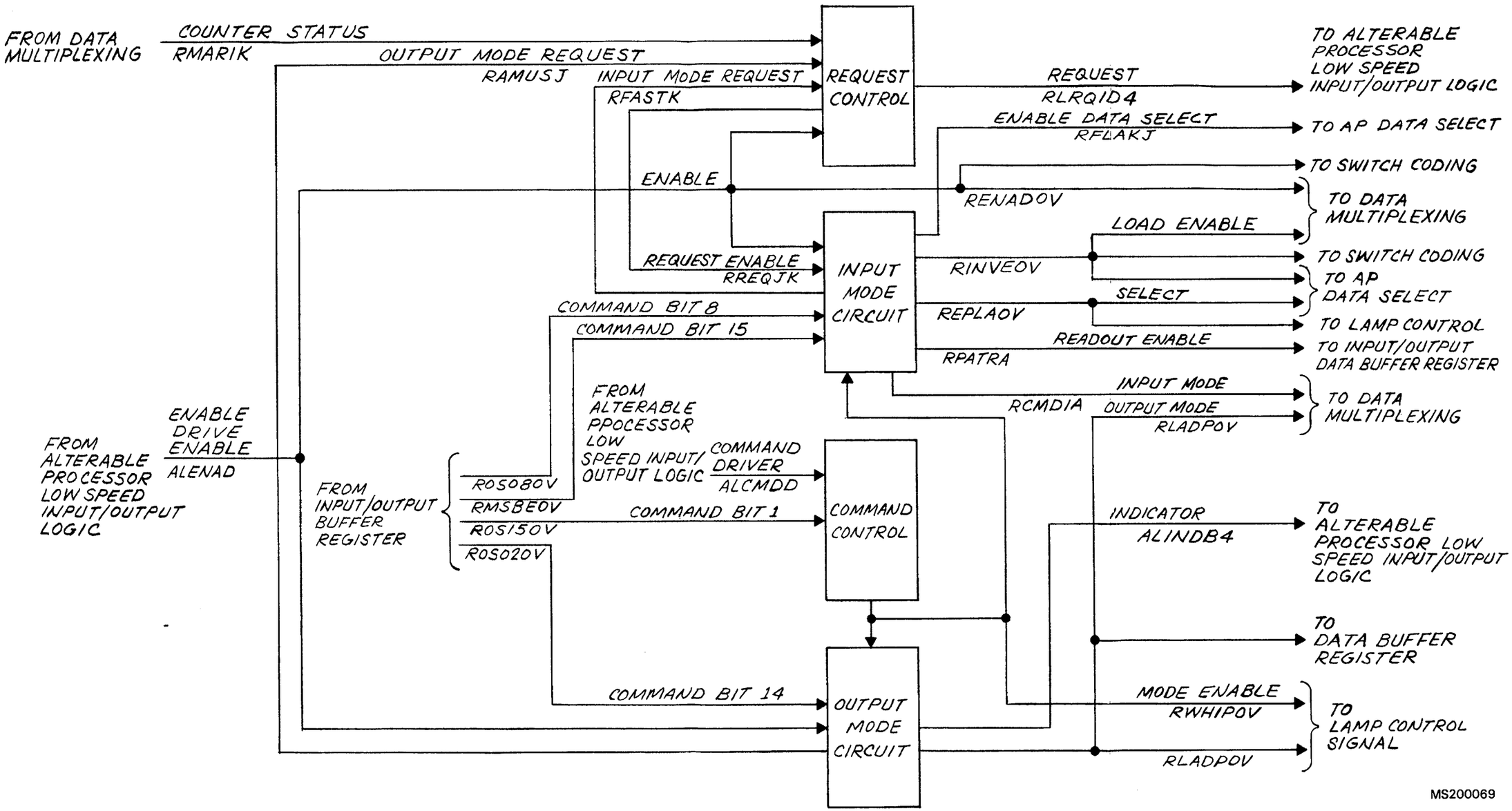


Figure 5-66. Input/Output Control Block Diagram

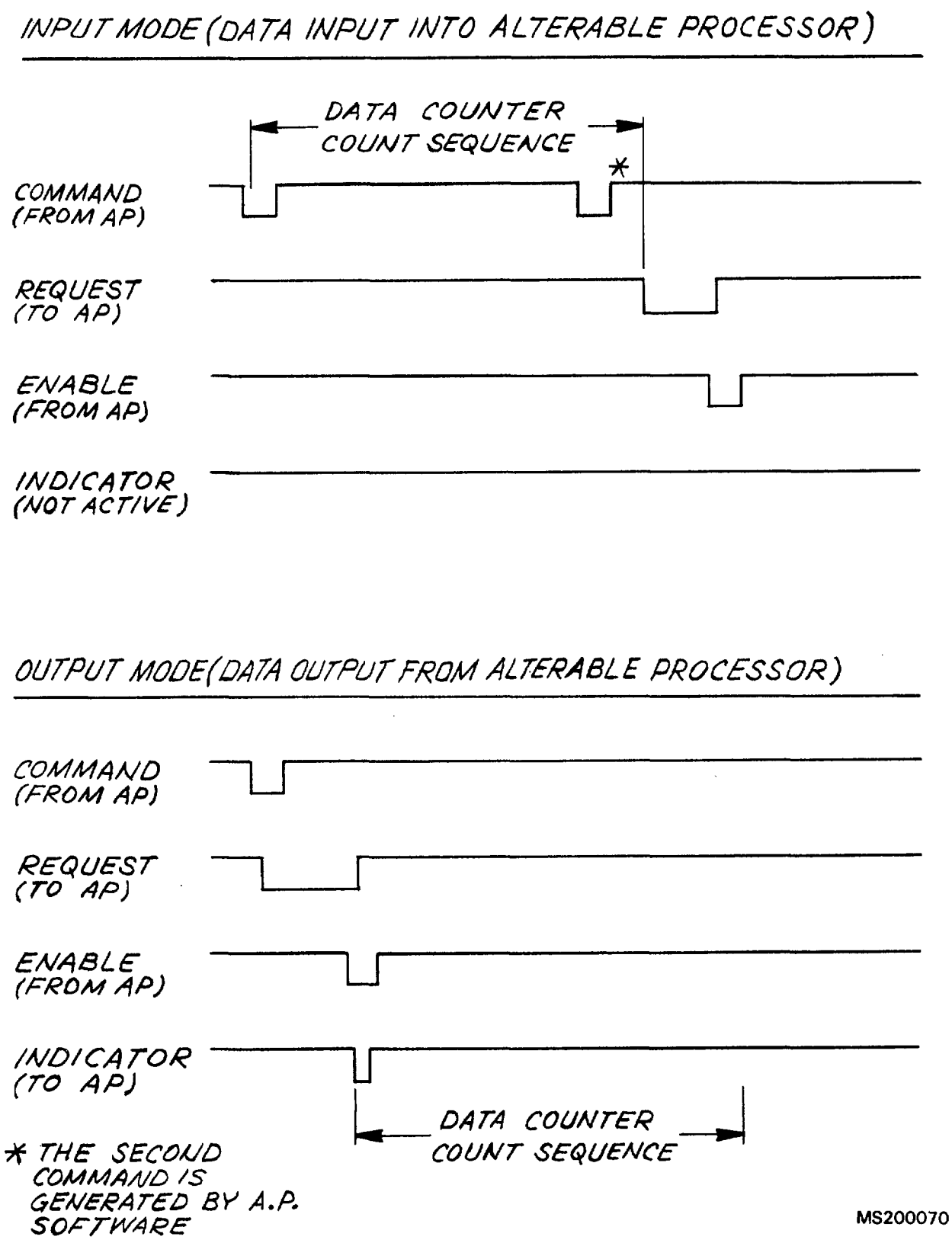


Figure 5-67. Input/Output Control and Alterable Processor Interchange Control Signals

signal to the AP. When request control receives a counter status signal from data multiplexing, the request signal is forwarded to the AP. Request control, also upon receiving the counter status signal, sends a request enable signal to the input mode circuit for transfer of a readout enable signal to the I/O data buffer register. The readout enable signal allows the I/O data buffer register to read out data to the AP. After receiving the request signal, the AP sends an enable signal to the I/O control which resets the request control and input mode circuit. The enable signal, through the I/O control, is supplied also to data multiplexing for terminating AN keyboard and switch selection and for clearing prior force stick data, and to switch coding for removing existing switch data.

b. *Lamp Input Mode*. The input mode circuit, upon receiving command word bits 8 and 15 from the I/O data buffer register. allows only data readout to lamp sources. When the first AP command signal is received by command control, a mode enable signal is sent to lamp control for loading of lamp group data bits. The mode enable signal is also applied to the input code circuit which outputs the following: a select signal to AP data select and lamp control, which selects the hardwired lamp select code and allows readout of lamp data, respectively; an enable signal to AP data select, which loads the lamp data source select code (lamp group data bits 9 thru 13); an enable data select signal to AP select, which allows input selection; and an input mode signal to data multiplexing, which initializes the data word count sequence. Upon receiving the second AP command signal, the I/O control performs the same functional sequence as described for the control input mode.

c. *Output Mode*. The output mode circuit receives a command, bit 14 from the I/O data buffer register. The output mode designates the transfer of lamp data words. Upon receiving an AP command signal, command control sends a mode enable signal to lamp control which loads command word instructions (lamp group data bits 9 thru 1 3). The mode enable signal is also sent to the output mode circuit which transfers an output mode request signal to request control. Upon receiving the output mode request signal. request control sends a request signal to the AP. The AP supplies an enable signal to the I/O control which terminates the request signal and allows the output mode circuit to output an indicator signal and output mode signal. The indicator signal is supplied to the AP for indicating that current lamp data is loaded on the data bus. The output mode signal is supplied as follows: to the I/O data buffer register for loading the lamp data on the data bus; to lamp control for lamp register selection; and to data multiplexing for initializing the data count sequence.

5-45. AP Data Select Detailed Description (fig. 5-68, FO-43). AP data select consists of the following elements:

Command select
Data select
Command storage
AN keyboard/switch select circuit

The command select has two coded data inputs, one variable and the other fixed. The variable coded data input accepts the switch data bits (9, 10, and I 1) from the I/O data buffer register. The switch data bits are used to select one of six data sources, excluding lamp data, for data word readout to the I/O data buffer register. The other input code is hardwired and selects the lamp data source only. The select signal from the 1I0 control logic to the command select selects one of these two data source input codes. The selected data source code is loaded into command storage, by a load enable signal from I/O control logic, which stores the code for the data select switch coding and data multiplexing. The data select uses the code to select a data word from one of the six data sources. The selected data is sent to the I/O data buffer register from data select upon receiving an enable data select signal from the I/O control logic. Upon receiving either an enable AN keyboard or enable switch data word signal, the AN keyboard/switch select circuit selects switch or AN keyboard to be sent to the data select.

5-46. Switch Coding Detailed Description (fig. 5-69, FO-44). Switch coding consists of the following elements:

Switch matrix
Front panel switches
Row encoder
Column encoder
Enable output detect
Load register circuit
Clear register circuit
Encoder output circuit
Row counter register
Column counter register
Output select

a. *Switch Matrix*. The switch matrix supplies a row and column code for all switches except the video selection, ARO data selection, task function, task selection, and center tab. When a switch in the switch matrix is pressed, a row code (rows 1 thru 16) is sent to the row encoder, and a column code (column 1, 2, 3, 6, and 7) is sent to the column encoder. Upon pressing the task function (row 5 thru 16) or task selection (row 1 thru 4) switches, a row code is supplied to the row encoder and, in turn, the row encoder applies a column code (column 4) to the column encoder. When pressed, the video selection switches (row 2 thru 7) supply a row code to the row encoder which, in turn, supplies a column code (column 5) to the column encoder through the fifth column select. When the ARO data selection switches (row 12 thru 16) are pressed, the row code is passed through the switch matrix to the row encoder, and the column code (column 5) is supplied to the column

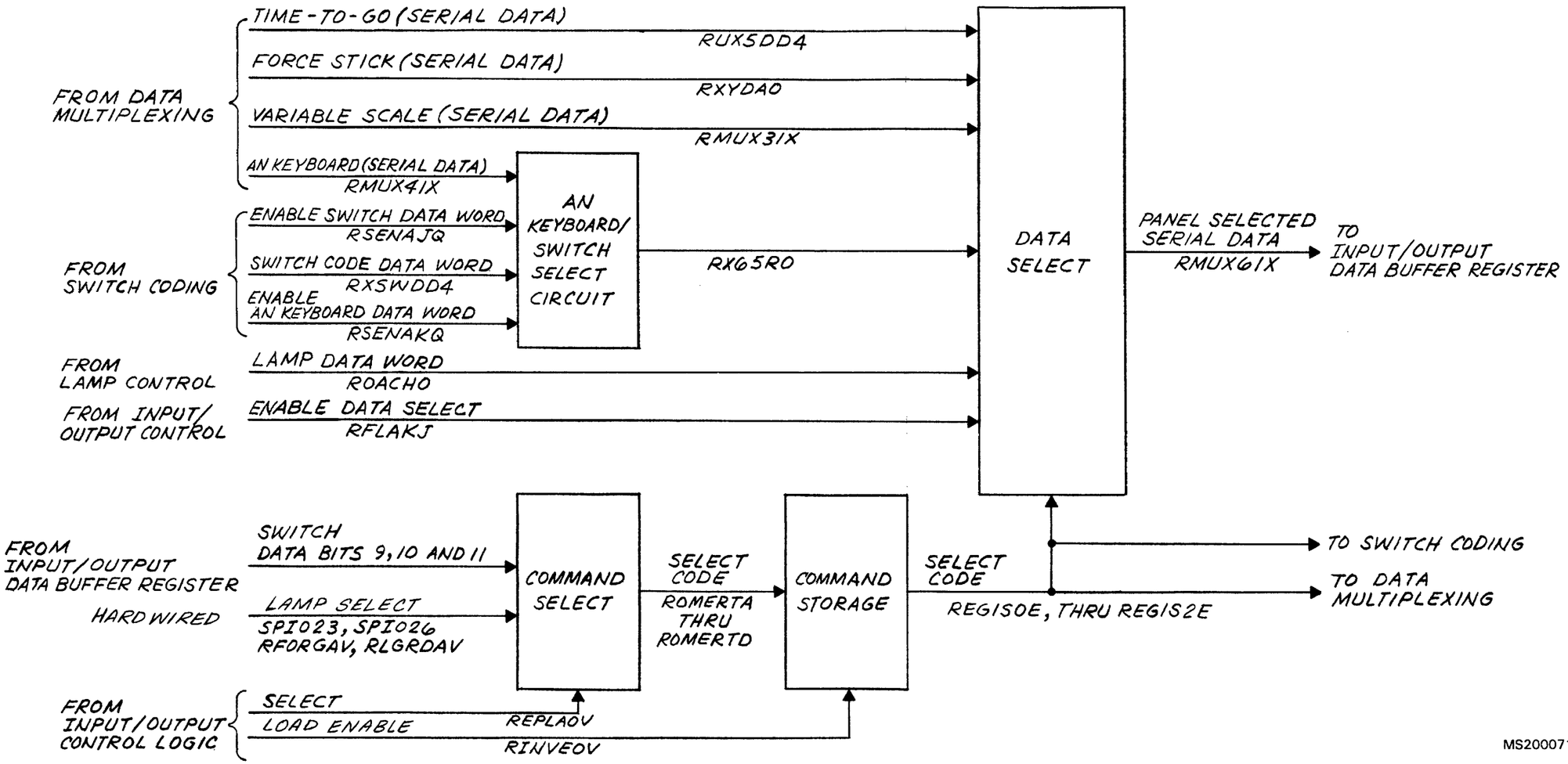


Figure 5-68. AP Data Select Block Diagram

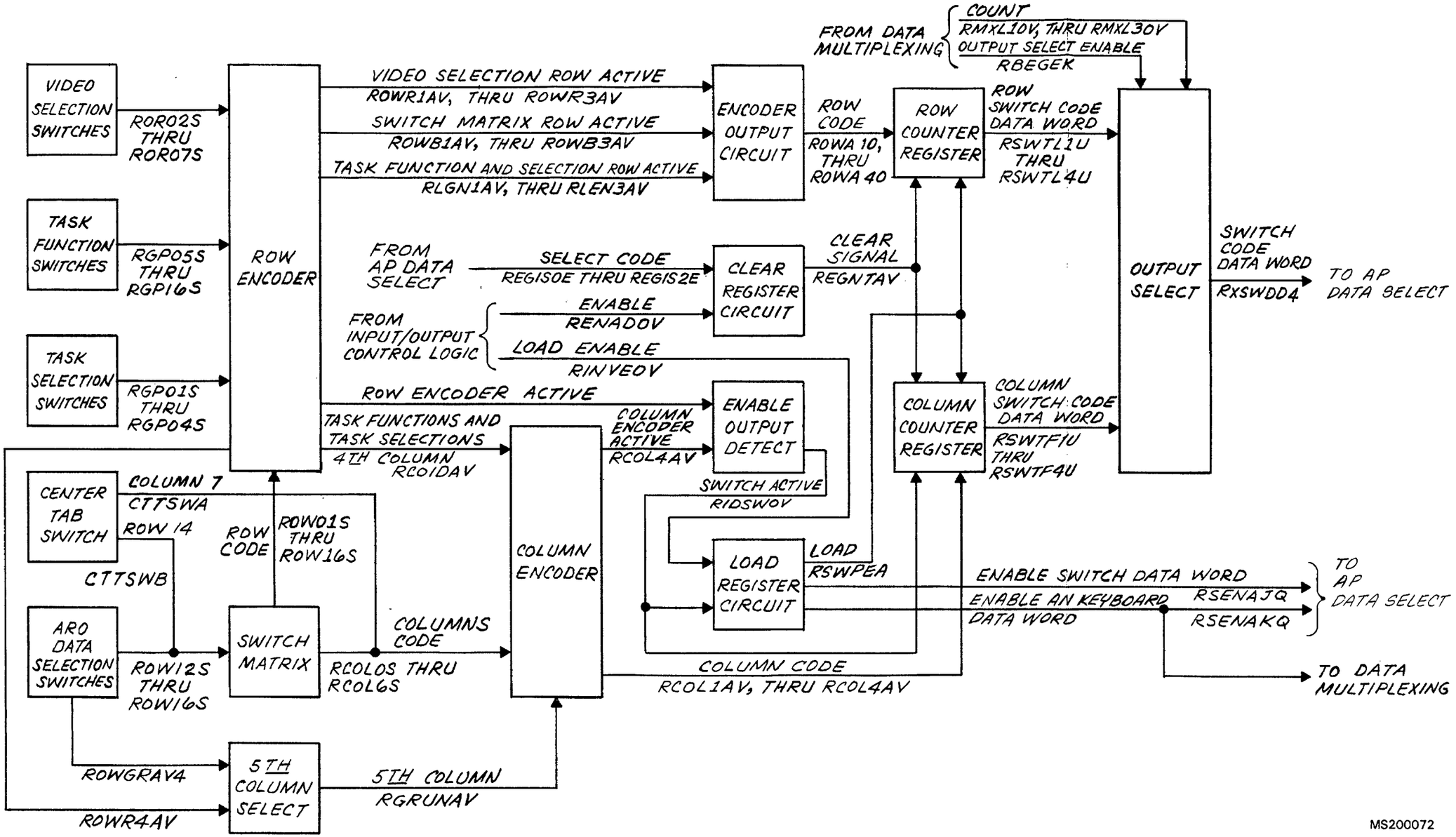


Figure 5-69. Switch Coding Block Diagram

encoder through the fifth column select. When pressed, the center tab switch (row 14) supplies the row code through the switch matrix to the row encoder and the column code (column 7) to the column encoder.

b. *Row and Column Encoders*. Upon detecting that a switch is pressed, the row and column encoders send row and column encoder active signals to the enable output detect. The row encoder also supplies video selection switch matrix, or task function and selection row active signals to the encoder output circuit. The encoder output circuit monitors the row active signals and supplies a row code to the row counter register. The column encoder supplies a column code to the column counter register.

c. *Enable Output Detect*. When both the column and row encoder active signals are received, the enable output detect outputs a switch active signal to the load register circuit and the column counter register. Upon receiving a load enable signal from I/O control, the load register circuit sends a load signal to the row and column registers to allow the row and column codes to be stored as row and column switch code data words. It also sends an enable switch data word signal to AP data select for selecting switch data. When the switch active signal is not active, the load register outputs an enable AN keyboard data word signal to AP data select and data multiplexing for selecting AN keyboard data.

d. *Output Select*. Upon receiving a count and output select signal from data multiplexing, output select transfers the switch code data word from the row and column counter registers to AP data select. After the switch code data word is read out, an enable signal from I/O control and a select code signal from AP data select clears the row and column counter registers through the clear register circuit.

5-47. Data Multiplexing Detailed Description (fig. 5-70, FO-45). Data multiplexing consists of the following elements:

Counter enable circuit
Position tab control
Clear circuit
Force stick driver and interface circuit
Pulse generator
Output select
Variable scale encoder
AN keyboard encoder
Time-to-go encoder
Data counter
Buffer
12-count circuit

a. *Counter Enable Circuit*. The counter enable circuit receives an input or an output mode signal from I/O control, which sends a shift signal to the I/O data buffer register for register shifting. The shift signal also activates the data counter which then transfers a count signal to the output select. The count signal is used to select data word bits for the position tab control, variable scale encoder, and AN keyboard encoder. The time-to-go encoder data bits are selected by the count signal which passes through a buffer for signal conditioning. The buffer also supplies the conditioned count signal to switch coding. Upon receiving the count signal, the output select sends the data word bits to the AP data select for serial readout. The count signal is also sent to the 12-count inhibit circuit which inhibits lamp control. After the data counter has terminated the count signal, a reset signal is sent to the counter enable circuit. The counter enable circuit then supplies a status output signal to the I/O control indicating completion of data word bit transfer. The counter enable circuit also supplies a shift signal to the data counter and I/O data buffer register to clear the data counter and inhibit the I/O data buffer register shifting.

b. *Position Tab Control*. The position tab control provides X and Y output voltages to the count generator which converts the voltages to X and Y pulse rates. The X and Y pulse rates are supplied to the X and Y force stick accumulator counter which provides X and Y parallel data (7 bits) to the output select. The pulses are accumulated between successive front panel data readout cycles (50 ms). At the conclusion of a readout cycle, the clear circuit receives an enable signal from I/O control and a select code signal from AP data select, which resets the X and Y force stick accumulator counter.

c. *Variable Scale and Time-to-Go Encoders*. The variable scale and time-to-go encoders convert manual selected data to parallel digital data for transfer to output select. The variable scale encoder outputs an 8-bit gray scale digital code.

d. *AN Keyboard Encoder*. The AN keyboard encoder converts keyboard selected data to a 7-bit parallel digital code for transfer to output select. Upon receiving an output select enable signal from the enable circuit, output select outputs AN keyboard data to AP data select. The enable circuit determines whether a switch in switch coding or a key on the AN keyboard is pressed. When the enable circuit receives a key actuation signal from the AN keyboard encoder or an enable AN keyboard data word signal from switch coding and a load enable signal from I/O control, an output select enable signal is sent to switch coding and to output select. Upon receiving an enable signal from I/O control, the enable circuit inhibits the output select enable signal.

5-48. Input/Output Data Buffer Register Detailed Description (fig. 5-71, FO-46). The I/O data buffer register consists of the following elements:

Input control circuit
I/O shift register
Output control circuit

The command word formats, shown in table 5-30, are for the various data categories that are processed by the front panel logic. The command word format shown for panel

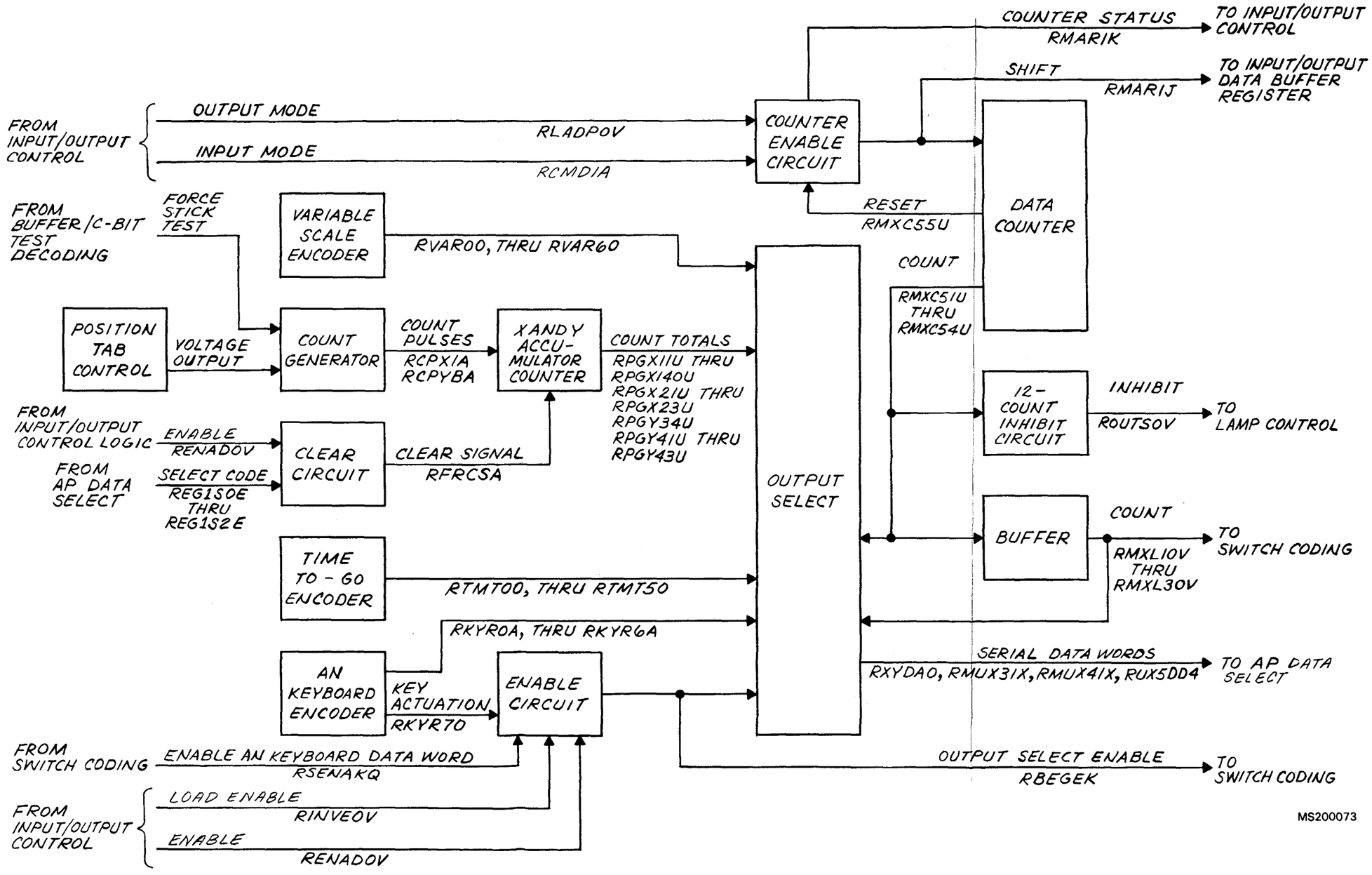


Figure 5-70. Data Multiplexing Block Diagram

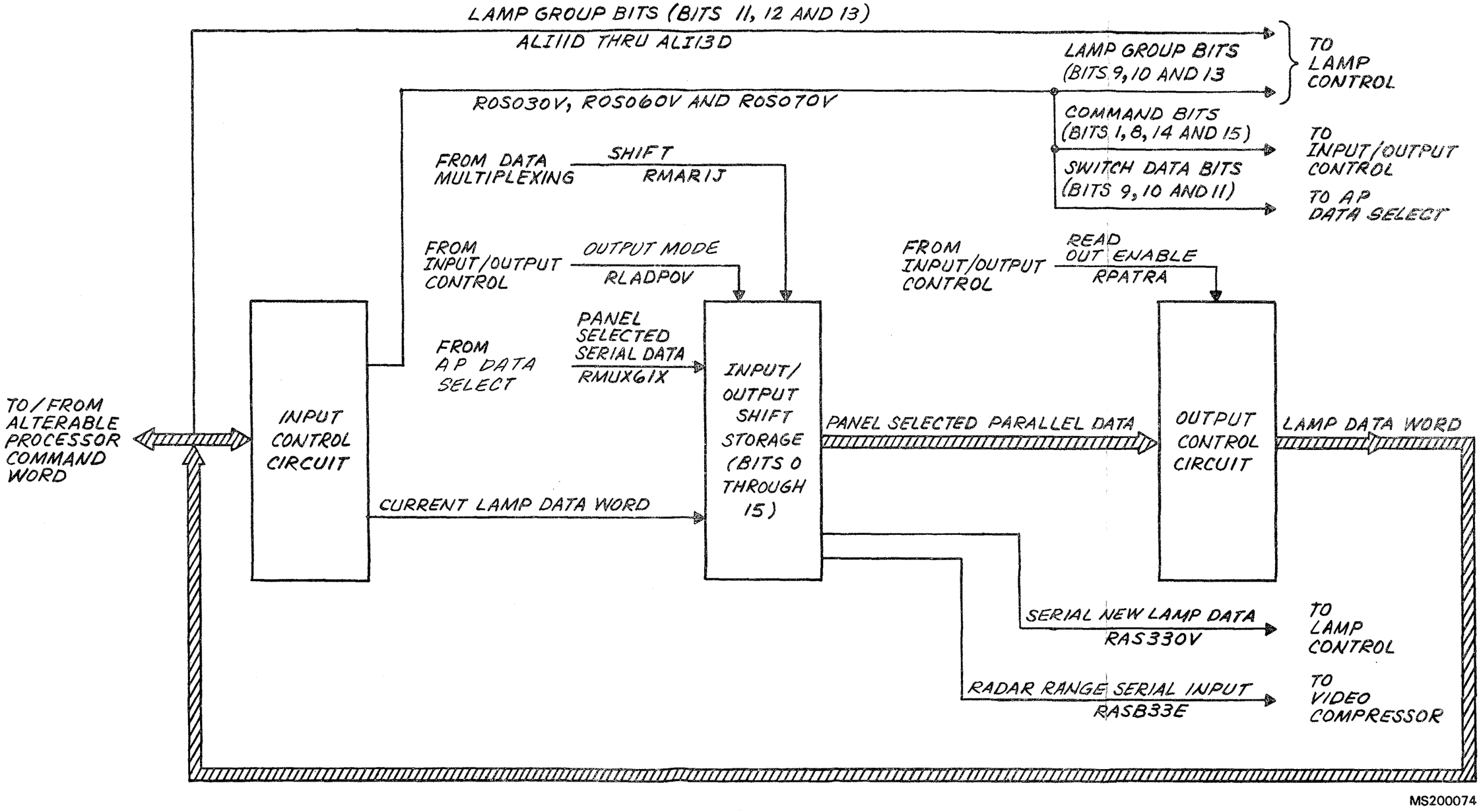


Figure 5-71. Input/Output Data Buffer Register Block Diagram

switches also applies to the AN keyboard, since either a switch data word or an AN keyboard data word is read out to the AP. One of the command words is also placed on the data bus by the AP at the start of an input or output mode data word transfer between the front panel logic and the AP. Once the command word has been placed on the data bus, certain bits of the command word are inverted or noninverted by the input control circuit and are distributed throughout the front panel logic. The command word bits are coded instructions to prepare the front panel logic for data word transfer. The command word consists of the following: switch data bits (9, 10, and 11) which are sent to the AP data select; command bits (1, 8, 14, and 15) which are sent to the I/O control; lamp group bits (9 thru 13) which are sent to the lamp logic.

a. *Input Mode.* Panel selected serial data (from the AP data select) is loaded into the I/O shift storage by a shift signal from data multiplexing. The shift signal enables the shifting function of the I/O shift storage. Once the data has been serially loaded into the I/O shift register, a readout enable signal from the I/O control to the output control circuit places the lamp data word on the data bus, ready for parallel readout to the AP.

b. *Output Mode.* Following introduction of the appropriate command word, the current lamp data word, after bit inversion by the input control circuit, is parallel-loaded into the I/O shift storage by an I/O control output mode signal. When the shift signal from data multiplexing is applied again to the I/O shift storage, the 12 bits of the current lamp data word is serially sent from the I/O shift storage to lamp control and 4 bits of radar range serial input is sent to the VC. Table 5-31 identifies data word formats for the various data sources.

Table 5-30. Command Word Formats.

Operating mode	Data transfer command	Data bits*																
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Input	Variable range	1	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0
Input	Force stick	1	0	0	0	0	1	1	0	0	0	0	0	0	0	1	0
Input	Time-to-go	1	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0
Input	Panel switches	1	0	0	0	1	1	1	0	0	0	0	0	0	0	1	0
Input	Lamp status	1	0	Lamp group					1	0	0	0	0	0	0	1	0
Output	Lamp data	0	1	Lamp group					0	0	0	0	0	0	0	1	0

*After inversion in I/O data buffer register

Table 5-31. Data Transfer Word Formats

Data bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Variable range (range is comp.)	1	1	1	1	1	1	1	1	MSB ← Range →						LSB	
Force stick	YSIGN	MSB ←						→ LSB	XSIGN	MSB ←					→ LSB	
Time-to-go (TTG is comp.)	1	1	1	1	1	1	1	1	1	1	TTG					
Panel switches and keyboard SB = 1 for panel switches	SB	MSB ←						→ LSB	SB	MSB ←					→ LSB	
Lamp data					MSB ←										→ LSB	

Section IX. COMPUTER BUFFER/C-BIT

5-49. General (fig. 5-72). The computer buffer/C-BIT provides data and control communications between the display console and the IOX and fault and control communications with the DOU. The computer buffer/C-BIT also provides the control and data lines required to accept and process the console status words from the AP. In addition, this logic deciphers the various operations codes from the IOX, informing the console logic of the current operation mode indicated by the IOX information. During the test mode, the computer buffer/C-BIT decodes the current test command, initiates the test routine in the addressed console logic, collects the resultant built-in test (BIT) sample, and forwards the test data to the IOX. The computer buffer/C-BIT comprises the following primary functional logic circuits:

Parity logic
I/O register
Test decoding
AP and DOU interface
I/O control
BIT sample multiplexing
Initialization logic

a. *Parity Generation*. The parity generation logic checks the input data for proper parity and generates proper parity for each output data byte.

b. *I/O Register.* The I/O register contains the data and control interface to the IOX and also provides temporary storage for up to 32 bits of I/O data. The I/O data, parity bit, enable, command, indicator, and request lines are temporarily latched at the interface when activated. This provides time for the IOX to accept the output information or for the computer buffer/C-BIT to process the input information. The input data is supplied to the parity generation logic for checking and to the I/O control for operation code deciphering and storage. The data byte output from the 32-bit register is distributed throughout the computer buffer/C-BIT for control signal generation and test command decoding. The I/O register outputs are also supplied to the AP, DB, and DC for use as test data.

c. *Test Decoding*. During a test mode, the test decoding decodes the input test commands and distributes the control signals required to implement these commands. When the proper sequence of input operations (a DEV-3 followed by an OFR) is received, the test decoding generates the device maintenance signal, placing the console in the test mode. The test control outputs to the AP and DC indicate the type (e.g., single step or loop) of test indicated by the current test command.

d. *AP and DOU Interface.* The AP and DOU interface generates the timing and control signals required to transmit data between the computer buffer/C-BIT and the AP. This logic also accepts DOU fault data and generates DOU control information. Data to the AP is OFR test information; data from the AP is console status information which is routed to the I/O register through the BIT sample multiplexing logic.

e. *I/O Control.* The I/O control detects the presence of IOX input and output bytes and generates the timing and control sequence required to process the data. The command/enable signals determine whether the current operation is an input or an output process. The I/O control decodes the control word byte to determine the type of input or output operation. The logic then generates the sequence of byte timing signals required to route the data from the source to the destination indicated by the current operation.

f. *BIT Sample Multiplexing.* The BIT sample multiplexing controls the sequence of feedback data processing and routes the selected data over the serial feedback data line to the I/O register. The feedback data may be console status data from the AP and DOU interface or one of the number of BIT samples from the console logic. The C-BIT control output addresses BIT sample muxs in the AP and DC. The status inputs from the AP and DC are utilized to ensure that no processing is occurring that might disturb the BIT sample being collected.

g. *Initialization.* The initialization logic responds to software and/or hardware reset signals to initialize pertinent logic in the console.

5-50. Parity Generation Detailed Description (fig. 5-73, FO-47). The parity generation logic consists of the following elements:

I/O byte mux
Input parity gate
Parity check mux
Parity error gate
Parity error flip-flop

The parity generation logic inspects IOX input data for property parity and generates proper parity for output data to the IOX.

a. The logic mode (parity detection or generation) is determined by the output timing active signal from the I/O control. When this signal goes low, data is being sent to the IOX. This disables the input parity gate and routes the mux bit 0-7 from the I/O register through the I/O byte mux to the parity check mux. This circuit develops a high signal for even byte parity and a low signal for odd byte parity. These signals are utilized by the I/O register to insert the proper parity bit into the output byte.

b. When the output timing active signal is high, the input parity gate is enabled and input bits 0-7 are

routed to the parity check mux. The nine input bits are then compared for proper odd parity. Proper parity results in a high byte parity signal to the I/O control permitting the associated input control byte to be processed. The byte examine enable signal indicates that an input byte accompanied by a parity bit was received by the I/O register. At byte count 0, indicating that the parity byte is stored in the input data latches, the parity error gate checks the output from the parity check mux. Even parity toggles the parity error flip-flop. The resultant signal to the I/O control aborts processing of the input byte.

5-51. Input/Output Register Detailed Description (fig. 5-74, FO-48). The I/O register consists of the following elements:

Reset gate
Parity bit I/O coupling
Data byte I/O coupling
Enable I/O coupling
Command I/O coupling
Indicator I/O coupling
Parity I/O gate
Data I/O gate
Enable I/O gate
Command l/O gate
I/O register bits 0-31
Output byte 2 shift
Output byte 1 shift
Output buffer mux
ITR online
Computer buffer parity output
Computer buffer data output
CPU request output
CPU indicator output
Address select

The I/O register provides the interface coupling and temporary storage for the data and control lines between the computer buffer/C-BIT and the IOX. The 8-bit data lines and the parity bit line are bidirectional, the enable and command lines are inputs to the computer buffer/C-BIT, and the indicator and request lines are outputs. This circuit utilizes a 32-bit storage register to buffer up to 4 bytes of input or output words.

a. The parity bit, data, enable, and command I/O coupling and the associated I/O gates are configured as latches which are set upon detection of an active input signal. The parity bit and 8-bit input data are supplied to the external computer buffer/C-BIT logic for byte detection and parity checking. The 8-bit byte is also supplied to the most significant stage of the 32-bit I/O register. The byte move signal goes active each time data is to be transferred from the data byte I/O coupling to the shift register. The byte move signal transfers any byte currently stored into the next least significant 8-bit stage of the register. When the byte has been properly processed or stored, the byte latch clear (from I/O control) releases the latches for the next byte. Thus, during the input mode, the I/O register acts as four 8-bit parallel-in/parallel-out registers. For an OFR operation, the register stores the 4 OFR data bytes. For a DEV operation, the single data byte is stored in the most significant stage. There is no data byte utilized for an EOB or STOP operation. The outputs from the 32-bit register are distributed to various console logic for use during the aforementioned operations.

b. During console status data output for an output data operation, each 8-bit stage acts as a serial-in/parallel-out register. Serial shifting for each stage is enabled by a separate shift feedback bits signal to accept the 8 bits of serial feedback data from the BIT sample multiplexing. When all 4 bytes are stored in the register, the I/O control will commence the timing sequence required to transmit the console status data to the IOX. The byte move signal steps each byte into the next least significant stage. For a console status word output operation, the output buffer mux routes the 8 bits from the least significant register stage to the computer buffer data output gates. This data is also sent to the parity generation logic which develops the proper parity bit and supplies this bit to the computer buffer parity output gate. The output strobe from the I/O control then transfers the information to the parity and data I/O coupling. After 200 nsec for the IOX to accept the data, the I/O coupling latches are released by the byte latch clear signal. This sequence continues until all 4 console status bytes have been transmitted to the IOX.

c. For a conventional ITR operation, the 16-bit BIT sample word is loaded into the two least significant stages of the I/O register. The two most significant stages still contain the 2 least significant bytes of the previous OFR message. The 2 ITR bytes and 2 OFR bytes are then transmitted to the IOX.

d. When the BIT sample multiplexing has collected the 16-bit BIT sample, the BIT sample LSB shift signal goes active for eight clock times. The eight BIT sample LSBs supplied over the serial feedback data line are then shifted into the second least significant I/O register stage. The BIT sample MSB shift signal then goes active, shifting the 8 MSBs into the least significant register stage. A subsequent ITR operation will shift the 4 bytes to the IOX in an identical manner as for the console display message.

e. Logic is provided for an ITR online operation (note that this operation is not currently utilized in the IOX/computer buffer/C-BIT repertoire). The ITR operation permits the IOX to request fault information by means of an ITR operation without entering the maintenance mode. The computer buffer/C-BIT responds with a single DOU fault byte. If utilized, this operation would allow the IOX to collect test data while the console was online with the DOU. The set condition of the ITR flip-flop and the inactive maintenance mode signal enables the ITR online gate. This routes the DOU fault data from the interface AP and DOU logic through

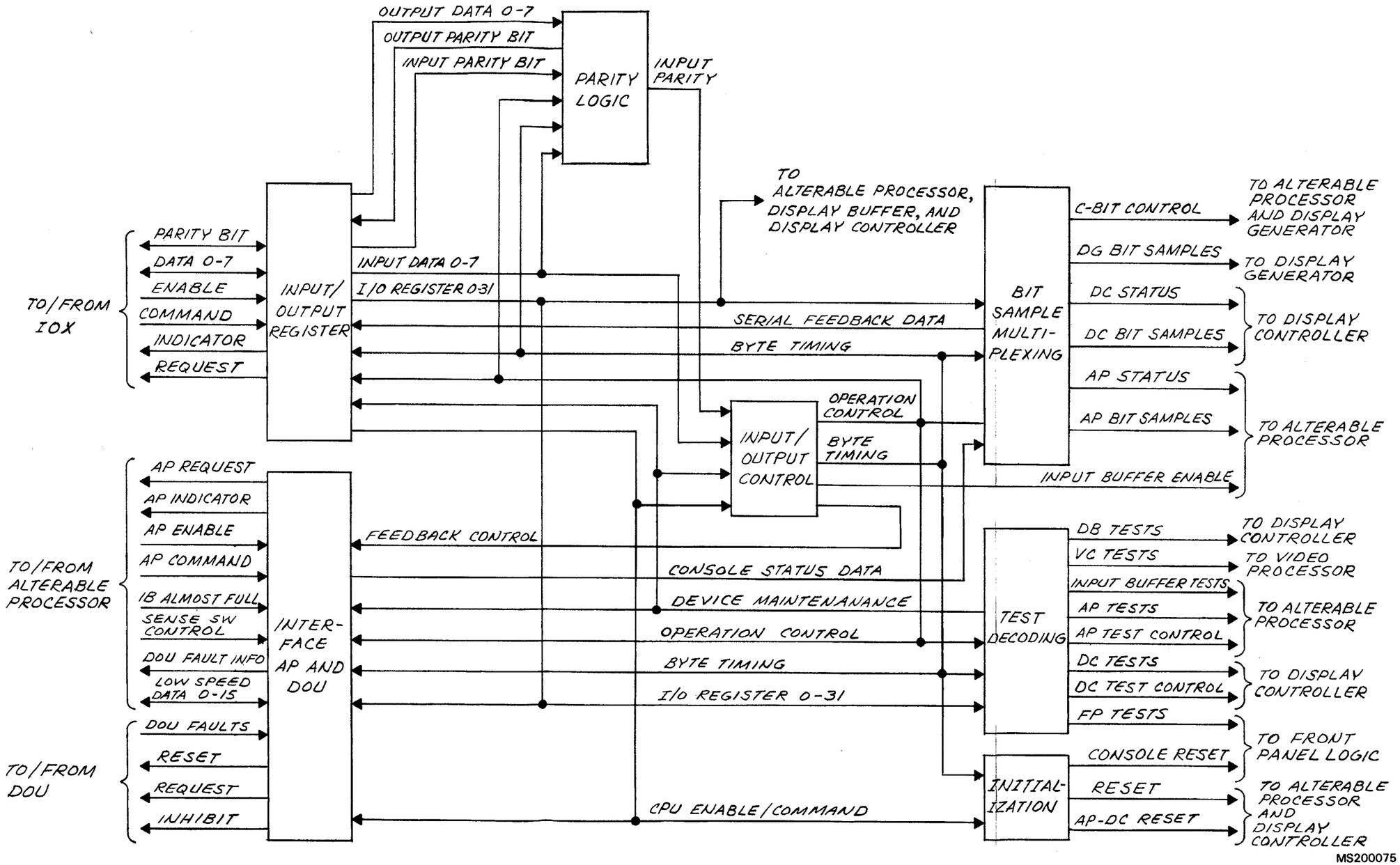


Figure 5-72. Computer Buffer/C-BIT Block Diagram

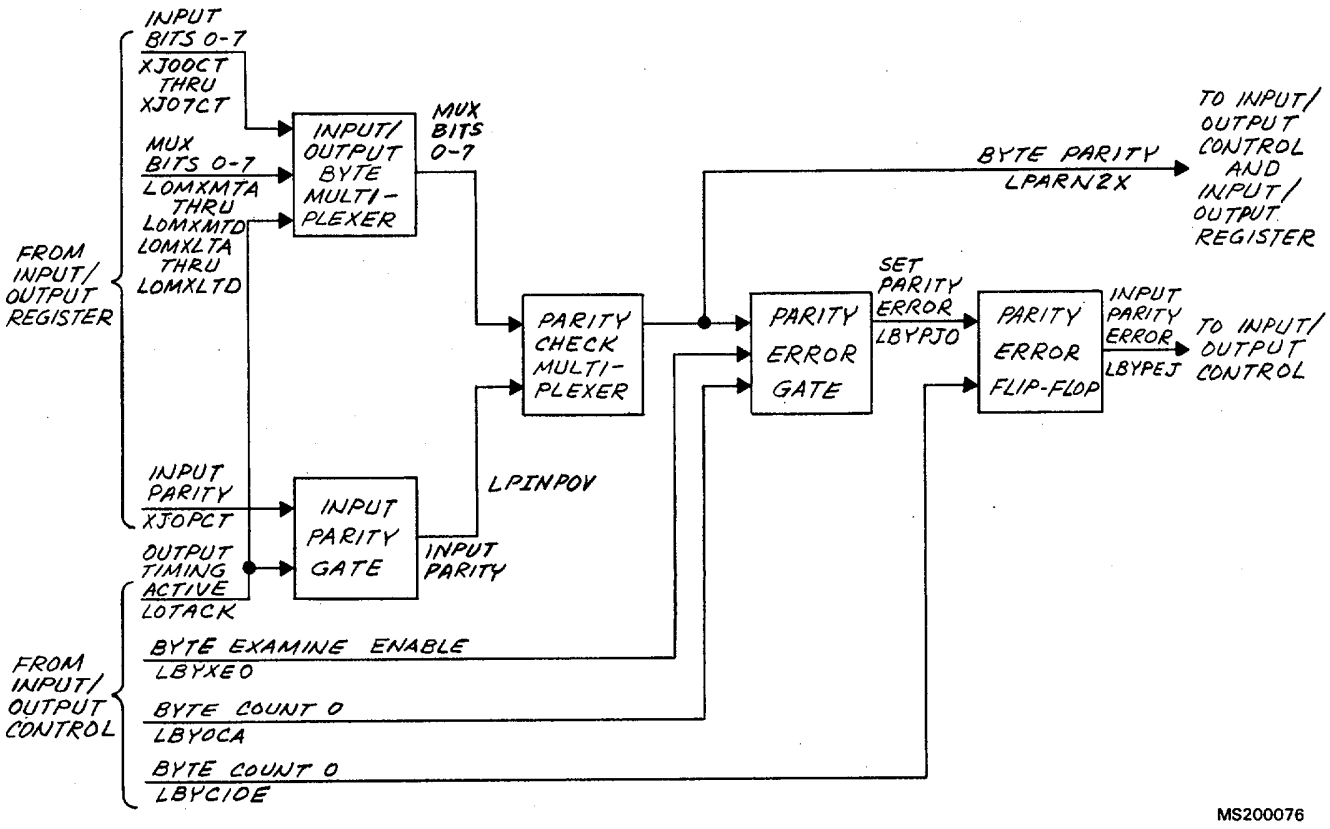


Figure 5-73. Parity Generation Block Diagram

the output buffer mux to the output gates. A single output strobe then latches the DOU fault byte.

f. Address selection is performed by ADDRESS SELECT switch S1 which permits each console to manually select one of eight console addresses. The input address byte is converted to a 3-bit binary address in the address select circuit and forwarded to the 8-input mux for inclusion in the console status word. The circuit also routes the request signal to the IOX over the proper request line. In addition, a signal is applied to the test decoding logic indicating when the particular console is being addressed.

5-52. Test Decoding Detailed Description (fig. 5-75, FO-49). The test decoding logic consists of the following elements:

Group select decoder
Radar video mixer test control
Mode change command decoder
Signal action command decoder
Device maintenance
BIT GO gate
AP-DC maintenance go
BIT execute enable
DOU simulate
Display data mux enable
AP run
DC breakpoint
AP external command execute
AP command execute
AP breakpoint
DC command execute
DC external command execute
Alterable processor go
Display controller go
Input parity
Input buffer loop latch
Force stick test latch
VC center section test go
VC test go
Display buffer input select
Display buffer test data
Display buffer loop latch

The test decoding logic detects the OFR operation, decodes the associated test commands, and distributes the control signals required to implement the commands. The OFR operation is initiated by a DEV-3 input from the IOX. An active device indicator signal from the AP and DOU interface indicates that a DEV operation is addressed to a particular console. The I/O bit 26 input signal represents a ONE in input data bit 1. This is indicative of a DEV-3 operation and sets the maintenance mode circuit. The device maintenance outputs inform various external computer buffer/C-BIT and AP logic of the impending test operation. The AP-DC GO circuit is set each time the console is initialized or for an AP-DC free run test. The circuit generates the AP and DC GO levels which permit those circuits to function normally for normal or free-run test operations. For all other test modes, the AP and DC GO levels are inactive unless enabled by the appropriate test operation. When the subsequent OFR operation and associated data bytes are received and stored, the BIT GO gate is enabled to set the BIT execute enable flip-flop. Subsequent logic operation is dependent upon the context of the OFR word now stored in the I/O register. There are two OFR word formats, the non-input and the input buffer test, as shown in figures 5-76 and 5-77, respectively. The specific type of test required is dependent upon the group select (bits 24 thru 26) and the test select (bits 20 thru 23) codes. Table 5-32 details the tests associated with the various group and test select codes. The group select decoder combines the group select inputs (bits 24 thru 26) to determine the type of test required (single action, mode change, radar video mixer, or input buffer). For example, a 000 group select address enables the single action command decoder. Decoding bits 21 thru 23 will enable one of eight discrete tests involving the AP, DB, DC, or the VC. A 001 group select address enables the mode change command decoder. Bits 21 thru 23 are then decoded to enable one of five loop modes, run to breakpoint, or force stick tests. Group select code 0 1 0, in conjunction with bits 20-23, initiates one of nine radar video mixer tests. Group select OFR bit 24, containing a ONE, indicates an input buffer test command. For these commands, the OFR third byte (bits 16 thru 23) is utilized as data to the input buffer. An active bit 24 enables the DOU simulate gate which develops the display data mux enable signal. The parity bit for this operation is stored by the input parity flip-flop. The following is a brief description of each of the OFR test commands.

a. Single Action Test Commands. Single-action test commands are as follows:

(1) *BIT sample inhibit (000 x 000).* The BIT sample inhibit to the BIT sample multiplexing inhibits the BIT sample shift function to the I/O register. Thus, the input data will remain undisturbed and be returned to the IOX during the subsequent ITR operation, verifying IOX to computer buffer/C-BIT and computer buffer/C-BIT to IOX transmission.

(2) *New BIT sample (000 x 000).* The new BIT sample signal to the BIT sample multiplexing permits a new BIT sample address to be specified while inhibiting any logic testing manipulation. Thus, a BIT sample will be returned without altering the status of the addressed logic.

(3) *Video compressor test (000 x 010)*. This code enables the VC logic test. The video compressor test signal going low, combined with the BIT GO signal, develops the VC CENTER SECTION TEST GO signal which prepares the VC logic for the impending test. The video compressor test signal also generates the VC TEST GO signal which enables the test. During this test, all other console logic is inhibited. The test requires approximately 750 ms. The BIT address for this test is all

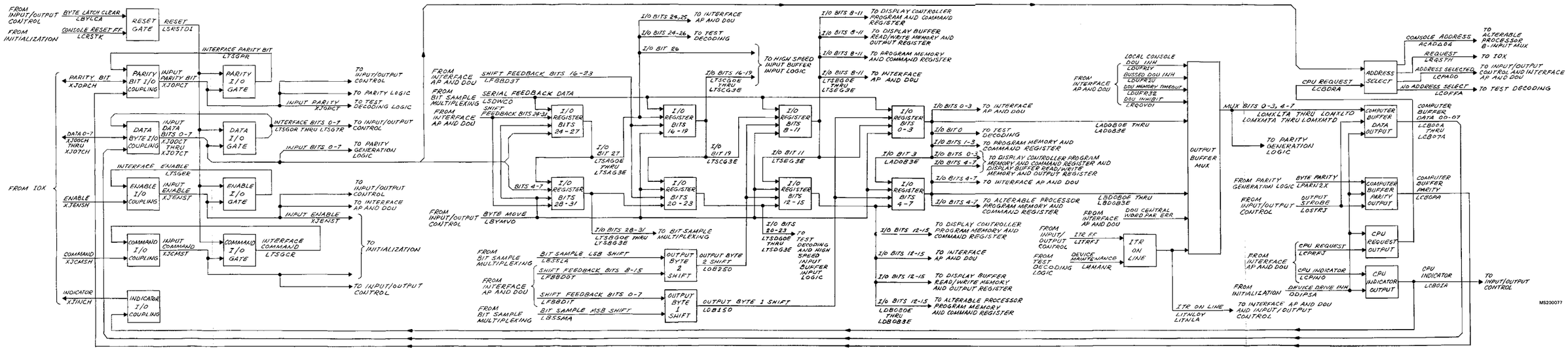


Figure 5-74. Input/Output Register Block Diagram

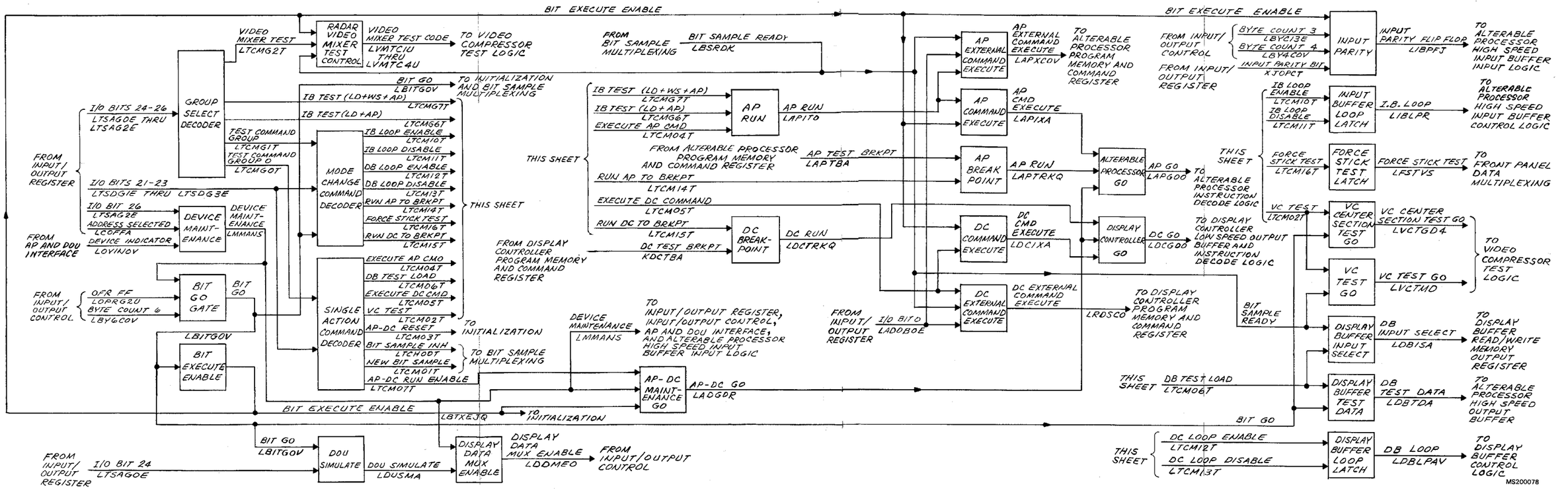
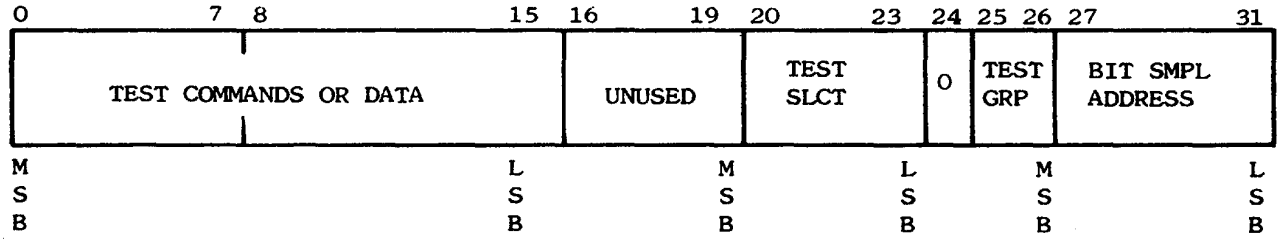


Figure 5-75. Test Decoding Block Diagram



NOTE: BIT 24 IS A ZERO FOR
A NON-INPUT BUFFER OFR.

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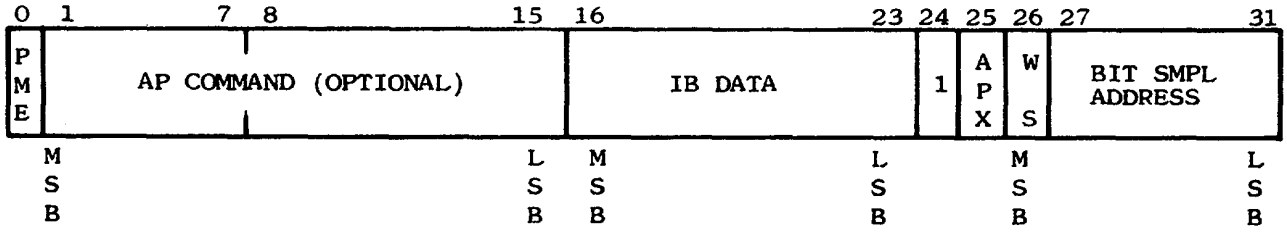
Figure 5-76. OFR Word Format (Non-IB Test)



NOTE:

PME = PROGRAM MEMORY ENABLE
APX = ALTERABLE PROCESSOR EXECUTE
WS = WORD SYNC (1ST BYTE FLAG)

BIT 24 IS A ONE FOR
AN INPUT BUFFER TEST.

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Figure 5-77. OFR Word Format (IB Test)

Table 5-32. OFR Test Command Encoding

	Code							
	Group select			Test select				Test type
	24	25	26	20	21	22	23	
Single action test commands	0	0	0	X	0	0	0	BIT sample inhibit
				X	0	0	1	New BIT sample
				X	0	1	0	Video compressor test
				X	0	1	1	Reset AP and DC
				X	1	0	0	Execute AP command
				X	1	0	1	Execute DE command
				X	1	1	0	Display buffer test load
				X	1	1	1	AP-DC free run
Mode change test commands	0	0	1	X	0	0	0	Input buffer loop enable
				X	0	0	1	Input buffer loop disable
				X	0	1	0	Display buffer loop enable
				X	0	1	1	Display buffer loop disable
				X	1	0	0	Run AP to breakpoint
				X	1	0	1	Run DC to breakpoint
				X	1	1	0	Force stick test enable
				X	1	1	1	Unused
Radar video mixer test commands	0	1	0	0	0	0	0	Unused
				0	0	0	1	RVM test channel 1
				0	0	1	0	RVM test channel 2
				0	0	1	1	RVM test channel 3
				0	1	0	0	RVM test channel 4
				0	1	0	1	RVM test channel 5
				0	1	1	0	RVM test channel 6
				0	1	1	1	RVM test channel 7
				1	0	0	0	RVM test channel 8
				1	0	0	1	RVM test channel 9
	0	1	1	X	X	X	X	Unused
Input buffer test commands	1	0	0	(Data)				Load third byte
	1	0	1	(Data)				Load third byte, word sync
	1	1	0	(Data)				Load third byte, execute one AP command
	1	1	1	(Data)				Load third byte, word, sync, execute one AP command

ONES in OFR bits 27 thru 31. Bits 2 thru 7 of the subsequent ITR will contain the BIT sampling data.

(4) Reset AP and DC (000 x 011). This code reinitializes all console logic with the exception of the computer buffer/C-BIT. All normal logic processing is halted and a BIT sample is collected for a subsequent ITR.

(5) Execute AP command (00 x 100). This code generates the AP GO signal, which enables the AP to execute the instruction currently stored in the command register. The next command register instruction is dependent upon the state of OFR bit 0. When this bit is a ONE, the command register is loaded with the next programmed instruction. When OFR bit 0 is a ZERO, the AP external command execute signal loads OFR bits 0 thru 15 into the command register. When the command register is reloaded, the AP stops and the BIT sample is collected.

(*6) Execute DC command (000 x 101).* This code operates for the DC precisely as the above code operates for the AP.

(*7) Display buffer test load (000 x 110*). This code transfers OFR bits 0 thru 15 into the DB memory.

(*8) AP-DC free run (000 x 111*). This code sets the AP-DC MAINTENANCE GO latch enabling the AP-DC GO signal to the respective circuits. This permits the AP and DC to operate from their normal programs, utilizing data from the high speed input buffer and the DB, respectively. Either or both buffers may be in the loop mode. After a free run command is issued, a DEV-3 operation must be received before any BIT sampling is performed or any ITR operation is recognized.

b. *Mode Change Test Commands.* Mode change test commands are as follows:

(1) *Input buffer loop enable (001 x 000*). The code sets the input buffer loop latch. The resultant enable allows the high speed input buffer to loop (the input buffer empty indication is ignored in order to allow the memory to continuously recycle).

(*2) Input buffer loop disable (001 x 001*). This code resets the input buffer loop latch so that only a single word can be read from the input buffer. Note that this latch is also reset when the console is initialized but is not reset by the AP and DC reset OFR.

(*3) Display buffer loop enable (001 x010*). This code sets the display buffer loop latch permitting the DB memory to continuously recycle.

(*4) Display buffer loop disable (001 x011).* This code resets the display buffer loop latch, terminating the recycle mode.

(5) Run AP to breakpoint (001 x1000). This code sets the AP breakpoint flip-flop which generates the AP go signal. The AP will then be run by the normal program routine until a breakpoint is indicated by a ONE in bit 15 of the current command. The resultant AP test breakpoint signal stops the AP operation and a BIT sample is collected.

(6) Run DC to breakpoint (001 x 101). This code initiates a DC operation in the identical manner as the above command functions for the AP.

(*7) Force stick test enable (001 x 10*). The code sets the force stick test latch supplying a test enable signal to the front panel logic. With no force stick pressure or test signal, the force stick increment counters are cleared. Application of the test signal will result in a non-ZERO counter output. The test signal will remain enabled until the console is reinitialized.

c. *Radar Video Mixer Test Commands.* A 010 group select code loads test select bits 20 thru 23 into the radar video mixer test control. This circuit is normally cleared, indicating normal video mixer operation. In a test condition, sequential OFRs are supplied, selecting video mixer channels 1 thru 9, each followed by an ITR to retrieve the resultant BIT sample. The BIT address for this sequence of tests is all ONES in OFR bits 27 thru 31. The BIT sample for the video mixer tests are reflected in the two most significant digits of the ITR words.

d. *Input Buffer Test Commands.* A ONE in OFR bit 24 indicates an input buffer test command and develops the display data mux enable. This permits the OFR third byte (bits 16 thru 23) to be transferred to the high speed input buffer as data. For a 100 group select, only the 3rd byte is transferred. For a 101 group select, the word sync bit is loaded with the data byte. For a 110 group select, the data byte is loaded and AP GO is enabled to execute a command. For a 111 group select, the data byte and word sync bit are loaded and the AP GO signal is generated. The above scheme permits the computer buffer/C-BIT to simulate normal DOU display data transfers with a sequence of OFR operations. The input buffer test commands utilize OFR bit 0 in an identical manner as for the execute AP and DC commands. A ONE in OFR bit 0 loads the next programmed command into the command register. A ZERO in OFR bit 0 copies OFR bits 1 thru 10 into the command register. When the command is executed and the command register is properly loaded, the BIT sample is collected.

5-53. AP and DOU Interface Detailed Description (fig. 5-78, FO-50). The AP and DOU interface consists of the following elements:

AP output circuit
AP input flip-flop
AP request
Indicator bus
AP input enable
Feedback load
Feedback received
Feedback shift
Feedback counter
Feedback halfway circuit
Feedback decoder
Feedback requirement enable
Feedback requirement to CPU
Feedback ready flip-flop
AP output gates
I/O shift register
Feedback serial data
Enable gate
Console message indicator
Console message received
Console message request
CPU request
ITR last byte
ITR indicator
CPU indicator
Device indicator
Device stop
OFR indicator
Request command
DOU device reset
DOU request inhibit
DOU inhibit bus
Radar only gate

Display console DOU INHIBIT OVERRIDE switch
DOU fault sensor

The AP and DOU interface develops the timing and control sequences required for information transmission between the computer buffer/C-BIT and the AP. The logic also generates various command signals for the DOU and IOX and fault information for inclusion in console status and ITR messages.

a. AP low speed interface provides the data transfer and control logic associated with the low speed data communication between the AP and the computer buffer/C-BIT. Logic is provided to respond to AP commands indicating whether the imminent transfer is an AP input or output operation. Figure 5-79 illustrates the timing sequence required for the transfer of status control data from the AP. For this operation, the AP supplies a command and AP output signal to which the computer buffer/C-BIT replies with a request. The AP then generates an enable signal which initiates the timing sequence required to transfer the initial 15-bit word to the computer buffer/C-BIT I/O register. A second enable transfers the second word to the I/O register, and the computer buffer/C-BIT forwards a request signal to the IOX indicating that the console status word is available.

b. An AP output operation is initiated by the concurrence of an active AP addressed command and ZERO in low speed data bit 8 from the low-speed I/O logic. These conditions set the AP output circuit and activate the request signal to the AP.

c. An active enable signal indicates that the AP is prepared to transfer the initial console status byte. The enable input generates the feedback load signal which transfers the information currently on the low speed data lines into the I/O shift register. The feedback load signal also generates the indicator signal, informing the AP that the data has been accepted. The next clock sets the feedback received flip-flop initiating the word feedback timing sequence. The feedback shift signal provides a shift enable to the I/O shift register and a count enable to the feedback counter. The 15-bit word is then stepped through the I/O shift register to the BIT sample multiplexing for ultimate storage in the I/O register. The feedback counter monitors the data being shifted, supplying control signals to the feedback decoder. The feedback decoder develops the signals required to ensure that each feedback byte is stored in the proper stage of the I/O register. Table 5-33 details the relationship between the decoder inputs and outputs. For the initial eight counts, the feedback bits 8-15 enable is generated. Note that the feedback byte is shifted out most significant byte first. When the most significant stage of the counter sets, the feedback bits 0-7 goes active. When the counter reaches its terminal count, the feedback halfway circuit is set, temporarily inhibiting all feedback decoder outputs.

d. The logic now waits for the next enable associated with the second 15-bit feedback word. This enable loads the second word into the feedback register, generates the indicator signal to the AP, and initiates the second word feedback timing sequence. The feedback load also sets the feedback requirement enable latch. When the feedback counter again reaches terminal count, the set condition of the feedback halfway circuit and feedback requirement latch causes the feedback ready and CPU request flip-flop to set. The CPU request indicates that the console status word is available to the IOX. The feedback ready will remain set until the last status byte is transferred to the IOX.

e. When the current AP command requires data to be input, the set AP input FF signal is activated. Setting this flip-flop, in conjunction with an active low speed I/O command signal, causes the AP input enable to place the I/O bits 0-15 on the low speed data bus. A subsequent enable from the AP generates the indicator signal, informing the AP that the desired data is available.

f. Request indicator and DOU command generation is utilized to generate the CPU request and indicator signals and the DOU reset and request commands. An active sense switch 8 signal from the AP indicates that a console status message is being prepared for transmission. As long as the console is not in the maintenance mode, the SW8 signal generates a CPU request to the I OX interface and also sets the console message received flip-flop. When the IOX is prepared to accept the console message, the enable signal and appropriate console address generates the console message indicator which resets the console message received flip-flop and supplies the indicator signal to the IOX.

g. The CPU indicator is also generated for other interface communications in response to command signals and the proper sequence of data bytes. The ITR indicator is generated immediately after the 4th and last BIT sample data byte is forwarded to the IOX during an ITR operation. The device indicator is activated after the initial data byte is received during a DEV operation. The OFR indicator is generated after the 4th and final byte is received during an OFR operation.

h. For a DEV-1 command, which instructs the console to request the DOU for display refresh data, data bit O is active. Note that since the single device data byte is stored in the most significant stage of the I/O register, I/O bit outputs 24 thru 31 correspond to input data bits O thru 7. As long as the console is not in the maintenance mode, a DEV operation with bit O (I/O bit 24) active supplies a request command to the DOU. The reset command is activated by either a reset signal from the initialization logic or a DEV-2 operation indicated by input data bit I (I/O bit 25) being active.

i. The DOU request inhibit is generated either by sense switch 7 going set or by the high speed input buffer memory becoming almost full. This indication is for-

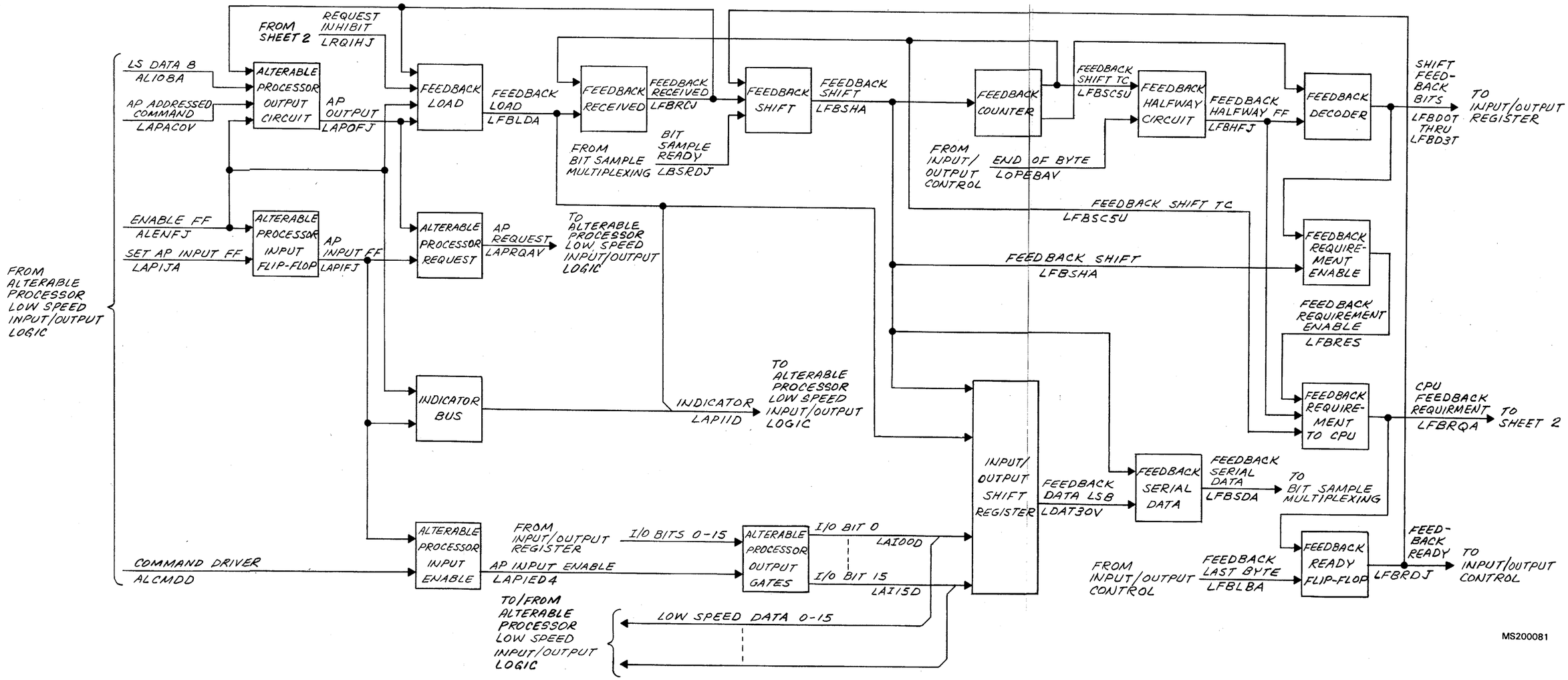

Figure 5-78. AP and DOU Interface Block Diagram (Sheet 1 of 2)

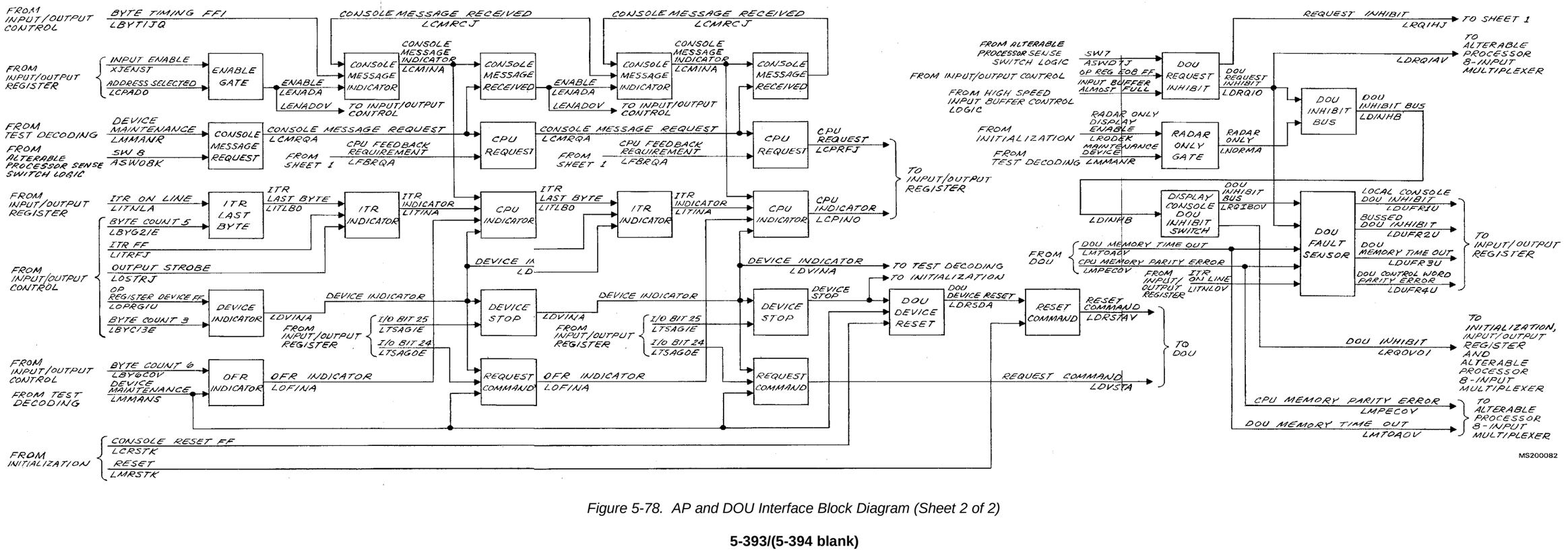

Figure 5-78. AP and DOU Interface Block Diagram (Sheet 2 of 2)

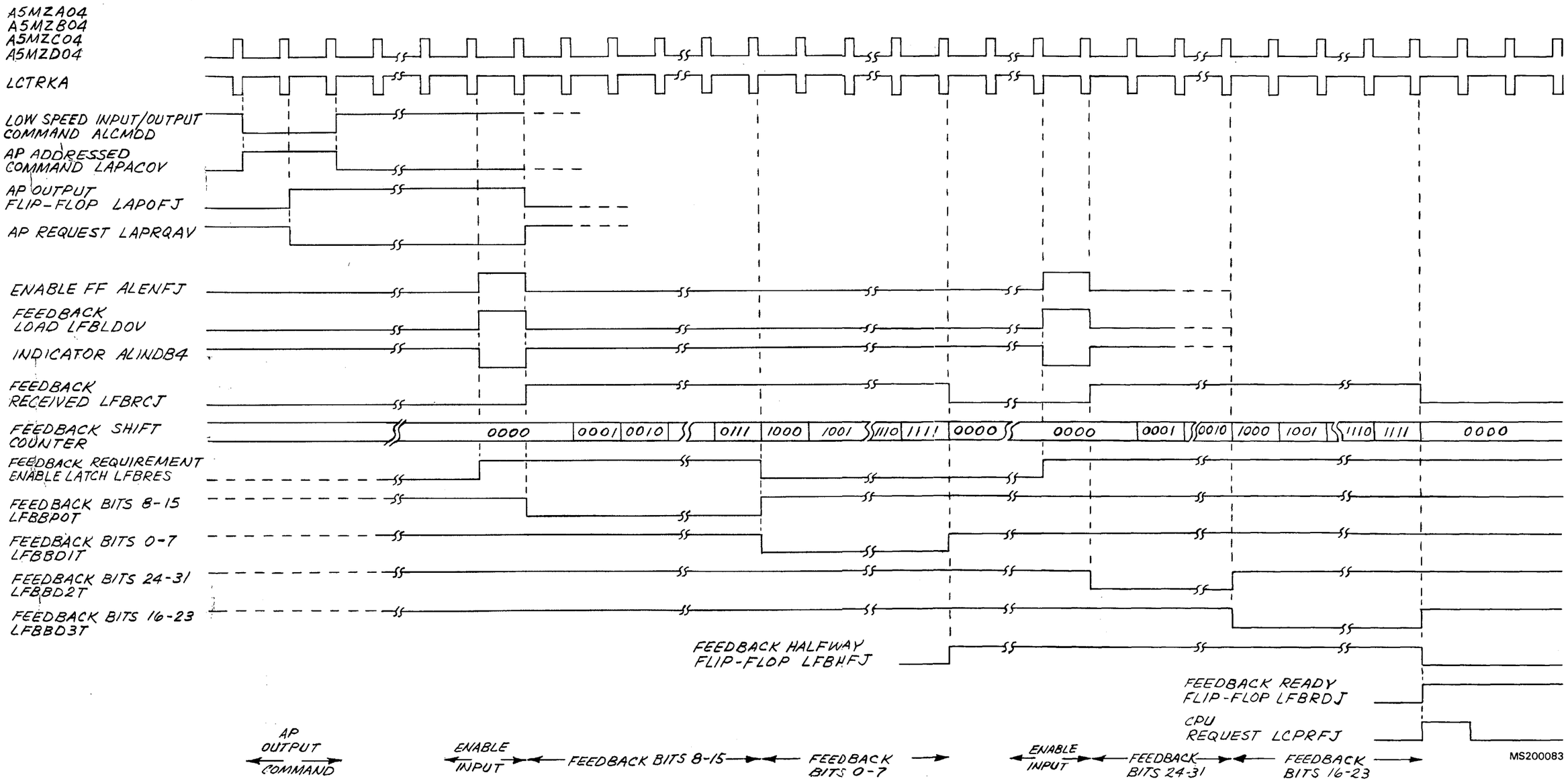

Figure 5-79. Computer Buffer/C-BIT Feedback Timing Diagram

Table 5-33. Feedback Decoder Inputs and Outputs

Inputs				Feedback shift bits			
A3	A2	A1	A0	8-15	0-7	24-31	16-23
L	L	L	L	L	H	H	H
L	L	L	H	H	L	H	H
H	L	H	L	H	H	H	H
L	L	H	L	H	H	H	H
L	L	H	H	H	H	H	L

warded to the AP 8-input mux for inclusion in the console status message. This indication is also supplied to the DOU fault sensor for inclusion in an ITR message in the event that mode of operation is in progress. The DOU memory timeout and CPU memory parity error indications are also supplied to both the 8-input mux and the DOU fault sensor.

j. During initial startup, the radar only display input enables the DOU inhibit bus. When the DOU INHIBIT OVERRIDE switch is activated, the bussed DOU inhibit is also supplied to the DOU fault sensor for inclusion in a required ITR message.

5-54. Input/Output Control Detailed Description (fig. 5-80, FO-51). The I/O control logic consists of the following elements:

Input byte detect
Parity bit detect
Byte detect
Byte examine enable
Output byte examine
Operation register load
ITR circuit
Operation register
ITR maintenance mode
Byte timing flip-flop 1
Byte timing flip-flop 2
Feedback last byte
Byte latch clear
Counter not terminated
Input buffer enable
Output timing
ITR abort
Byte count advance input
Output delay counter
Output delay between byte
Byte move input
Set byte counter advance
Byte counter command clock
Output strobe
Byte 2 = last
Parity terminate
Byte 2 terminate
Byte count advance flip-flop
Byte counter clock
Byte move output
Byte counter
Byte move

The I/O control provides input byte detection, input control word operation decoding, and I/O byte timing for the computer buffer/C-BIT. The control word operation codes are listed in table 5-34. The type of DEV operation is indicated by bits 0-2 in the associated data byte. An active bit 0 is device normal (DEV-1); an active bit 1 is device reset (DEV-2); an active bit 2 is device maintenance (DEV-3).

a. During input data processing, an OFR input logic sequence, as illustrated in figure 5-81, is performed. The interface timing is shown in figure 5-82. The timing diagrams show an OFR command sequence for which the IOX transmits a command signal accompanied by an address byte, followed by an operation control byte and 4 bytes of data. A ONE on any one of the interface bit lines or on the input parity line initiates a byte detection timing sequence which synchronizes the input data to the display console clock. The byte timing flip-flops provide a three count sequence which permits the computer buffer/C-BIT logic to accept the input byte and then clears the input data latches in the I/O register in preparation for the next input byte.

b. An OFR operation must be preceded by a DEV-3 operation which places the display console in the maintenance mode. The OFR operation is initiated by a command signal accompanied by an address byte. In the quiescent state, the 8-bit byte counter is loaded with 11110001, placing an enable on the byte counter command clock gate. The console address selected input, in conjunction with the trailing edge of the command input, then increments the byte counter to 1111 0010. The logic is now prepared to process the operation control byte.

c. The input operation control byte initiates a second byte detect timing sequence. Setting the byte timing 1 flip-flop enables the byte count advance input

Table 5-34. Input Control Byte Operation Codes

Control byte active bits	Data byte active bits	Function
0 and 3	0	Device normal (DEV-1)
0 and 3	1	Device reset (DEV-2)
0 and 3	2	Device maintenance (DEV-3)
0 and 4		Output from register (OFR)
0 and 5		Input to register (ITR)
0 and 6		End of block (EOB)
0 and 7		Device stop (STOP)

gate to set the byte count advance flip-flop. The byte counter is then incremented by the next clock. The set conditions of the byte timing 1 and 2 flip-flops enable the byte examine enable gate. In addition, since input bit 0 must be a ONE for a command control word, the output byte examine gate is also enabled. As long as no parity error is detected for the input byte, the operation register load and ITR circuit is enabled. The OFR operation (control bits 0 and 4 active) is then stored in the operation register. The logic is now prepared to process the 4 OFR data bytes.

d. The reception of input byte 1 again initiates the byte detect timing sequence. Setting byte timing flip-flop 2 results in a high byte move signal which loads the initial input data byte into the most significant stage of the i/o register. The active byte timing flip-flop 1 output also allows the byte counter advance flip-flop to be set by the next clock and the byte counter to be incremented by the succeeding clock.

e. Input bytes 2, 3, and 4 are processed in an identical manner. The byte move signal loads the current input byte into the I/O register most significant stage and prior input bytes are stepped into succeeding stages. Each input byte steps the byte counter until, at byte count six (1000 0000), the CPU indicator signal is supplied from the I/O register. This generates the byte terminate signal, which initializes the byte counter with a 1111 0001 count and clears the operation register, preparing the I/O control logic for the next input or output sequence.

f. For a DEV operation, the IOX issues a command signal accompanied by an address byte, followed by a control byte and I data byte (see fig. 5-82). The command signal triggers the byte counter and the control word DEV operation (bits 0 and 3 active) is loaded into the operation register. The input data byte is then detected and stored by the byte move signal. However, since only I data byte is utilized during a DEV operation, the CPU indicator signal is received at byte count 3, generating the byte counter terminate signal, reinitializing the byte counter, and clearing the operation register. While the DEV operation is stored, outputs are supplied to external computer buffer/C-BIT logic to determine whether the operation is a device 1 (for normal display refresh input operation), a DEV 2 (for software console reset), or DEV 3 (for console maintenance mode). After the operation register is cleared and as long as no high speed input buffer test is required, the input buffer enable is forwarded to the AP, permitting display refresh data to be accepted.

g. For an EOB operation, the command signal and address byte are followed by the usual control byte but no data byte is required (see fig. 5-82). Thus, the byte counter is terminated by the byte count 2 signal, reinitializing the I/O control logic. A STOP operation (0 and 7 control byte bits active) forwards a level to the initialization logic, halting any current operation and resetting all pertinent logic.

h. Output data processing (fig. 5-83) illustrates the timing and control sequence required to transfer a console status word from the computer buffer/C-BIT to the IOX. Interface timing is shown in figure 5-84. The illustrated sequence is preceded by the generation of a request signal to the IOX indicating that a console status word is stored in the I/O register (see fig. 5-84). When the IOX responds with an enable signal and the appropriate console address byte, the computer buffer/C-BIT will shift the 4 console status bytes to the IOX.

i. An active signal on any one of the interface bit lines or the input parity bit line initiates a byte detect timing sequence. The input enable signal is combined with a 5-MHz clock in order to synchronize the timing sequence with the display console clock. The enable signal is combined with the feedback ready signal and byte timing flip-flop output to enable the output timing circuit. This places a set enable on the output timing circuit and a load enable on the output delay counter. The output timing circuit is set by the next 10-MHz clock while the output delay counter is loaded to a 1101. The

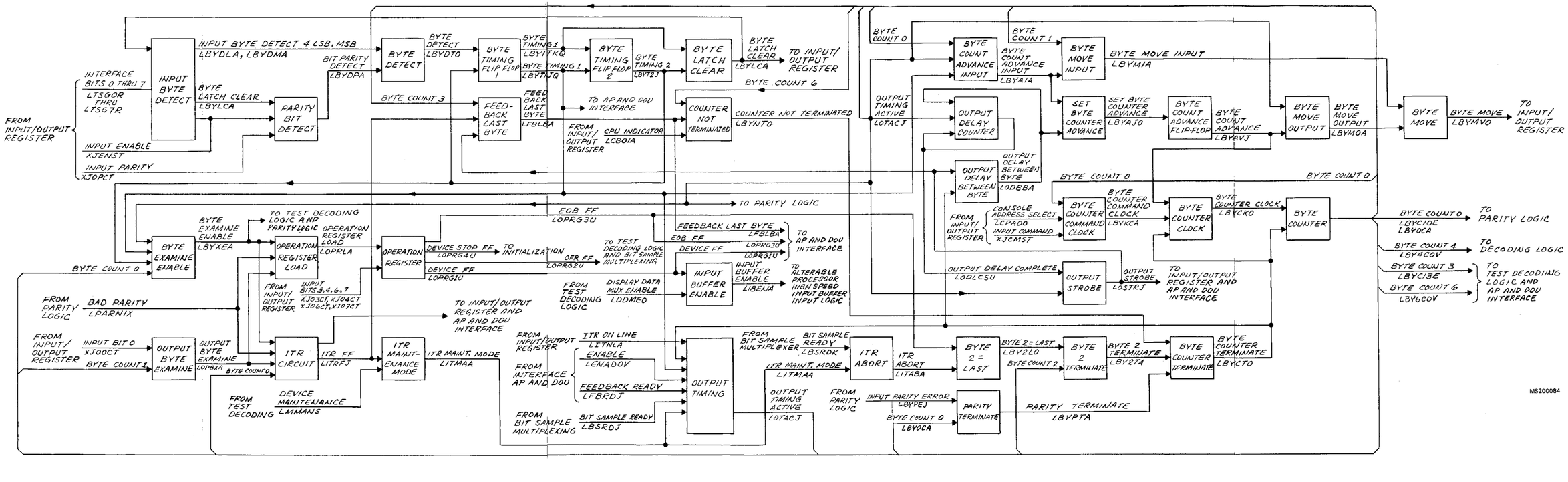

Figure 5-80. Input/Output Control Block Diagram

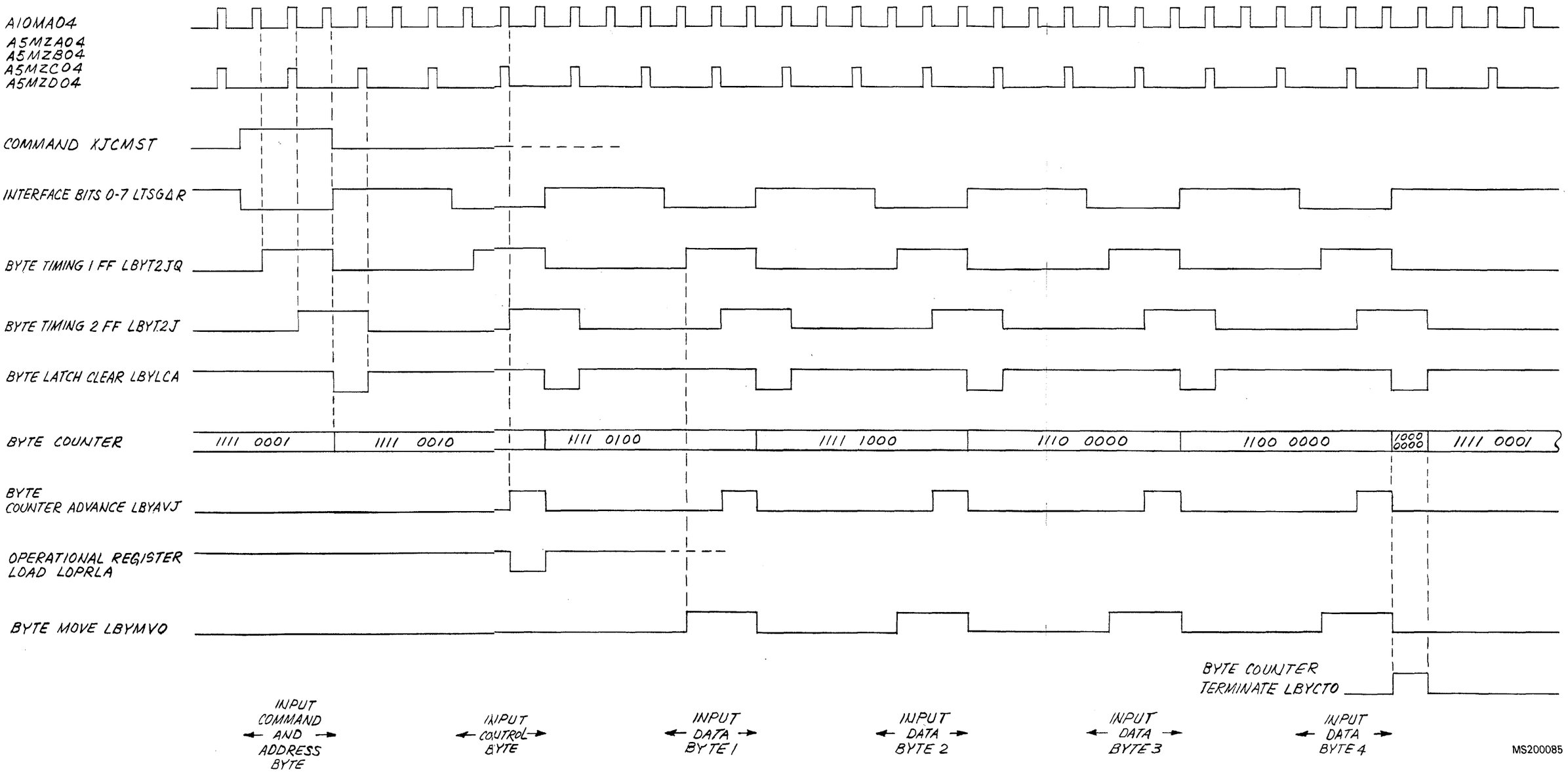

Figure 5-81. Timing and Control OFR Input Logic Timing

5-401/(5-402 blank)

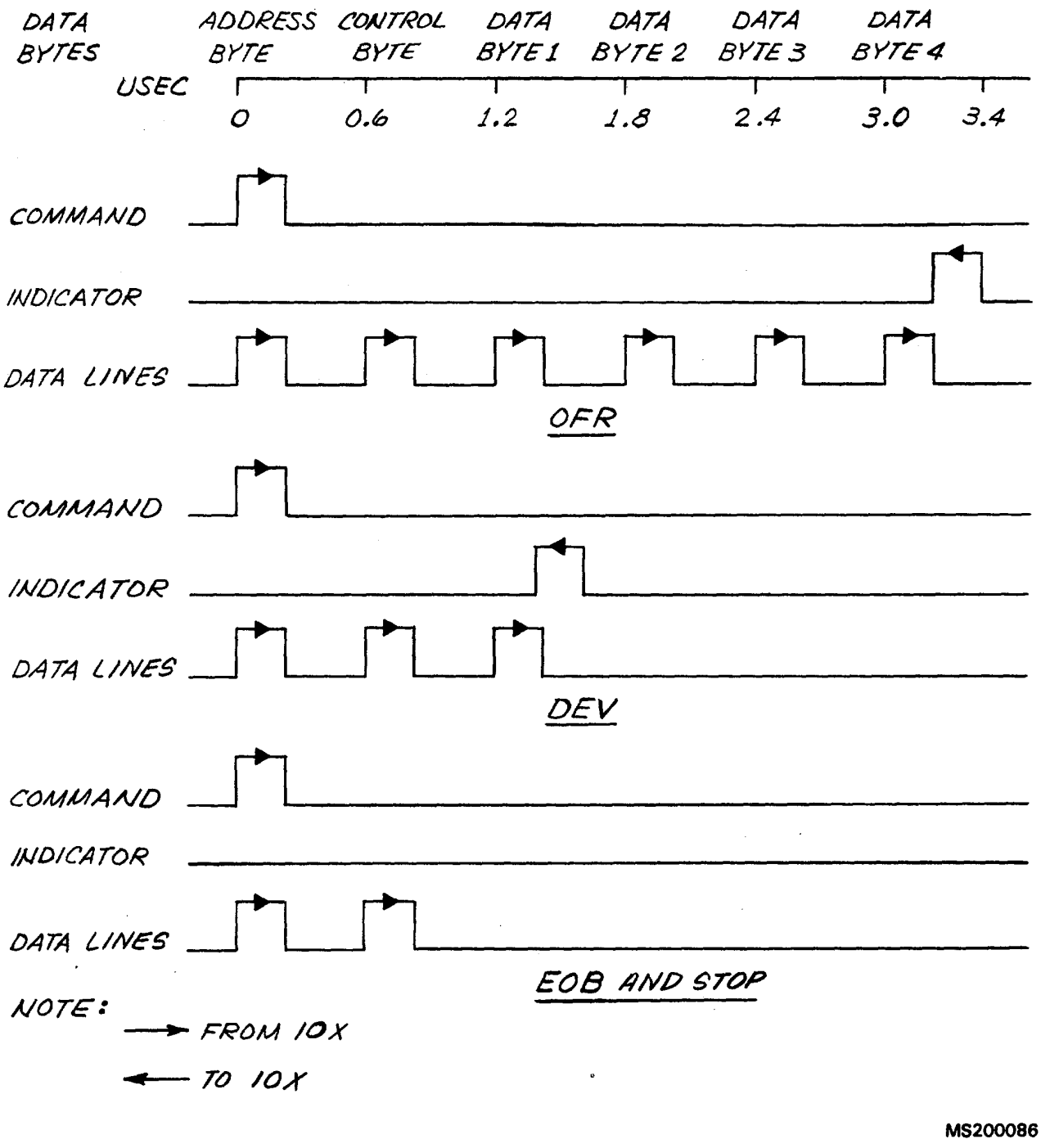

Figure 5-82. OFR, DEV, EOB and STOP Interface Timing

output delay counter is utilized to provide a delay between output bytes imposed by the IOX interface (a minimum of 400 Us). This counter is incremented by a 5-MHz clock and, upon reaching a 1111 count, places a set enable on the output strobe circuit. Setting the output strobe circuit transfers the initial console status byte to the l/O latches, initiating a byte detect timing sequence. The active output strobe signal also results in a load enable to the output delay counter and a set enable to the byte counter advance flip-flop. The output delay counter is then reloaded with 1101. Setting the byte advance flip-Hop generates a byte move enable to the l/O register. At the end of this clock time, the l/O data latches are cleared, the 3 remaining console status bytes are each stepped one stage in the I/O register, and the byte counter is incremented by one.

j. Console status bytes 2, 3, and 4-are transferred to the IOX in an identical manner. When the output strobe circuit sets for console status byte 4, the byte counter is in a 1111 1000 state or byte count 3 active. This enables the feedback last byte gate to generate the byte counter terminate signal, which reinitializes the byte counter, returning the l/O control logic to the quiescent state.

k. Data outputting is also initiated by an ITR operation for which the computer buffer/C-BIT returns the BIT sample collected as a result of a previous OFR operation. For an ITR operation, the IOX issues a command signal accompanied by an address byte and then a control byte. The computer buffer/C-BIT then transmits the 2-byte BIT sample word to the IOX followed by the 2 least significant bytes of the OFR word. The address and control bytes are detected and processed in an identical manner as described for the input data command operations. The command signal initially increments the byte counter to 1111 0010. The ITR circuit is set by each command control byte. As long as the console is in the maintenance mode (an OFR and ITR operation sequence must be preceded by a DEV-3) and the BIT sample ready line is active, the output timing circuit is set, initiating the 4-byte output sequence. Since the command signal incremented the byte counter at the beginning of the operation, the feedback last byte gate is inhibited from terminating the byte counter at count 3. instead, the CPU indicator is generated after the 4th byte is transferred, reinitializing the byte counter and resetting the ITR circuit. Note that if the sample is not ready when the ITR maintenance mode is enabled, the ITR abort gate generates the byte terminate signal at byte count 2, effectively ignoring the ITR instruction. Any parity error detected during any operation will also terminate the byte counter.

5-55. BIT Sample Multiplexing Detailed Description (fig. 5-85, FO-52 The BIT sample multiplexing logic consists of the following circuits:

Input buffer wait
Left side BIT sample enable
Right side BIT sample enable
BIT sample shift gate
BIT sample disable
BIT sample shift
BIT sample address counter
C-BIT enable decoder
LSB BIT sample shift
MSB BIT sample shift
BIT sample ready
BIT sample ready reset
DC low speed output data mux bits 00-09
DB output data low and high byte mux
DC file data low and high byte mux
DC program data low and high byte mux
DC command register data low and high byte mux
DC program address bits 00-07 mux
DC program address and bus select mux
DC ALU function mux
Right side BIT data mux A, B. and C
AP low speed data low and high byte mux
AP R/W memory data low and high byte max
AP input buffer data low and high byte mux
AP file data low and high byte mux
AP program command data low and high byte mux
AP command register data low and high byte mux
AP program address bits 00-07 mux
AP program address and bus select mux
AP ALU function mux
Left side BIT data mux A, B. and C
C-BIT enable decoder
X counter low and high bit mux
X counter mux out
Y counter low and high bit mux
Y counter mux out
Character generator mux A and B
Character generator mux out
Analog digital converter
Analog bit mux A and B
Analog bit mux out
Serial feedback data
Left side serial data

The BIT sample multiplexing logic controls the sequence of BIT sampling and routes the selected BIT sample word from the circuit being tested to the l/O register.

a. BIT sample shifting is enabled when the OFR operation is currently active and all console junctions that could interfere with the BIT sample are quiescent. The input buffer wait circuit is set as long as no DOU data is being input to or output from the high speed input buffer. When in the test maintenance mode, the TI wait signal indicates that the AP timing sequence is being temporarily interrupted for a BIT sample operation. The condition generates the left side BIT sample enable. The right side BIT sample enable going active indicates that the DB. DC, VC, and DG are quiescent. These conditions will set the BIT sample shift circuit and load the BIT

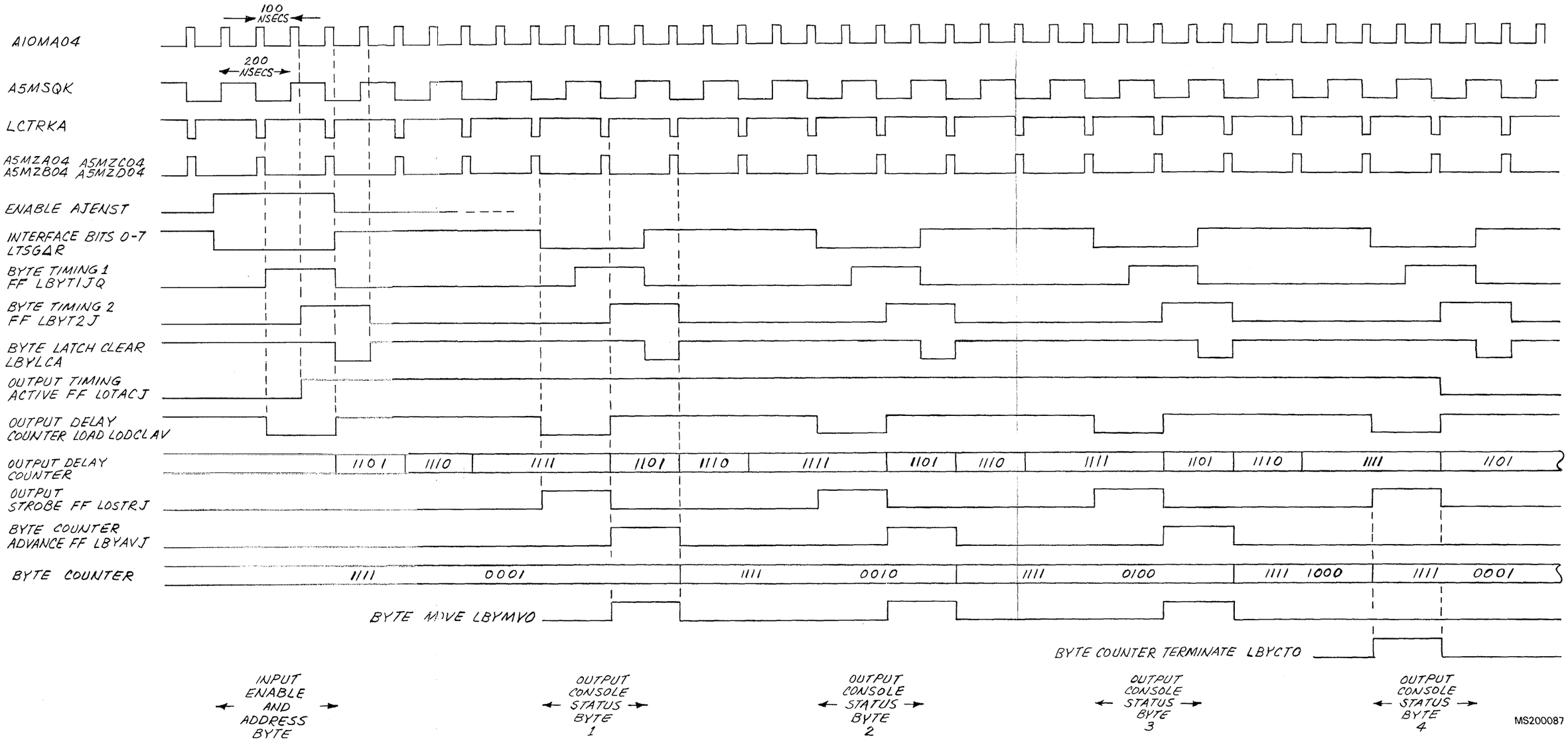

Figure 5-83. Timing and Control Status Word Output Logic Timing

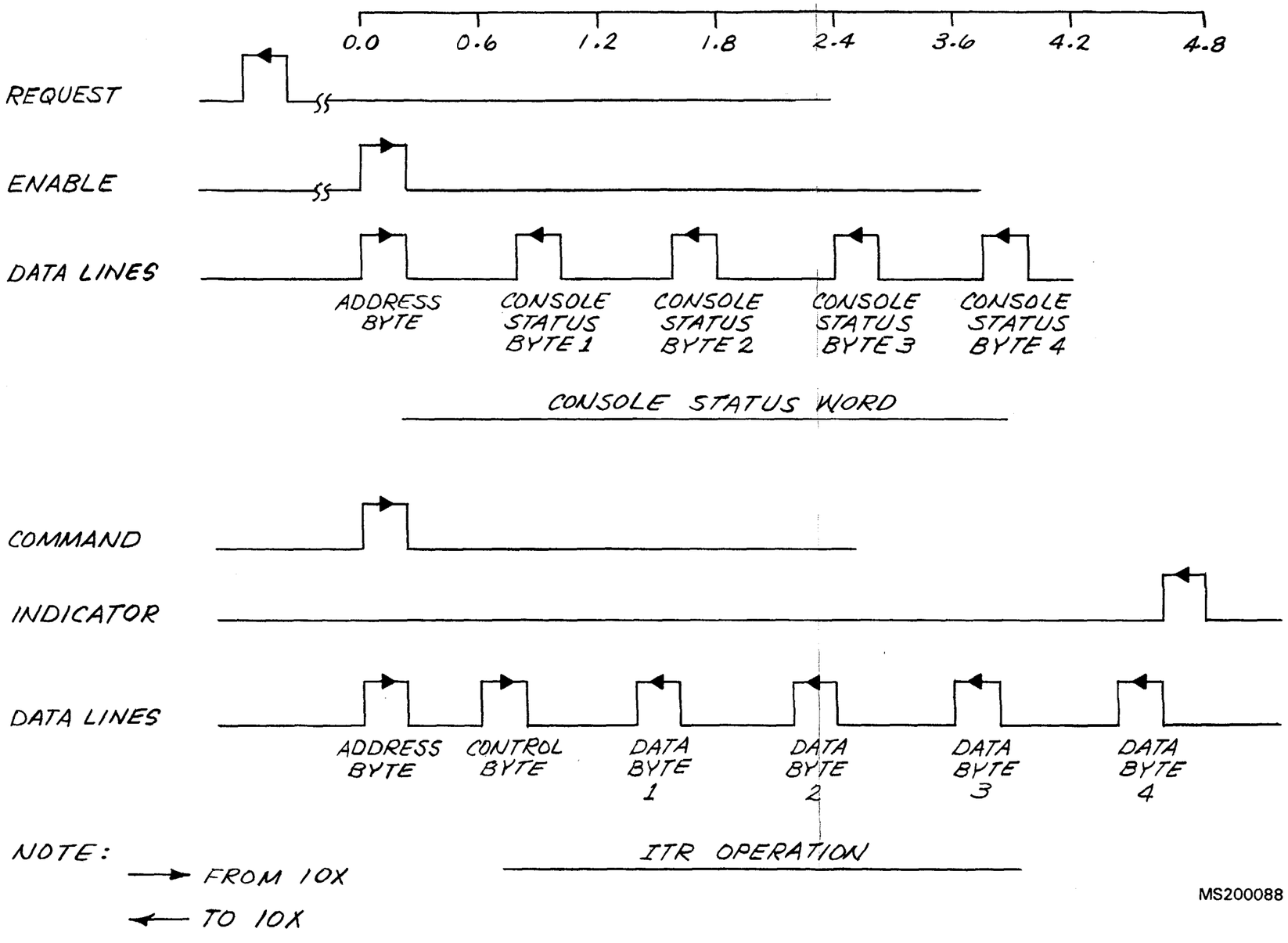

Figure 5-84. Console Status Word and ITR Operation Interface Timing

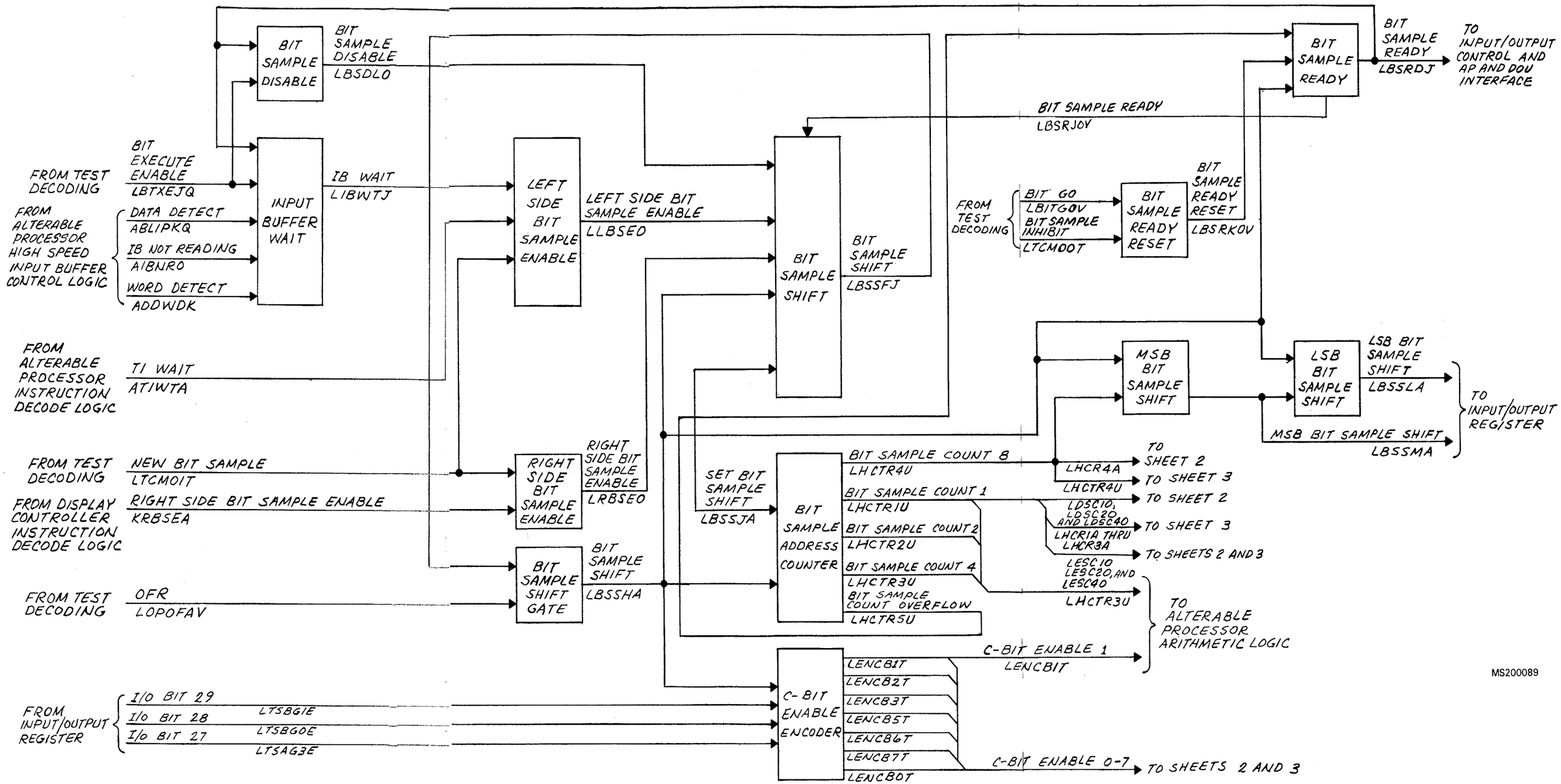

Figure 5-85. BIT Sample Multiplexing Block Diagram (Sheet 1 of 3)

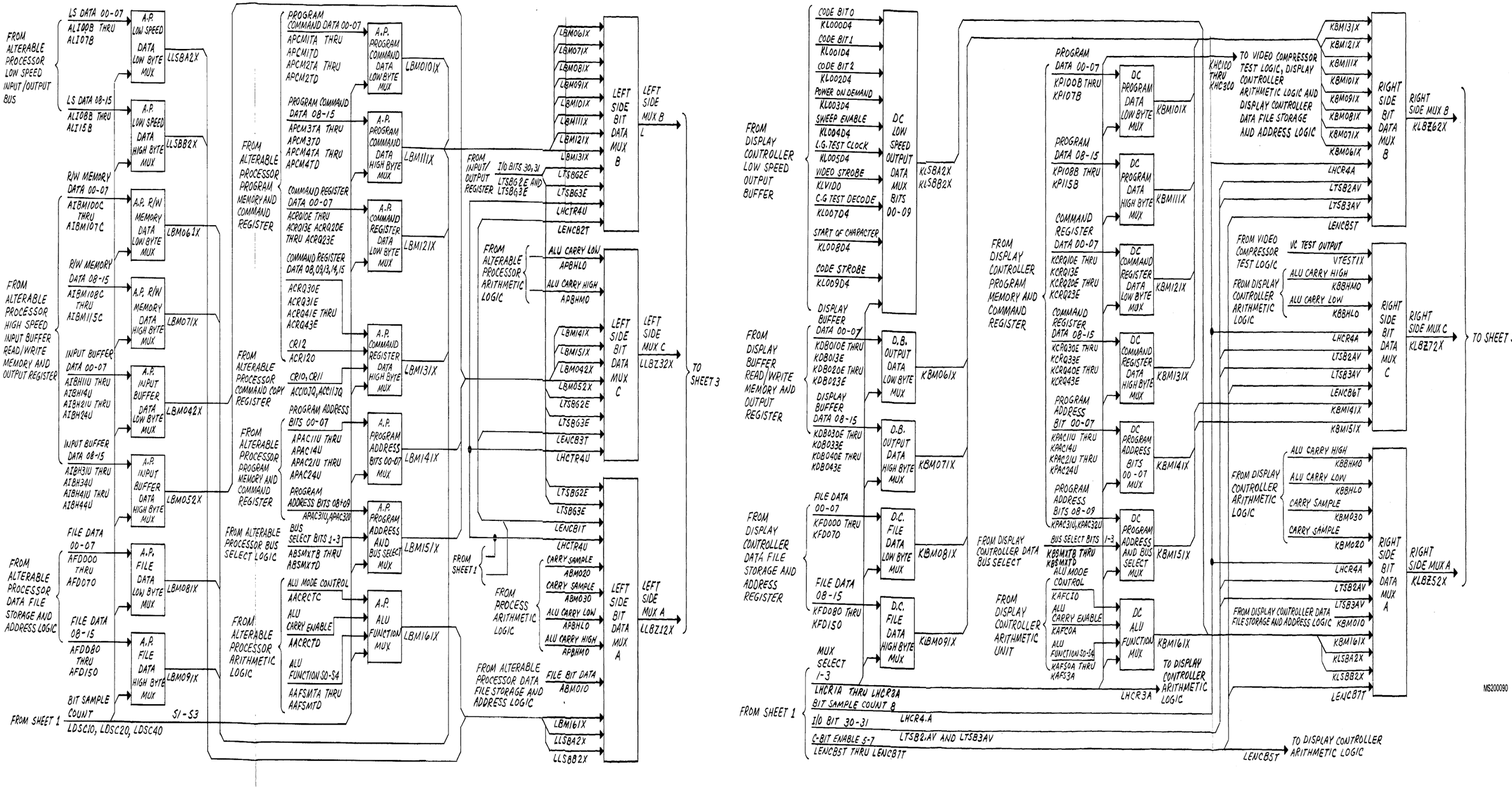

Figure 5-85. BIT Sample Multiplexing Block Diagram (Sheet 2 of 3)

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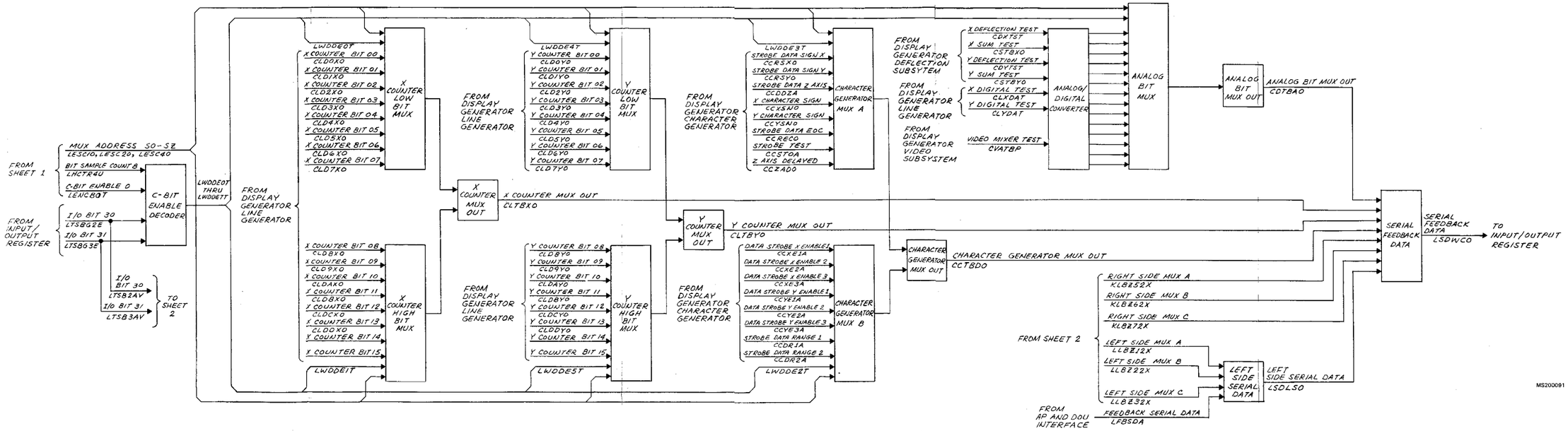


Figure 5-85. BIT Sample Multiplexing Block Diagram (Sheet 3 of 3)

sample address counter. As long as an OFR operation is in progress, setting the BIT sample shift circuit enables the C-BIT enable decoder, permits the BIT sample address counter to be incremented, and forwards the LSB BIT sample shift signal to the I/O register.

b. The BIT sample address counter generates a 16-count sequence utilized in the multiplexing logic to serialize the 16-bit parallel input data. When a count of eight is reached, the MSB BIT sample shift is enabled, disabling the LSB BIT sample shift. This ensures that the 2nd byte is shifted into the proper I/O register stage.

c. The C-BIT decoder combines BIT sample address I/O bits 27 thru 29 to provide an active signal on one of eight C-BIT enable lines. This enable, combined with bits 30 and 31, will select one of the BIT sample mux inputs for routing to the I/O register. Table 5-35 details the BIT sample information provided for the various BIT sample addresses.

d. When the BIT sample address counter reaches a count of 16, BIT sample shift is reset and BIT sample ready is set. Resetting the BIT sample shift disables the BIT sample address counter and the C-BIT enable decoder. Setting the BIT sample ready temporarily disables any new BIT sample shift operation, and informs external computer buffer/C-BIT circuitry that the BIT sample word is stored in the I/0 register and is prepared for transmission to the IOX. BIT sample ready will remain set until the BIT GO signal becomes active, indicating that the IOX has supplied a new OFR operation requesting a new BIT sample. Note that BIT sample ready is also reset by the BIT sample inhibit test command. This prevents any collection of a new BIT sample, and the IOX is supplied with the OFR data currently contained in the I/O register.

e. Fifteen muxs, controlled by the BIT sample count, serialize the 8-bit bytes from the various AP information lines. The mux outputs, in addition to serialized data from the arithmetic logic and the data file storage and address logic, are supplied to the input of three left side BIT data multiplexers. The C-BIT enable is used to enable an addressed multiplexer. The information source is determined by the BIT sample count input. BIT sample count 4 bits is used to select the least or most significant BIT sample byte. An array of multiplexers perform the identical function for the right side BIT sample information lines from the DC and the VC test logic.

f. Multiplexers are provided to select C-BIT samples from the DG. The selected serial data is routed through the serial feedback data gate to the I/O register. This line is also used for the console status serial feedback data from the AP and DOU interface.

5-56. Initialization Detailed Description (fig. 5-86, FO-53). The initialization logic consists of the following elements:

Master reset
Display console reset
Console reset
Radar only display enable
Reset clock
AP and DC reset

The initialization logic combines the various reset indication and distributes the reset signals to various console logic. The coincidence of the command and enable signals from the IOX sets the master reset. Any one of the master reset, reset operation, CONSOLE RESET switch action, or a device stop operation sets the console reset generating a single pulse reset signal which initializes all pertinent console logic. During a maintenance mode operation (BIT go active), the AP-DC reset test command initializes only those pertinent circuits in the AP and DC. The radar only display enable is generated when the CONSOLE RESET switch is activated. In this mode, DOU data is inhibited and only radar data is displayed.

Table 5-35. MUX Addresses and Bit Data

MUX address OFR and ITR							Bit sample (ITR)														
(HEX)		27	28	29	30	31	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	0	M ← CENTER SECTION ANALOG TEST BITS → L															
0	1	0	0	0	0	1	M ← CENTER SECTION LINE GEN. Y → L															
0	2	0	0	0	1	0	M ← CENTER SECTION CHAR. GEN. → L															
0	3	0	0	0	1	1	M ← CENTER SECTION LINE GEN. X → L															
0	4	0	0	1	0	0	M ← AP LOW SPEED I/O BUS → L															
																	AP ALU CONTROL					
0	5	0	0	1	0	1	M ← AP FILE ADDRESS →						L		X		X		$\overline{CO}$	M	$\overline{S3}$	$\overline{S2}$	$\overline{S1}$	$\overline{S0}$
								AP ALU "AND"					AP ALU CARRY LOGIC										
0	6	0	0	1	1	0	0-3		4-7		8-11		12-15		C12		C-8		C-4		C-16		P15		P11		G11		P7	G7	P3	G3
0	7	0	0	1	1	1	M ← AP DATA BUS → L															
0	8	0	1	0	0	0	M ← AP INPUT BUFFER MEMORY → L															
0	9	0	1	0	0	1	M ← AP FILE DATA → L															
0	A	0	1	0	1	0	M ← AP PROGRAM MEMORY → L															
0	B	0	1	0	1	1	M ← AP COMMAND REGISTER → L															
								AP BUS SELECT														
0	C	0	1	1	0	0	X		$\overline{S2}$		$\overline{S1}$		$\overline{S0}$		X		X		M ← AP ORIGRAM ADDRESS → L			
0	D	0	1	1	0	1	M ← AP INPUT BUFFER RECEIVING REG. → L															
0	E	0	1	1	1	0	M ← AP HIGH SPEED OUTPUT REG. ← L															
0	F	0	1	1	1	1	UNASSIGNED															

Table 5-35. MUX Addresses and Bit Data - Continued

MUX address OFR and ITR							Bit sample (ITR)													
(HEX)		27	28	29	30	31	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	0	1	0	0	0	0	UNASSIGNED															
1	1	1	0	0	0	1	UNASSIGNED															
1	2	1	0	0	1	0	UNASSIGNED															
							UNASSIGNED															
1	4	1	0	1	0	0	M ← DC LOW SPEED OUTPUT → L															
															DC ALU CONTROL							
1	5	1	0	1	0	1	M ← DC FILE ADDRESS → L								X		XO	M	$\overline{S3}$	$\overline{S2}$	$\overline{S1}$	$\overline{S0}$
							DC ALU "AND"								DC ALU CARRY LOGIC							
							0-3	4-7	8-11	12-15	C12	C8	C4	C16	P15		G15	P11	G11	P7	G7	P3	G3
1	7	1	0	1	1	1	M ← DC DATA BUS → L															
1	8	1	1	0	0	0	M ← DC DISPLAY BUFFER MEMORY → L															
1	9	1	1	0	0	1	M ← DC FILE → L															
1	A	1	1	0	1	0	M ← DC PROGRAM MEMORY → L															
1	B	1	1	0	1	1	M ← DC COMMAND REGISTER → L															
							DC BUS SELECT															
1	C	1	1	1	0	0	X	$\overline{S2}$		$\overline{S1}$		$\overline{S0}$		X	X		X	M ← DC PROGRAM ADDRESS →				L
1	D	1	1	1	0	1	UNASSIGNED															
1	E	1	1	1	1	0	M ← DC HIGH SPEED OUTPUT REG. → L															
1	F	1	1	1	1	1	X	X	X	X	X	X	X		RVM TEST				VID COMPRESSOR			

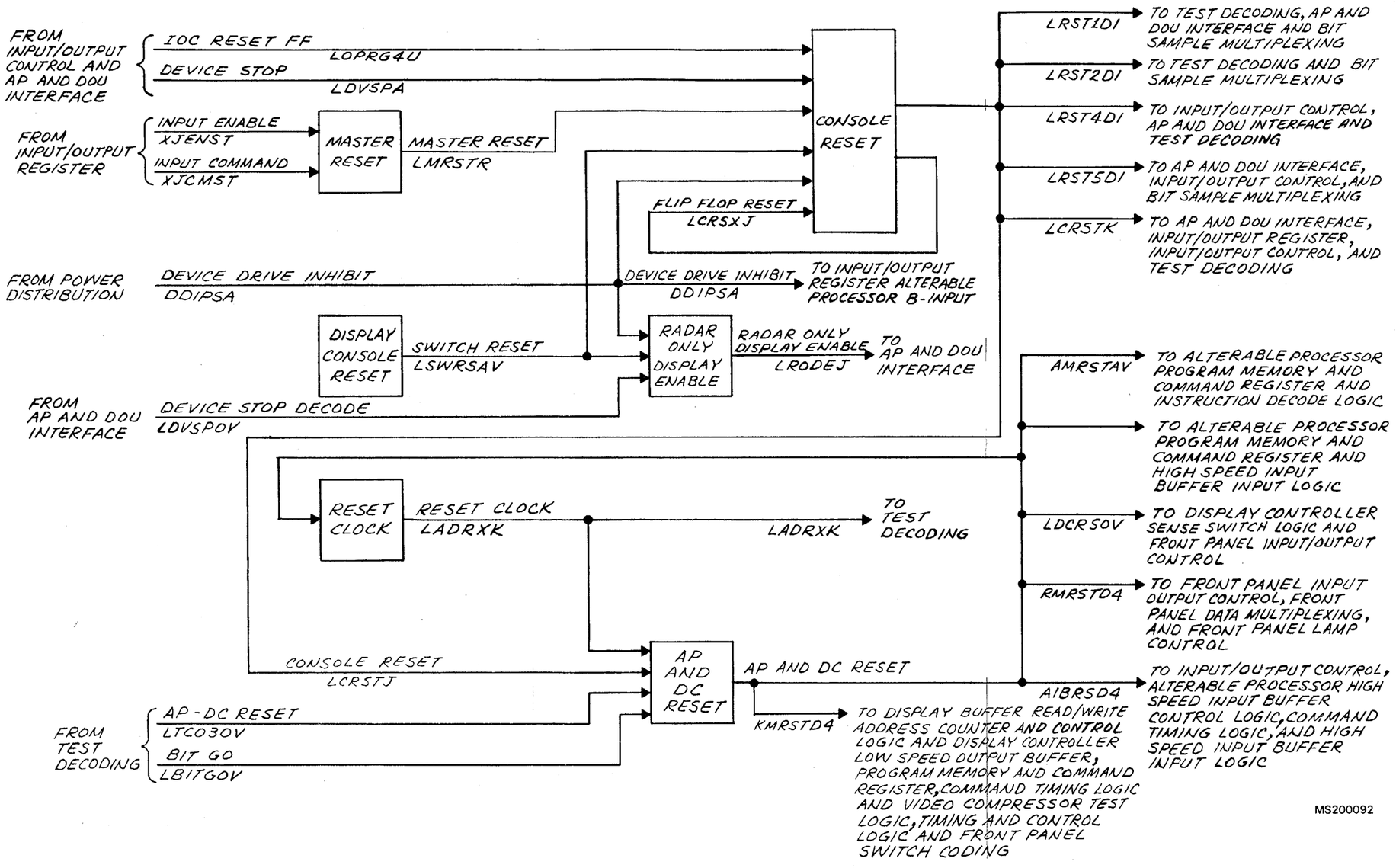


Figure 5-86. Initialization Block Diagram

Section X. CLOCK CIRCUIT

5-57. Clock Circuit Detailed Description (fig. 5-87, FO-54). The clock circuit contains the 20-MHz oscillator generator, pulse shaping logic, frequency dividers, buffers, and clock drivers required for clock timing by the display console functional circuits. Refer to figure 5-88 for display console clock phases and waveforms. The basic clock is generated by a free-running 19.6657-MHz (hereinafter referred to as 20-MHz) crystal oscillator which is applied to clock shaping logic. The clock shaping logic is controlled by a clock enable level from the test set which remains active during normal operating conditions. The clock shaping logic consists of a delay line and comparator flip-flop logic which ensures a symmetrical, 20-MHz square wave clock train. This clock train is supplied to frequency dividers and buffering logic for distribution to the appropriate logic. The 20-MHz clock is supplied directly as a video clock to the video subsystem and as a character/video clock to the deflection subsystem, character and line generator. Upon receiving a sweep video enable from the line generator, a 20-MHz buffer gate supplies a 20-MHz digital clock signal to the line generator. The sweep active level signal from the line generator enables the line clock buffer. The line clock buffer divides the basic clock signal by two and supplies the clock signal to the line generator as a line clock. Frequency divider A provides two 10-MHz signals and one 5-MHz signal for shaping, buffering, and distribution to the appropriate logic. When required, the 5- and 10-MHz clock trains are ANDed, removing relative logic delays and ensuring phase synchronized clock pulse trains to the display console functional circuits.

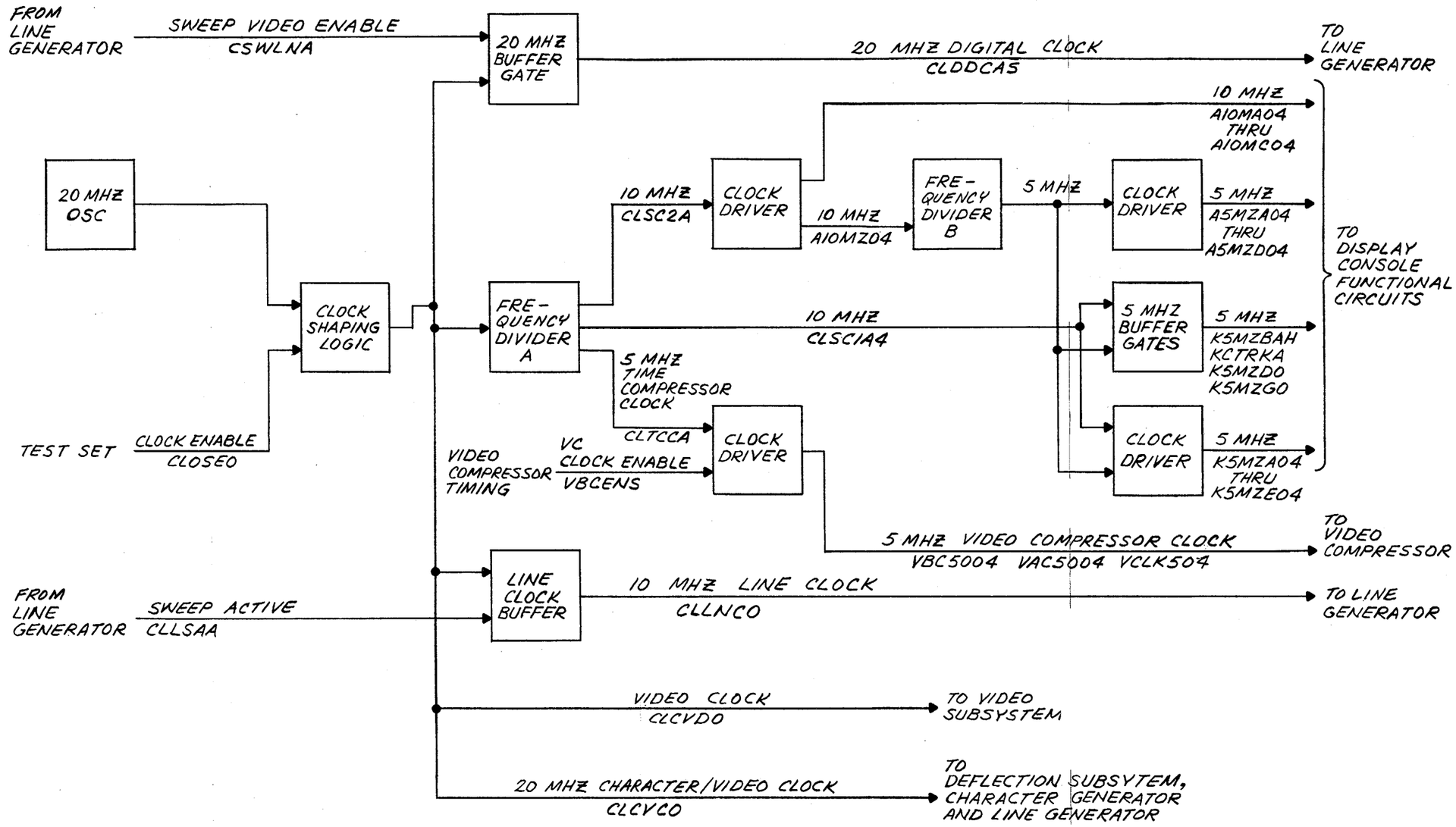


Figure 5-87. Clock Circuit Block Diagram

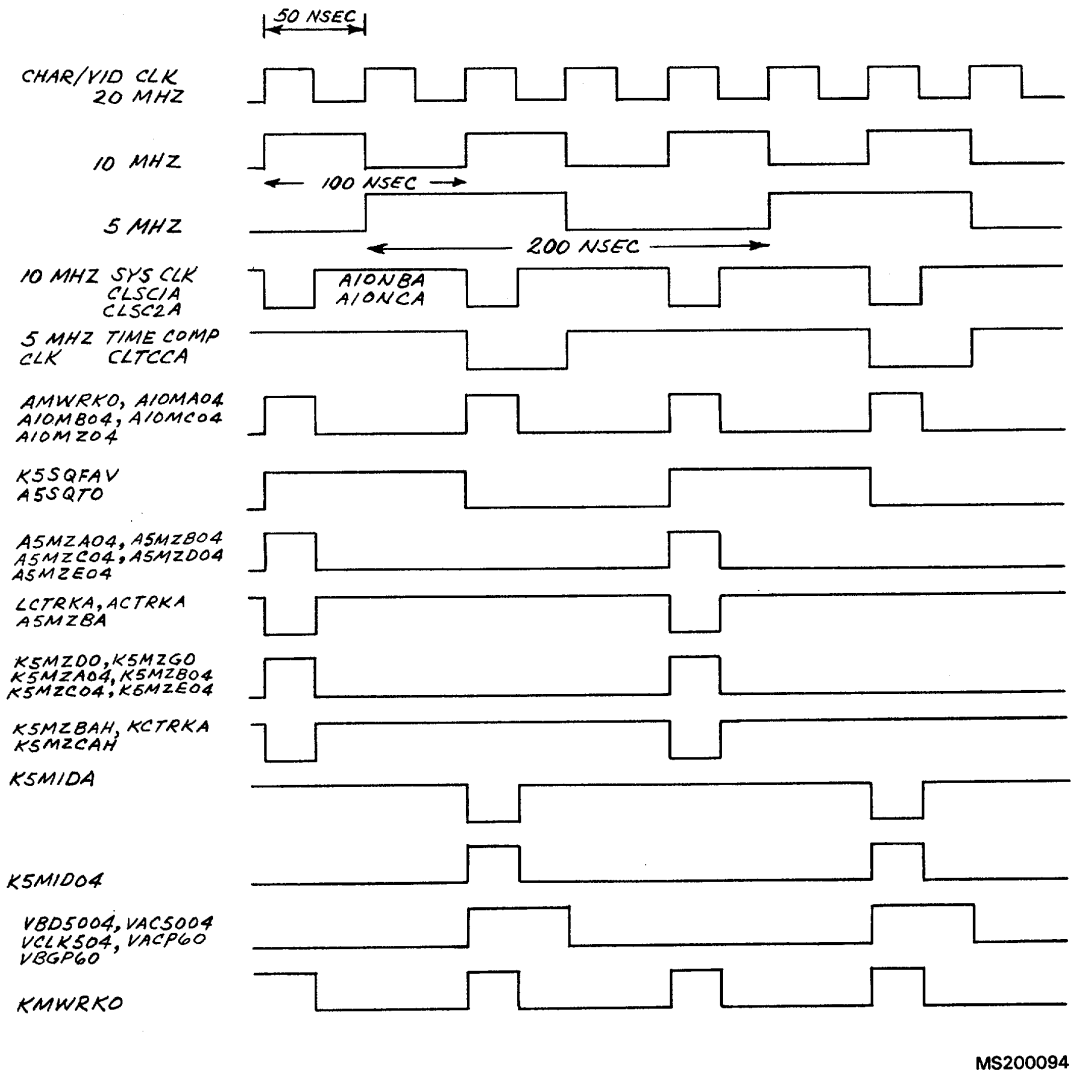


Figure 5-88. Display Console Clock Phase and Waveforms

Section XI. IOX AND DOU INTERFACE

5-58. IOX Interface (FO-55). The IOX interface provides communication between the display consoles and the ADP. Communication is provided through the ADP interface panel using information and control signal lines. The information lines permit bidirectional transmission of address, control, and data information between the display console and the IOX. The control signal lines direct the information flow between the display consoles and the IOX. The control signal lines consist of enable, command, indicator, and request.

5-59. DOU Interface (FO-56). The DOU interface provides the display consoles with synthetic data from the display refresh file (DRF) contained in the ADP memory. The complete DRF is transferred every 50 ms. Data is provided through the ADP interface panel using data lines fault and control signal lines. The data lines supply the DRF data to the display consoles as messages containing 32-bit words. The number of words in a message varies depending upon the message type. The fault signal lines indicate a message transfer malfunction either in the DOU or the display consoles. The control signal lines direct the data flow between the display consoles and the DOU. The control signal lines consist of request and inhibit, and the fault signal lines consist of memory timeout, parity error keyboard, parity error data, and overrun (memory).

Section XII. POWER DISTRIBUTION

5-60. Display Console Power Distribution (fig. 5-89, FO-57). The display console power distribution circuits consist of primary power, low voltage distribution, MTS interface card, console power fault monitoring, and high voltage protective circuits.

a. Primary Power. Primary power for the display console is provided by the system power cabinet. Primary power includes complementary +135v and -135v referenced to dc center tap (common) and single-phase, 120v, 400 Hz referenced to neutral (neutral is common to safety or frame ground through the power cabinet). Refer to paragraph 5-62 for primary power application in remote display console configuration.

(1) +135v and -135v is applied to dc/dc converters PSI thru PS3, variable lamp power supply PS4, and deflection amplifier power supply A2PS2 contained in the center section. Local turn on, turnoff, and power reset is controlled by the CONSOLE POWER-POWER ON switch located on the center section front panel.

(2) Ac power is used solely for fan assembly A4. The fan assembly is part of the display console cooling which is maintained through an external ventilation system.

b. *Low Voltage Distribution.* Low voltage distribution consists of low voltage outputs from the dc/dc converters and the variable lamp power supply. Refer to the detailed power distribution diagram for power application to the display console subassemblies. For card cage backplane distribution, + 5v and + 5v common are shown as common buses; these buses are insulated voltage and ground planes which form the backplane.

(*1) Dc/Dc converter PSI.* Dc/dc converter PSI contains three transformer-coupled, floating power sources which may be used for positive or negative voltage supplies. These voltage supplies include 12.5v, 5.5v, and 5.6v sources which are used for display console + 12v, + 5v, and - 5v distribution, respectively. A device drive inhibit signal is generated from PSI for power status logic and is applied to the computer buffer/C-BIT initialization circuit.

(*2) Dc/Dc converter PS2.* Dc/dc converter PS2 is identical to PSI. The 5.5v, 5.6v, and 12.2v sources are used for + 5v, - 5v, and - 12v display console distribution, respectively.

(3) Dc/Dc converter PS3. Dc/dc converter PS3 is similar to PSI and contains five power sources. The voltage supplies include 34.5v, two 15v, 5.0v, and -8.0v sources which are used for display console +34.5v, + 15v, + 5v and -8v distribution, respectively.

(4) Variable lamp power supply PS4. Variable lamp power supply PS4 is a dc/dc converter and provides a variable +5v output for front panel lamps. Dimming control is provided by the LAMP BRT control located on the center section front panel.

c. MTS Interface Card. The MTS interface card is normally installed in connector J15 adjacent to PS4; the card is accessible through a hinged door. When the MTS interface card is installed, +5v pullup resistor voltages (+5VRES1 thru +5VRES3), +34.5V, + 15VHV, and ground continuity is provided. When the MTS is used for an in-system card test, the MTS interface card is removed and the MTS umbilical cable W210 is connected to J15. This allows the MTS to provide isolated dc power for test purposes.

d. *Console Power Fault Monitoring.* Console power fault monitoring is accomplished through the CONSOLE OVER TEMP and CONSOLE POWER FAULT indicators located on the right hand front panel. In addition, the LAMP TEST switch, located on the center section front panel, permits periodic testing of power supplies and indicator lamps.

(*1) Console overtemperature. A* console overtemperature indication occurs when critical operating temperatures are reached in the center section deflection amplifier (AZAR1). During crt sweep generation, maximum power consumption in the display console occurs. Improper cooling or malfunction could result in an overtemperature condition. Two parallel thermostatic switches are mounted on X and Y deflection preamplifiers inside the deflection amplifier assembly. These switches close on increasing temperatures at 180 ^{o} F ± 14.4°F and provide a thermal interlock signal to the deflection amplifier power supply (A2PS2). Fault logic in the deflection amplifier power supply lights the CONSOLE OVER TEMP indicator, provides a DAPS fault signal to dc/dc converter PS3, and shuts down display console power. The DAPS fault signal causes an external fault indication on PS3 and lights the CONSOLE POWER FAULT indicator.

(*2) Console power fault.* Console power fault monitoring is accomplished through fault logic in dc/dc converters PSI thru PS3, variable lamp power supply PS4, high voltage power supply A2PS1, and deflection amplifier power supply A2PS2. Any high or low voltage power failure shuts down display console power and lights the CONSOLE POWER FAULT indicator. For a high voltage failure, the high voltage power supply provides an HV fault signal to dc/dc converter PSI to cause an external fault indication; a deflection amplifier power failure causes an external fault indication on PS3 (refer to para (1) above).

(3) Lamp test. A lamp test feature is provided for maintenance and test purposes. When the LAMP TEST switch is pressed, the internal and external fault lamps on

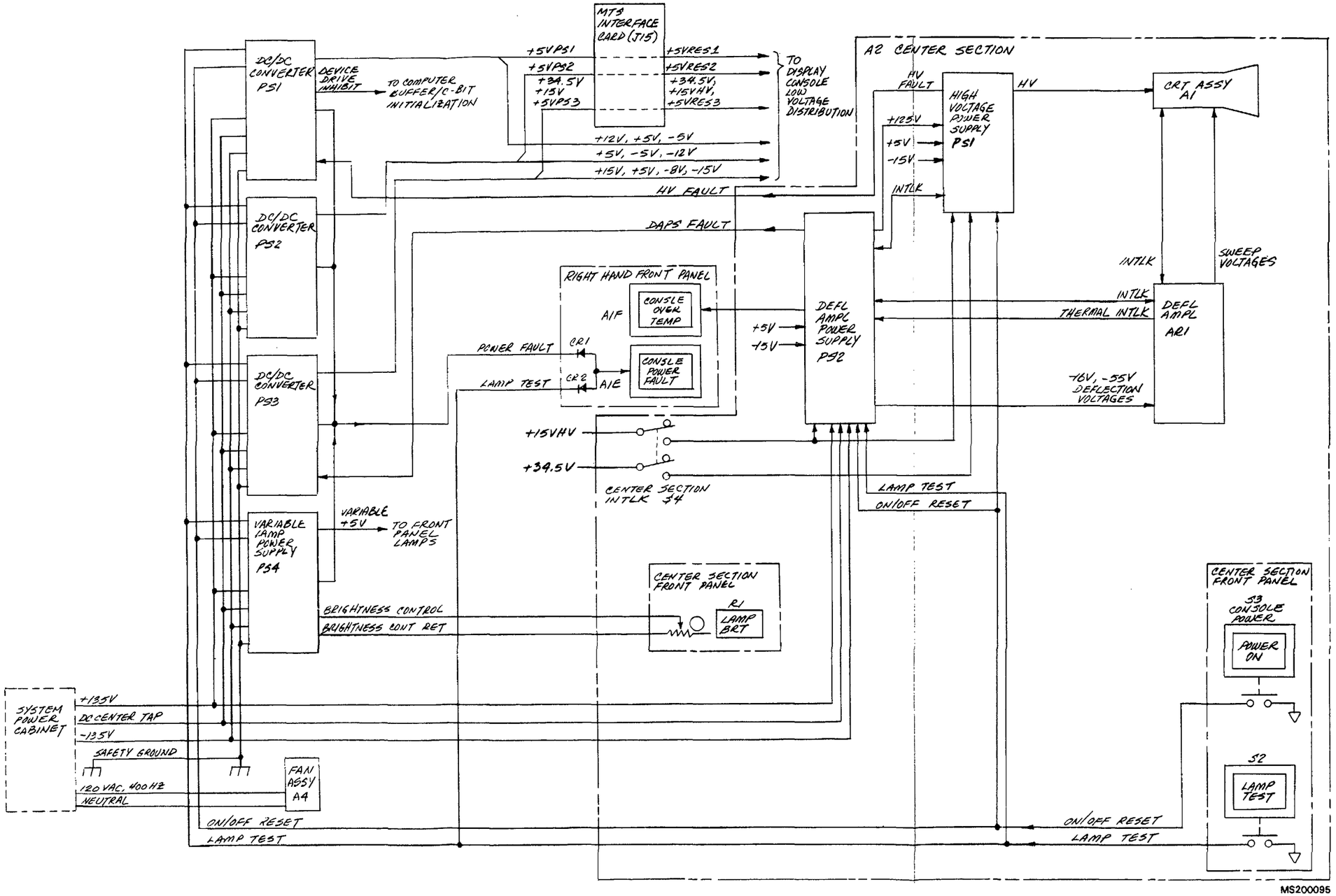


Figure 5-89. Display Console Power Distribution Block Diagram

5-431/(5-432 blank)

the dc/dc converters and the variable lamp power supply, the CONSOLE OVER TEMP indicator, and the CONSOLE POWER FAULT indicator light. The lamp test function is implemented in the respective power supply internal fault logic. The CONSOLE POWER FAULT indication and lamp test are implemented through diodes CR1 and CR2 which are mounted on the right hand card cage frame.

e. *High Voltage Protective Circuits.* High voltage protective circuits are provided by a continuity interlock and a chassis interlock switch. These interlocks provide high voltage protection in the display console center section.

(1) *Continuity interlock.* The continuity interlock consists of wired interconnections through the high voltage assemblies. When the crt assembly, deflection amplifier, deflection amplifier power supply, and high voltage power supply are properly interconnected, high voltage turn on is enabled.

(2) *Chassis interlock switch.* Interlock switch A2S4 automatically shuts down high voltage when the center section is extended from the display console. For maintenance, the interlock switch may be manually bypassed.

5-61. Remote Display Console Power Distribution (fig. 5-90, FO-58). For remote display configurations when display consoles are installed external to the system shelter, primary power is provided through the power cabinet power transfer unit to the display junction box.

a. *Power Transfer Unit.* The power transfer unit permits shelter power input and output interconnections while maintaining emi isolation. An independent ac/dc converter provides the +135v and - 135v primary dc power for remoted display consoles; in addition, phase B is used to provide the ac power for the display console fan assembly. The rear panel of the power transfer unit serves as a power demark panel where external power cables are connected. Remote display power application is controlled by the AC/DC CONVERSION NO. 2 circuit breaker on the power cabinet ac power panel.

b. *Display Junction Box.* The display junction box (unit 3) provides primary power outlets for an MTS and up to 10 display consoles. With ac/dc power available from the power transfer unit, the DC POWER AVAILABLE indicator is lighted; when the AC MASTER circuit breaker is placed to ON, the AC POWER AVAILABLE indicator is lighted. MTS power is available at connector J2; display console power is available at connectors J3 thru J12. Local circuit breakers, corresponding to the power connectors, are provided for independent power application.

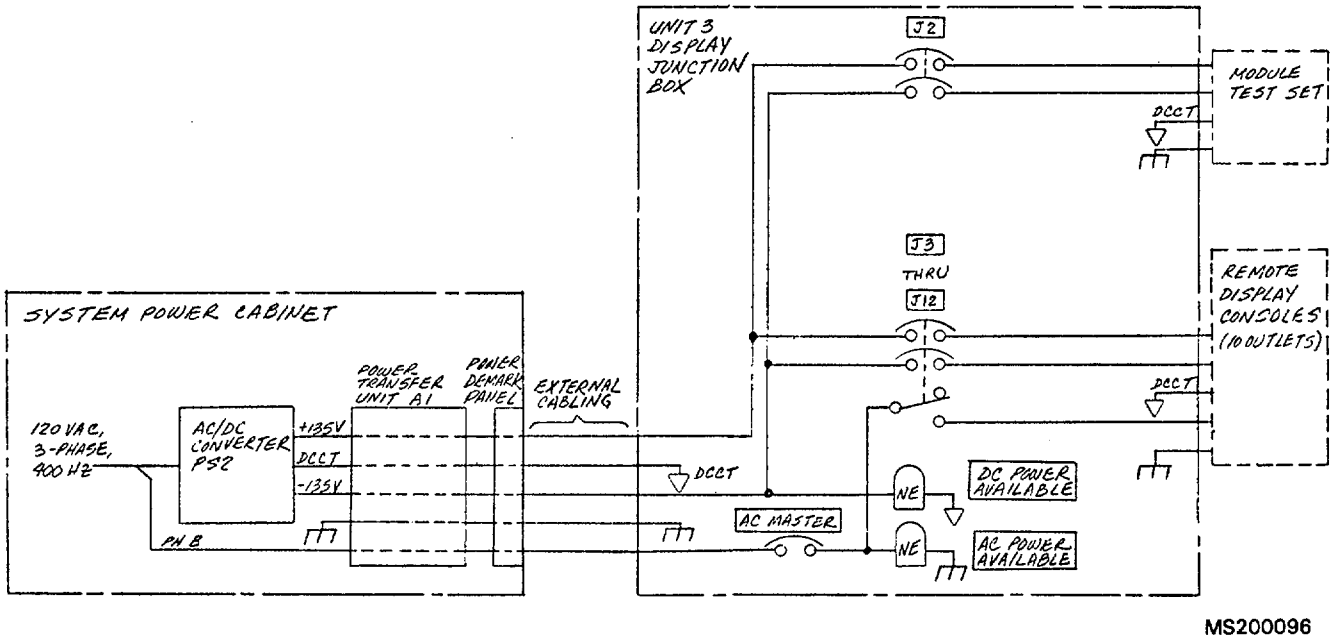


Figure 5-90. Remote Display Console Power Distribution Block Power

Section XIII. CABLING AND FRONT PANEL SCHEMATIC DIAGRAMS

5-62. Cabling Diagrams (FO-59, FO-60). The cabling diagrams are furnished to provide a means of identifying all elements of the equipment and to show how they arc electrically related. Included on the cabling diagrams are reference designators, part numbers, drawing (wire list) numbers, and references to cable wiring diagrams.

5-63. Front Panel Schematics (FO-61, FO-62, FO- 63). The left hand, center section, and right hand schematic diagrams are provided to identify controls and indicators and their electrical details. The primary purpose of the schematic diagrams is to illustrate pin arrangements and identify signal mnemonics associated with a particular control function.

Section XIV. AP AND DC PROGRAMS

5-64. AP and DC Program Description. This section provides a general description of the AP and DC program in addition to information on interpreting the various command codes and the resultant logical manipulations. The complete AP and DC program listing is detailed in tables 5-36 and 5-37. Information provided in tables 5-16 and 5-27, command word bit description, tables 5-17 and 5-28, source codes, should be referred to when analyzing the program listings.

a. The formats for the AP and DC programs are identical. The repertoire and manipulation of commands is very similar; therefore, only the AP program is described. Table 5-38 is an editorialized version of a portion of the AP sequence of commands utilized to initialize the console. The label is the program memory location in hexadecimal. This value will be automatically incremented after each command is implemented unless the sequence is altered by a branch or a skip. The operation column lists the hexadecimal value of the command word stored in the addressed memory location. The third column shows the binary construction of the associated 16-bit word and the significance of the operation code (bits 10 thru 14) and the utility field (bits 0 thru 9). The next column lists the command comments which are optional text used as programmer aids. The fifth column, when applicable, lists the programmer comments associated with the addressed storage (RAM) or constant (ROM) file location. Finally, a brief functional description of the particular command is provided.

b. When power is applied to the console, all pertinent bipolar logic is reset. After the power-on sequence is completed, the program address register is cleared and the AP commences processing the program from memory location 0000. Initially, the program resets all sense switches except sense switch 6 which indicates the initialization mode. The index register is then loaded with 007F (label 0002) which is binary 127, representing the most significant RAM address. The accumulator is loaded with all ZEROS (label 0003), which is stored in RAM location 127 (label 0004). The index register is now decremented to 007E (label 0005) and the program branched back (label 0006) to label 0004. This loop, which continues until the index register is decremented to 0000, clears all RAM storage locations.

c. The console is, at this time, in the radar only display mode. During this mode, the IOX and DOU are assumed to be offline, and the console program is dedicated to initializing the front panel lamps, responding to any operator switch actions, constructing the console status word, and preparing for DOU data processing. The remainder of the initialization program, as illustrated in table 5-38, can be seen to involve accessing various constants from the ROM and storing the processed values in the proper RAM locations. The continuation of the initialization program as provided in the listing (table 5-36) will clear all front panel lamps and set those lamps required to reflect the current mode of the console. The precise sequence of instructions is dependent upon any front panel switch action.

d. When the front panel lamps have been properly initialized, the program will enter a 50-ms loop to synchronize with the impending display refresh cycle. Console status words will be constructed arid passed on to the IOX as required. At this time, video data can be displayed and the general operational condition of the console can be observed and assessed.

e. When the ADP is prepared to enter the normal display refresh cycle, the IOX supplies a DEV-2 (reset) operation instruction, which terminates the radar only display mode and again initializes all logic. A DEV-1 (normal) operation instruction instructs the console to deactivate the DOU inhibit line and generate a DOU request. The DOU then commences to supply the train of messages constituting the display refresh file to the console. The initial word of a new message is logically detected and indicated by setting sense switch 9.

f. The program loop constantly tests the state of sense switch 9 and when the set condition is detected, the program enters the message processing phase. When the complete display refresh file has been transmitted, the DOU supplies an EOF message which causes the program to commence the console status report phase. This operation continues in the 50-ms display refresh cycle, continuously refreshing the display, responding to operator switch settings, and informing the IOX of console status.

Table 5-36. AP Program Listing

```
0000    07BF    PWRON   RSW     S0, S1, S2, S3, S4, S5, S6, S7, S8, S9
0001    0040            SSW     S6                      REMEMBER IN INITIALIZE
0002    6CBE            OFI     X7F                     LOAD INDEX
0003    30A5            CFA     XO                      LOAD ZEROES
0004    2200            STA     FILE, 1                 STORE' EM
0005    7400            DIS                             AGAIN?
0006    7804            CCB     *-2                     YES - GO BACK TWO SPACES
0007    30F1            CFA     R00F                            ASSUME RADAR ONLY UNTIL
0008    2047            STA     RONRO                           WE DISCOVER OTHERWISE
0009    34DB            CFO     XF7FF                   TO INIT COMPRESSOR RANGE
000A    242E            STO     CON09                   FOR RADAR ONLY
000B    34FC            CFO     ATIME                   GET ADDRESS OF TIME
000C    2449            STO     RDRO                    STORE IT
000D    30BD    BLANK2  CFA     X74                             INITALIZE
000E    2012            STA     SP9                             UPPER SW LIMIT
000F    7811            CCB     *+2                     ADVANCE TWO SPACES
0010    0008    BLANK1  SSW     S3                      REMEMBER STATUS ONLY
0011    30CE            OFA     X8000                   LOAD STATUS REPORT CODE
0012    2006            STA     SP3                     SAVE IT FOR CPU
                *** BLANK IS USE IN PWR ON TO CYCLE THRU ALL SWITCHES
                *** AND RESET THEM IT IS ALSO USED TO KEEP TRACK OF
                *** WHICH LAMP TO REPORT BACK  IN THE EVENT THAT NO
                *** SWITCH WAS PUSHED
0013    6812    BLANK   DFS     SP9
0014    7818            CC      CONSW2                  GO TO PNL PROC PROGRAM
0015    0440            RSW     S6                      GET US OUT OF INITIALIZE
0016    0008            SSW     S3                      AND INTO STATUS REPORT
0017    780D            CCB     BLANK2                  BRANCH
0018    50A6    CIBSW2  ADD     X1, A
0019    2010            STA     SP2
001A    7870            CCB     CONSW1
                *
001B    30D9    TIME    CFA     XCOO0
001C    2007            STA     RET2
0001D   6807            DFS     RET2
001E    781D            CCB     *-1
001F    7823            CCB     EOF1
                **********************************************************************
                **********************END OF FILE*********************************
                **********************************************************************
0020    71B0    EOF     EQS     XF, 0                           CHECK
0021    2C00            STH     RET                             EOF
0022    0080            SSW     S7                      INHIBIT DOU
0023    049F    EOF1    RSW     S0, S1, S2, S3, S4, S7,
                * ENTRY POINT CYCLES THROUGH ALL 3 SWITCHES
                *       WHEN  ANY OF THE ELEVEN BITS CHANGE
                *SWITCHES  13-15   POSTS  11Q-73RRSOURCE BITS FROM CPU
```

Table 5-36. AP Program Listing-Continued

```
                    * ENTRY POINT SW013   PROCESSES JUST SWTICH ACTION
                    *
                    * FIRST GO GET LAMP STATUS FROM PANEL, SHIFT AND STORE
                       IT AS STATUS
0024  342B                CFO   CON12          PICKUP NEW MASTER SOURCE
0025  41CC                AND   X75FFO, 0      SAVE Q-73 RR SOURCE BITS
0026  7028                EQS   SRCMTR         SAME AS LAST TIME?
0027  783F                CCB   SRCRET         RETURN
0028  2028                STA   SRCMT          NO - STORE NEW ONE
0029  30B3                CFA   X13            PICKUP LAMP GROUP CODE FOR 13-15
002A  7DF5                BST   RECV2          SEND COMMAND TO PANEL
002B  1100                CBA   LOS            BRING IN LAMP STATUS
002C  5C13                SHF   AR, 4          FAKES SW15 INTO POLE POSITION FIRST
002D  200B                STA   TEMP           PUT EM AWAY
002E  30A7                CFA   X2             SET FOR 3 CYCLES USING FAKE RESIDUAL
002F  2026                STA   SWFUIN         CODE - START WITH THEN 14, 13
0030  7832                CCB   SW013A         AT LEAST TRY
0031  0010  SW013         SSW   S4             RETURN TO BRO3 OR TO CALLING ROUTINE
0032  6C26  SW913A        CFI   SWFUIN         PICKUP  RESIDUAL SWITCH CODE
0033  7DEE                BST   WHODAT         NOW YOU HAVE CAT INDEX
0034  2027                STA   TMPWC          SAVE IT
0035  34E4                CFO   XFFFO          HOLE PLUGGER
0036  4128                AND   SRCMTR, O      DONT MESS WITH LO BITS OF SOURCE
0037  7E05                BST   SRCFIX         GO GET EVERTHING UPDATED
0038  0810                TSS   S4             CHECK RETURN PATH
0039  791C                CCB   BRO3           SWITCH CHANGE RETURN
003A  300B                CFA   TEMP           CPU SOURCE CHANGE RETURN
003B  5C21                SHF   AL, 2          QUE UP NEXT JUST IN CASE -BACKWARDS
003C  200B                STA   TEMP           STORE IT          -15   BEAUTIFUL
003D  6826                DFS   SWFUIN         DONE YET?
003E  7832                CCB   SW013A         NOPE -          RECYCLE
003F  342E  SRCRET        CFO   CON09          LOAD  RADAR RNG IN OPR
0040  5C4C                SHF   OL, 13         REGISTER IT
0041  240F                STO   STATUS
0042  30AE                CFA   X9
0043  7DDE                BST   OUTPUT
0044  5C4A  THRET         SHF   OL, 11
0045  41AC                AND   X7, 0          SAVE 3 LSB'S
0046  48E4                ORI   XFFFO, A       SET MANY ONES
0047  5C22                SHF   AL, 3          REGISTER WITH TRACK THREAT FIELD
0048  2921                STA   THREAT         FOR TRACK MESSAGE PROCESSOR
0049  302D                CFA   CON10
004A  5C23                SHF   AL, 4          REG
004B  2048                STA   CNTRL          STORE FOR LATER
004C  4CEA                ESB   XFFFE, A       REFRESH FLOODS??
004D  7855                CCB   CPUCON         CONTINUE WITH CPU STUFF
                    **** THIS CODE STARTS WITH 12 BITS OF LAMP STATUS IN
                    ****     TSP3 THIS WILL EXPAND THE 12 BITS TO 24, AND PUT
                    *** THEM IN LAMP REG TWO AND FIVE
004E  342D  FLOOD         CFO   CON10        LOAD FUNC STATUS TO OPR
004F  7DA4                BST   BITDBM
```

Table 5-36. AP Program Listing-Continued

```
0050  30B5                CFA     X15
0051  7DDE                BST     OUTPUT      OUTPUT GP 2  STATUS
0052  7DA3                BST     BITDBL
0053  30B2                CFA     X12
0054  7DA3                BST     OUTPUT
0055  3448                CFO     CNTRL       PU CONTRROL BITS
0056  4DE9                ESB     XFFFD, O    CPU WANT TO PUSH A SWITCH ???
0057  7361                CCB     SWPIK       NO-PROCESS OPERATOR SWITCH PUSH
0058  3436                CFO     CON01       YES GEP SWITCH CODE
0059  5C47                SHF     OL, 8       PUT IT IN LSBS
005A  41BE                AND     X7F, O      ISOLATE IT
005B  2010                STA     SP2         SAVE FOR LATER
005C  5C42                SHF     OL, 3       GET NEW STATE IN LSBS
0050  240B                STO     TEIMP       SAVE FOR LATER OVERRITE
005E  34A5                CFO     XO                PICK UP ZERO TO SAY
005F  2406                STO     SP3               NO REPT TO CPU THIS TIME
0060  7870                CCB     CONISW1     GO DO IT
                    *** DIFFERENTIATE LEAD EDGE OF SWITCH PUSH
0061  3016          SWPIK CFA     X8E02       LOAD CONS SWCMD TO ACC
0062  7DF7                BST     TALK        TRANSMIT 'TO FP
0063  3414                CFO     PHS         LOAD OLD CODE
0064  1100                CBA     LOS         REAL) NEW SWITCH CODE
0065  2014                STA     PHS         SAVE NEW SWITCH CODE
0066  70A5                EQS     XO, A       NEW CODE ZERO?
0067  7A3E                CCB     LOFF        BRANCH IF SO
0068  64A5                MICS    XO          OLD CODE ZERO?
0069  7810                CCB     BLANK1      BRANCH IF N(OT
006A  4CI)E               ESB     XFF7F, A    IS IT KEYBOARD?
006B  791F                CCB     KBD1        YEP - GO THERE
006C  40BE                AND     X7F, A      NOPE - CLEAN IT UP
006D  2010                STA     SP2         SAVE IT
006E  301)9               CFA     XC000       LOAD CONS SWITCH ACT CODE
006F   2006               STA     SP3         SAVE STATUS WORD
                    *     THIS CODE SELECTS UPPER OR LOWER HALF OF
                    *     MANADD TABLE FOR USE 13Y SUBLUP
0070  3410          CONSW1 CFO    SP2         PICK UP SWITCH CODE
0071  30F4                CFA     116         ASSUME NOT > 64
0072  64EC                ISC     X40         IS IT?
0073  30F6                CFA     132         YES - FIX IT
0074  2007                STA     TSP5        PUT IN FOR SUBLUP
0075  51BB                ADD     X3F, O      ASSUME NOT > 64
0076  64EC                IMCS    X40         IS IT?
0077  54LB                SUB     X3F, A      YES - F[X IT
0078  2011                STA     SP4         SAVE IT
              *  THIS ROUTINE STARTS WITH SWITCH CODE AND JUMPS TO
              *   PROPER SUBROUTINE TO HANDLE IT.
              * ASSUMES SWITCH CODE STORED IN SPR
              * ASSUMES :33 SWITCH GROUPS
              *         -ASSUMES LOCATION MANADD IN FILE IS TABLE OF MIAGIC
              *         NUMBERS AND BRANCH ADDRESSES <PACKED TOGETHER>
              *
              *  SUBROUTINE LOOKER UPPER
```

Table 5-36. AP Program Listing-Continued

```
0079  6C07  SUBLUP  CFI   TSP5          SAVE IT
007A  32FF           CFA   ELBL, I
007B  5C23           SHF   AL, 4
007C  48B0           AND   XF, A
007D  5011           ADD   SP4, A        ADD TO SWITCH CODE
007E  2011           STA   SP4           SAVE SW CODE + MANADD
007F  4CBE           ESB   X7F, A        GREATER THAN 127?
0080  7896           CCB   SUB1          NO - TRY NEXT ONE
                     *
                     * THE FOLLOWING STEP PRE-INITALIZES LOCATION
                     *SWFUIN--SWITCH FUNCTION INDEX--JUST IN CASE WE NEED IT
                     *
0081  2026  STA      SWFUIN              STORE FOR LATER
                     * SUBLUP HAS FOUND THE SWITCH SUBROUTINE
                     * TSP5 CONTAINS THE SWITCH INDEX, IREG CONTAINS INDEX
                     *LAMPS IS AREA WHERE LAMP CONSTANTS ARE STORD
0082  3007  LIGHTS   SUB   TSP5
0083  54F2           CBI   TABL2         INDEX TO UPPER CONSTANTS
0084  OCO            CFO   ACC
0085  36FF                 ELBL, I       GET LAMP CONSTANT
                     * NOW BREAK LAMP CONSTANT APART FOR USE
0086  41BE  AND      X75, 0              PICK OFF BOTTO( SWITCH CODE
0087  2008  STA      TSP2
0088  5C44  SCH      OL, 5               POSITION LAMP GROUP
0089  41B8  AND      X1F, O              PICK OFF LAMP GROUP
008A  2009  STA      TSP3
008B  5C42  SHF      OL, 3               POSITION ALGORITHM CODE
008C  41AC  AND      X7, 0               PICK OFF ALGORITHM CODE
008D  5OF9  ADD      ALGOFF              ADD ALGORITHM OFFSET
008E  200A  STA      STP4
                     * DOES SWITCH BELONG TO REPORT ONLY CATEGORY?
008F  0407  RSW      SO, S1, S2
0090  4DCD  ESB      X7FFF, O            IS IT REPORT ONLY?
0091  7899  CCB      BIT16               NO
0092  30A5  CFA      XO                  YES - REPORT ONLY
0093  0808  TSS      S3                    DON'T GIVE A STATUS REPOLRT
0094  2006  STA      SP31                  FOR A REPORT ONLY SWITCH
0095  78D2  CCB      BR01                BRANCH
0096  6807  SUB1     DFS                 TSP5   DECREMENW  INDEX
0097  7879  CCB      SUBLUP              TRY AGAIN
0098  79BB  CCB      FAULTY

                     *** IS THIS GROUP 111-116 OR 40-51?
                     *** IF SO SET SO OR S2 RESPECTIVELY TO REMEMBER
                     *** TSP5 CONTAINS THE SWITCH INDEX
0099  3407  HIT16    CFO   TSP5          LOAD SWITCH INDEX
009A  71F5           EQS   I31, 0              IS I - 31
009B  0001           SSW   SO                  REMEMBER  111-116
009C  71F3           EQS   I14, 0              IS I = 14?
009D  0004           SSW   S2                  REMEMBER GP 40-51
```

Table 5-36. AP Program Listing-Continued

```
                    * THIS CODE STRING TAKES LOWEST SWITCH CODE NO STORED
                    * IN LMAP REGISTER AND SUBTRACTS IT FROM ACTUAL
                    * THE NO OF SHIFTS REQUIRED TO POSITION LMP CD STATFX
009E    3010    DIFGEN      CFA     SP2             PICK UP PRESENT SW CODE
009F    5408                SUB     TSP2            DIFF IN TWO CODES
00A0    100C                STA     TSP10           SAVE DIFF
00A1    1400                CBO     ACC
00A2    64AA                MCS     X5              IF DIFF LT 6 SKP NEXT CMD
00A3    79B6                CCB     CONSW7          SUB 6 &ADD 1 TO LAMP GROUP
00A4    6809                DFS     TSP3            DIFF<6 SUB 1 FROM LAMP CD
00A5    5C40    CONSW8      SHF     OL, 1           DOUBLE DIFF TO GET SH INDEX
00A6    2413                STO     SPIN            SAVE SHIFT INDEX
00A7    7DF4                BST     RECV1           SEND REQ TO FRONT PANEL
00A8    1100                CBA     LOS             READ STATUS FROM FT PANEL
00A9    7DE8                BST     RSHIFT          F05 LAMP CODE FOR ALG
                    *** IF THIS IS JUST STATUS SAVE IT AND GO TO FSTK
00AA    0808                TSS     S3              SKIP IF NOT STATUS
00AB    78DF                CCB     SAVE            GO SAVE IT
00AC    0804                TSS     S2              SKIP IF NOT 40-51
00AD    7905                CCB     LENT            GP  IS 40 51
00AE    3448                CFO     CNTRL           PICKUP UNARY CONTROL WORD
00AF    4DE9                ESB     XFFFD, 0        CPU OVERRIDE???????
00BO    2006                STA     TEMP            SAVE OLD STATUS
00B1    40E8                AND     XFFFC, A        2AP 2 LSB 5
00B2    200F                STA     STATUS          SAVE REST OF STATUS WORD
00B3    300B                CFA     TEMP            PICK UP OLD STATUS
00B4    0640                TSS     S6              SKIP IF NOT INITIALIZE
00B5    48A8                ORI     X3, A           SET INITIALIZE STATUS
                    *       THIS ROUTINE STARTS WITH OLD STATUS OF LAMPS IN
                    *       LOCATION "STATUS" AND ALGORITHM PATTERN NUMBER IN
                    *       INDEX  -  RETURNS WITH NEW STATUS OF LAMPS IN
                    *       LOCATION "STATUS"   CALLES WITH A "BST"
                    *
                    *** STATUS FIXER UPPER ***
00B6    40A8    STATFX      AND     X3, A
00B7    200B                STA     TEMP            SAVE 'EM
00B8    30A9                CFA     X4              INITLALIZE FAULT WATCHDOG
00B9    2027                STA     TMPWC           TO TRAP BAD INPUT STATUS CODES
00BA    6COA                CFI     TSP4            OAD ALF IN INDEX REG
00BB    36FF                CFO     ELBL, I         GET PATTERN
00BC    41A8    STAT1       AND     X3, 0           KEEP 2 BSB'S
00BD    700B                EQS     TEMP, A         IS STATUS SAME?
00BE    78C2                CCB     STAT2           BRANCH IF SO
00BF    5C41    STAT2       SHF     OL, 2           SHIFT PATTERN
00CO    6821                DFS     TIMPWC          STILL WORKING ON LEGAL ONES??
00C1    78BC                CCB     STAT1           TRY AGAIN
00C2    3048                CFA     CNTRL           IF IT IS CPU USE THE CUED CODE
00C3    4CE9                ESB     SFFFD           OTHERWISE WE SHIFT TWICE AND USE IT
00C4    5C41                SHF     OL, 2           SHIFT PATTERN
00C5    41A8                AND     X3, 0           KEEP 2 LSB'S
00C6    200B                STA     TEMP            SAVE 'EM
00C7    480F                ORI     STATUS, A       MAKE NEW STATUS
00C8    200F                STA     STATUS
```

Table 5-36. AP Program Listing-Continued

```
                * THIS CODE STRING WILL TAKE NEW LAMP CONDITION AS
                * STORED IN STATUS PUT IT BACK AND ZIP IT BACK TO
                * THE FRONT PANEL ALG**16-SPIN=NO OF SHIFTS
00C9    30B1    SPINBK    CFA     X10
00CA    5413              SUB     SPIN          NEW SHIFT CODE
00CB    2013              STA     SPIN
00CC    300F              CFA     STATUS        STATUS WORD FROM STATFX
00CD    7DE8              BST     RSHIFT        GO SHIFT STATUS WORD
00CE    200F              STA     STATUS        SAVE NEW LAMP DATA
00CF    3009              CFA     TSP3          LOAD LAMIP GROUP IN ACC
00D0    7DDE              BST     OUTPUT
00D1    300B              CFA     TEMP          LOAD NEW STATUS OF LAMP
00D2    7CDA    BR01      BST     SVST          SAVE IT FOR CPU
00D3    6707              CFI     TSP5          LOAD SWITCH BRANCH POINT
00D4    3026              CFA     SWFUIN        TOO LARGE BY X80-XF
00D5    54ED              SUB     X80, A              FIXIT FOR TRUE SWITCH RESIDUAL
00D6    1400              CBO     ACC           HOLD IT IN OPND
00D7    2026              STA     SWFUIN        STORE IT TOO
00D8    50BO              ADD     XF, A         FIXIT FOR TOWAY2
00D9    62FF              CFB     ELBL, 1       BRANCH TO THE ROUTINE
                *** THIS SUBROUTINE SAVES LAMP STATUS STORE IN THE
                *** ACCUMULATOR FOR OUTPUT TO THE CPU
00DA    40A8    SAVST     AND     X3, A         SAVE LSBS OF SWITCH STATUS
00DB    5CA6              SHF     AL, AS, 7     POS LAMP STATUS
00DC    4810              ORI     SP2, A        ADD TO SW CODE
00DD    2005              STA     SP1           SAVE IT FOR OUTPUT TO CPU
00DE    6000              CFB     RET           RETURN
00DF    7CDA    SAVE              BST           SAVST SAVE IT FOR CPU
00EO    791C              CCB     BR03          LAMP EXIT
                * SWITCHES 1-12 PART OF TRACK DATA DISPLAY
                *   BUILD  ESB UNARY MASKS FOR LOCAL, OTHER, ATMS-TOS
                *
                * FIRST LETS GET INDEX TO BASIC CAT
                *         SWFUIN HAS RESIDUAL SWITCH CODE
                *         TEMP   "              2BIT NEW LAMP STATE
00E1    0C80    SW001     CB1     OPR           LOAD INDEX REG
00E2    7DEE              BST     WHODAT        GET UNARY SOURCE FLAG READY
00E3    34A6              CFO     X1            ASSUME FRIEND
00E4    4CE4    SW001A    ESB     XFFFO, A      THERE YET??
00E5    78FA              CCB     SW0001B       NO -TRY AGAIN
00E6    2427              STO     TMPWC         STORE CAT INDEX
00E7    1400              CBO     ACC           PUT IT HERE TOO FOR PLUGGER
00E8    7E05              BST     SRCFIX        GO TO SOURCE FIXER-UPPER
00E9    791C              CCB     BRO3          RETURN TO REPORT THING
                *SW001B   IS STRANGE  UNARY AND SWITCH NUMBER FIXER
00EA    5CCO     SW001B   SHF     OL, AS, A     SHIFT ONCE LEFT
00EB    5C93              SHF     AR, AS, R
00EC    78E4              CCB     SW001A        GO TEST AGAIN
                *
                *
                * SWITCH 19 -MODE -SPEC TEST &NOW-TEST ENTER SW019
```

Table 5-36. AP Program Listing-Continued

```
00ED  34A6  SW020   CFO  X1                SAY IT WAS 20 FOR RGSTR4
00EE  0410  SW019   RSW  S4                SAYS 19-20  TO RGSTR4
00EF  2029          STA  TMPWC1            STORE FUNNY INDEX NO FOR TOWAY1
00FO  7E20          BST  RGSTR4            GO FIX UP LAMP PATTERN
00F1  3029          CFA  TMPWC1            PICK UP FUNNY INDEX , NO FOR TOWAY1
00F2  7A1D          CCB  SW019B            GO TO TOWAY1 CHAIN
                    * SWITCH 21 - HOSTILE /UNKNOWN TTG SELECTOR MASK SETTER, ETC
00F3  7E16  SW021   BST  FNY5Z             FUNNY FIVES KNOWS HOW-SEE HIM
00F4  2020          STA  TRTTG             BACK ALREADY - THANKS
00F5  791C          CCB  BRO3              QUICK HUH --
00F6  1780  SW024   CBO  SB                PICKUP STATUS BITS RADAR ONLY?'?
00F7  4DDA          ESB  XDFFF, O          RADAR ONLY??
00F8  791C          CCB  BRO3              NO-RETURN
00F9  7A22          CCB  TOWAY1            YES-FIX RO OFFSET CENTER INTERNALLY
                    *SWITCH 26 - MAP1/MAP2 SELECTOR USES FNY5Z TOO
00FA  7E16  SW026   BST  FNY5Z             IBID
00FB  5C23          SHF  AL, 4             FIXIT-UP FOR REGISTRATION W/MAP BITS
00FC  201C          STA  MAPMSK            PUT IT WHERE MAP ROUTINE CAN FIND IT
00FD  791C          CCB  BRO3              ALL GONE
                    *SWITCHES 27-29 SELECT VELOCITY VECT FOR    F, U, H RESPECTIVELY
                    *    THIS ROUTINE MAKES ESB MASK AND PUTS IT INTO TRVEC
00FE  6C26  SW027   CFI  SWFUIN            INDEX TO CATEGORY USED
00FF  7DEE          BST  WHODAT            TOGENERATE  UNARY ONE IN RIGHT
PLACE
0100  2027          STA  TMPWC             SAVE FOR LATER
0101  1020          CBA  ACC, N            FLIP IT
0102  401F          AND  TRVEC, A          ASSUME SUBJECT VELOCITY DISPLAYABLE
0103  340B          CFO  TEMP              NOW GET THE FACTS ?
0104  4DEA          ESB  XFFFE, O          WERE WE RIGHT ?
0105  4827          ORI  TMPWC             NO-YOU WERE WRONG - PLUG HOLE
0106  48E6          ORI  XFFF8, A          PLUG OTHER HOLES
0107  201F          STA  TRVEC             PUT IT BACK WHERE TRACK CAN FIND
0108  791C          CCB  BRO3              GO AWAY , BYE
                    *SWITCHES 22 AND 23 -- RANGE SELECTION
                    *
                    * TRUTH TABLE FOR DETERMINING SCALE INDEX
                    *          22-01 SHIFT  2          23=01 SHIFT 3
                               22=10 SHIFT 0          23=10 SHIFT 1
0109  1080  SW022   CBA  OPR               PUT SWFUIN INTO ACC
010A  340B          CFO  TEMP              PICKUP SWITCH STATUS
010B  4DE9          ESB  XFFFD, O          BIG SHIFT '??
010C  50A7          ADD  X2, A             YES - DO TWO MORE
010D  2025          STA  RANGE             NO-STORE SHIFT INDEX
010E  2013          STA  SPIN              LOAD FOR SHIFT
010F  34EB          CFO  XFFFF             ASSUME RANGE NOT XERO
0110  70A5          EQS  XO, A             WAS IT
0111  34DE          CFO  XFF7F             YES-FIX IT
0112  2419          STO  GEOMSX            STORE IT
0113  30C4          CFA  X1F882            WINDOW CONSTANT
0114  7DE8          BST  RSHIFT            SHIFT WITH RANGE
0115  2024          STA  WINDOW            PUT AWAY
                    *
                    * NOW DO SOMETHING ABOUT THE LIGHT DRIVER CODE DEVELOPED
                    * IN SUBLUP ET AL --MAAKE 22&23 MUTUALLY EXCLUSIVE
```

Table 5-36. AP Program Listing-Continued

```
0116  0010          SSW   S4          SET SWITCH FOR RGSTR4
0117  3426          CFO   SWFUIN      PICK UP SWITCH INDEX AGAIN
0118  7E2D          BST   RGSTR4      GET SOMBODY TO FIX UP PATTERN
0119  791C          CCB   BRO3        COMMON SWITCH EXIT
011A  64A5  SW081   MCS   XO          IS IT SWITCH 81?
011B  7A21          CCB   SW082       NOPE - PLEASE GO TO RIGHT PLACE
011C  0840  BRO3    TSS   S6
011D  7813          CCB   BLANK       GET NEXT SW TO INITIALIZE
011E  7922          CCB   FSTK              FINISH SEND DATA TO CPU
                    **** LOAD KEYBOARD ACTION CODE
011F  2005  KBD1    STA   SP1         SAVE KBD CODE
0120  30C8          CFA   X4000       LOAD KBD ACT CODE
0121  2006  BK02    STA   SP3         STORE KBD ACT CODE
                    * FORCE STICK SUBROUTINE
0122  30D4  FSTK    CFA   X8602       LOAD FSTK CMD IN ACC
0123  7DF7          BST   TALK
0124  3425          CFO   RANGE       PICK UP RANGE COMP
0125  45A8          ORX   X3, 0       INVERT RANGE BITS
0126  2013          STA   SPIN
0127  1500          CBO   LOS
0128  0403          RSW   SO, S1      RESET SO AND S1
0129  4DD1          ESB   X8181, 0    IS X OR 7 GT 1
012A  34A5          CFO   XO          ZERO OPERAND
012B  41CB  CONV    AND   X7FO0, 0    PUT MAG Y IN ACC
012C  4DCD          ESB   X7FFF, O    IS IT NEGATIVE?
012D  7930          CCB   *+3         NOPE - ADVANCE 3 SPACES
012E  1020          CBA   ACC, N      YEP-FLIP IT
012F  50A6          ADD               X1, A    ADD 1 FOR 2/S COMP
0130  5CD7          SHF               AR, OL, AS, 8   SHIFT EVERYBODY
0131  6C13          CFI               SPIN            LOAD SHIFT INDEX
0132  79EF          BST               SHIFT
0133  6802          TSS               S1
0134  7938          CCB   VARS        FORCE STICK COMPLETE
0135  0202          SSW   S1, S9
0136  2003          STA   LOCY        SAVE YFORCE STICK
0137  792B          CCB   CONV
0138  2004  VARS    STA   LOCX        SAVE X FORCE STICK
0139  6047          CFB   RONRO       RADAR ONLY OFFSET CONNECTOR
013A  5034  R00FF   ADD   XOFF, A
013B  1400          CBO   ACC
013C  3003          CFA   LOCY
013D  5033          ADD   YOFF, A
013E  7941          CCB   PUTOFF      GO PUT AWAY
013F  34A5  ROCENT  CFO   XO          GET ZED
0140  1080          CBA   OPR         OFFSETS
0141  2434  PUTOFF  STO   XOFF        STORE RADAR ONLY OFFSET X
0142  2033          STA   YOFF        Y TOO
0143  303B          CFA   TEST        PICK UP TEST/NORM SWITCH
0144  5046          ADD   CMPSEL, A   ADD COMPRESSOR ON/OFF SWITCH
0145  70FD          EQS   TOTST       IS IT TEST MODE WITH COMPRESSOR ON?
0146  3CAD          CHF   X8          SEND M. T. 8 TO DC IF SO
                    * VARIABLE RANGE SCALE ROUTINE
```

Table 5-36. AP Program Listing-Continued

```
0147  3448  NRMOF  CFO   CNTRL
0148  4DE7         ESB   XFFFB, O
0149  794B         CCB   *+2              DO IT FROM FRONT PANEL-SKIP 1 STEP
014A  79FF         CCB   VARS1
014B  30D3         CFA   X8402            LOAD VAR RNG CMD IN ACC
014C  7DF7         BST   TALK
014D  1120         CBA   LOS, N
014E  1400         CBO   ACC              LOAD INVERSE GREY CODE
014F  6CAC         CFI   X7               BEGIN GREY TO BINARY CONVERSION
0150  4DDE         CFA   XO
0151  5C60         ESB   XFF7F, O                 IS INVERSE GREY A ZERO?
0152  7400  AGAIN  ORX   XFFOO, A          YES COMPLIMENT LAST BINARY BIT
0153  7951         SHF   AL, OL, 1                ET NEXT BIT, STORE LAST BIT
0154  40BF         DIS
0155  2022         CCB   AGAIN
0156  40BF         AND   XFF, A             GET RID OF JUNK
0157  2022         STA   POT
                   ************************************************************************
                   ********** TTG SWITCH PROCESSING ****************************
                   ************************************************************************
0158  30D5         CFA   X8802            LOAD TTG CMD IN ACC
0159  7DF7         BST   TALK
015A  1120         CBA   LOS, N           LOAT TTG DATA IN ACC INV
015B  1400  VARS2  CBO   ACC              PUT IT IN OPERAND TOO
015C  5CA7         SHF   AL, AS 8         POSITION TTG
015D  4822         ORI   POT, A           COMBINE WITH VAR RANGE
015E  7BFA         CCB   DOULPT           PATCH FOR DOU LOOP TEST
015F  5CC1         SHF   OL, AS, 2        . SCALE
0160  4CC1         ESB   X7FF, A          .       TTG
0161  5CC2         SHF   OL, AS, 3        . SETTING
0162  58B9         MPY   XD9              MULTIPLY BY SCALE CONSTANT
0163  2023         STA   TTG              SAVE FOR MSG PROCESSING

                   *
                   *  ROUTINE CONMKR-- MAKES CONSOLE UNARY MASKS--CONMSK
0164  1380         CBA   SB               PICKUP THING (SB)
0165  4CDA         ESB   XDFFF, A         RADAR ONLY??
0166  7998         CCB   NRDRO            NO-SETUP NORM
0167  40AC  LDCON  AND   X7               SAVE ONLY LOW 3 BITS
0168  OCOO         CBI   ACC              LOAD INDEX
0169  7DEE         BST   WHODAT           MAKE INVERTED MASK
016A  5CA6         SHF   AL, AS, 7        TO SHIFT MASK UP
016B  1020         CBA   ACC, N FLIP
016C  2017         STA   CONMSK           PLOP IT INTO CONMSK-CONTINUE
                   * LOAD STATUS WORD AND SWITCH ACTION CODE
016D  3401         CFO   ERROR            COPY ERROR ADDRESS
016E  1380         CBA   SB               LOAD STATUS BITS IN ACC
016F  64A5         MCS   XO               ERROR?
0170  48B7         ORI   X20, A           YES - SAY SO
0171  4806         ORI   SP3, A           LOAD SW ACT CODE IN ACC
0172  5C12         SHF   AR, 3            POS STATUS FOR FEED BACK
0173  2006         STA   SP3              SAVE STATUS FOR OUTPUT
```

Table 5-36. AP Program Listing-Continued

```
                * START OUTPUT TO COMPUTER BUFFER
0174    6CAA            CFI     X5
0175    30A5            CFA     XO              BRANCH
0176    704F            EQS     FLAG            IF NOT
0177    797D            CCB     CBOUT           DOU TEST
0178    2047            STA     FLAG                    PUT
0179    3050            CFA     TEST1                   TEST
017A    2002            STA     SP8                     DATA
017B    3051            CFA     TEST2                   IN
017C    2001            STA     ERROR                   FEEDBACK
017D    30A6            CFA     X1              LOAD CB INPUT CMD
017E    7DF7            BST     TALK
017F    3AOA            CFL     ERROR, I        READ WD OF DATA TO CB
0180    7DC2            BST     FAULT           NO IND RCD FROM CB
0181    7400            DIS                     DEC INDEX REGISTER
0182    797D            CCB     CBOUT
                *  SEND CONSOLE CONTROL TO D. C.
0183    0200            SSW     S9              SET SWITCH 9 FOR MSG OUTPUT
0184    3CAB            CFH     X6              SEND MESSAGE WOED
0185    S034            CFA     XOFF            COPY X-OFFSET
0186    1020            CBA     ACC, N          INVERT IT
0187    7FE9            BST     SCA             SCALE IT
0188    1COO            CBH     ACC             SEND IT
0189    3033            CFA     YOFF            COPY Y-OFFSET
018A    1020            CBA     ACC, N          INVERT IT
018B    7FE9            BST     SCA             SCALE IT
018C    1C00            CBH     ACC             SENT IT
018D    30A5            CFA     XO              COPY ZERO
018E    2001            STA     ERROR           RESET ERROR
018F    34C3            CFO     X110            GET COMPRESSOR-OFF RATE
0190    7046            EQS     CMPSEL, A       IS COMPRESSOR ON?
0191    34CA            CFO     X5550           YES - GET COMPRESSOR-ON RATE
0192    3025            CFA     RANGE           COPY RANGE
0193    70A6            EQS     X1, A           IS IT RUBBER RANGE??
0194    799D            CCB     RUBRNG          DO SOMETHING SPECIAL
0195    4925    RNGPUT  ORI     RANGE, O        PLUG IN RANGE
0196    1C00            CBH     ACC             SEND RATE/RANGE WORD
0197    6049            CFB     RDRO            RADAR ONLY CONNECTOR
                *RDRO MAIN FOR NORMAL, =TIME FOR RADAR ONLY
0198    34F0            NRDRO   CFO     NORMOF1         NORMAL OFFSET CONNECTOR
0199    2247            STO     RONRO           STORE IT
019A    3491            CFO     MTAB1+1         GET ADDRESS OF MAIN
019B    2449            STO     RDRO            AND STORE IT
019C    7967            CCB     LDCON           CONTINUE
                        *UPDATE RUBBER RANGE WINDOW EACH CYCLE IF NECESSARY
019D    392C    RUBRNG  CFA     CON11           RUBBER RANGE WINDOW FROM CPU
019E    2924            STA     WINDOW          STORE IT
019F    5822            MPY     POT             SCALE RATE FOR RUBBER RANGE
01AO    40E6            AND     XFFF8, A        SAVE UPPER PART
01A1    1400            CBO     ACC             RESTORE TO OPERAND
01A2    7995            CCB     RNGPUT          GO FINSH UP
                        **************************************************************
                        ******************BRANCHES AND SUBROUTINES*****************************
```

Table 5-36. AP Program Listing-Continued

```
                  *****    BITDBL TAKES  A 12 BIT REG CONTAINING LAMP
                  *****    STATUS AND PUTS IT IN LAMP GROUPS 2, 5 AND
                  *****    14 FOR FLOODLIGHTS, EPENDING ON INDEX REG
                  ****     THE 12 BIT LAMP STATUS MUST BE IN OPERAND
01A3    3409      BITDBDL  CFO   TSP3              PICK UP LAMP DATA
01A4    6CAA      BITDEN   CFI   X5                LOAD INDEX FOR SHIFT
01A5    30A5               CFA   XO                CLEAR ACC
01A6    4DDB      BITDBN   ESB   XF7FF, O          EXAMINE BIT 12
01A7    79A9               CCB   BITDBO
01A8    48A8               ORI   X3, A             MSB IS A "1"
01A9    5CEO      BITDBO   SHF   OL, AL, AS, 1
01AA    5CAO               SHF   AL, AS, 1
01AB    7400               DIS
01AC    79A6               CCB  BITDBN             NOT DONE YET
01AD    5C91               SHF AR, AS, 2
01AE    200F               STA STATUS              SAVE FOR SUBROUTINE OUTPT
011AF   2409               STO TSP3                SAVE OPR FOR NEXT TIME
01BO    6000               CFB  RET
01B1    30BC      CONSW6   CFA X67                 PUT SW 111 IN ACC
01B2    2008               STA   TSP2              PUT FAKE BOTTOM IN IN TSP2
01B3    30B6               CFA X19                 LAMP CODE
01B4    2009               STA   TSP3              SAVE CORRECT LAMEPCOODE
01B5    789E               CCB   DIFGEN
                  * THIS ROUTINE TAKES CARE OF PROBLEM WHEN DIFFERENCE
                  * BETWEEN LOWER LIMIT AND SWITCH NO IS GT 6. FOR ALL
01B6    0801      CONSW7   TSS   SO                SKIP IF SSO NOT SET
01B7    79B1               CCB   CONSW6            THISMEANS MAKE REG =8
01B8    55AB               SUB   X6, 0
01B9    1400               CBO   ACC
01BA    78A5                     CCB               CONSW8
                  **********      FAULT ROUTINE    ******************************
01BB    30A5      FAULTY   CFA   XO                GET NO REPORT CODE
01BC    6808               TSS   S3                . BRANCH IF
01BD    7921               CCB   BRO2              . STATUS REPORT
01BE    6840               TSS   S6                IS IT INITALIZE
01BF    7813               CCB   BLANK             BRANCH IF SO
01CO    7DC2               BST   FAULT             TAKE NOTES
01C1    7922               CCB   FSTK              KEEP GOING
01C2    3000      FAULT    CFA   RET               PRINT FAULT ENTRY LOCATION
01C3    2001               STA   ERROR             SAVE FOR LATER
01C4    6000               CFB   RET               RETURN
                  *** TAKE TASK SELECT CODE AND PUT IN REG 11 TO LIGHT
                  *** LENTICULARS
01C5    30A7      LENT     CFA   X2                LOAD LAMP GP IN ACC
01C6    0840               TSS   S6                ARE WE IN INITIALIZATION?
01C7    79CB               CCB   *+4               BRANCH IF SO
01C8    3410               CFO   SP2               PICK UP SWITCH CODE
01C9    71A4               EQS   X30;0             IS IT 48?
01CA    7810               CCB   BLANK1            BRANCH IF SO
01CB    7DF5               BST   RECV2             BRANCH IF NOT
01CC    1500               CBO   LOS               READ LAMP STATUS
01CD    41EO               AND   XFFCO, O          MASK OUT LOWER 6 BITS
```

Table 5-36. AP Program Listing-Continued

```
01CE  480C                ORI     TSP1O, A          COMBINE TO GET NEW REG ST
01CF  50AD                ADD     X8, A
01D0  200F                STA     STATUS            SAVE IN LAMP OUT LOCATION
OlD1  30A7                CFA     X2                LOAD LAMP GP IN ACC
01D2   7DDE                       BST     OUTPUT
01D3  6COC                CFI     TSP10             LOAD INDEX
01D4  7DEE                BST     WHODAT            SHIFTS A ONE UP
01D5  1400                CBO     ACC               PUT INTO OPERAND
01D6  7DA4                BST     BITDBM            FINISHED  USE TASK FUNCT
01D7  30A6                CFA     X1
01D8  7DDE                BST     OUTPUT            9 AND 10
01D9  7DA3                BST     BITDBL            GET LAST 6 BITS FOR LOAD
01DA  30A5                        CFA     XO
01DB  7DDE                BST     OUTPUT            LOAD LAMP STATUS ON
01DC  30A8                CFA     X3                SAVE IT FOR CPU
01DD  78DF                CCB     SAVE
                  * OUTPUT LAMP DATA IN TSP3          LAMP GP IN ACC, CALL IT
01DE  240D  OUTPUT        STO     TSP11             SAVE LAMPGP
01DF  3400                CFO     RET
01EO  240E                STO     TSP12             SAVE RETURN ADD
                  *** SUBROUTINE TO  SEND COMMAND TO FRONT PANEL
                  *** FOR SENDING
01E1  5CA8                SHF     AL, AS, 9         POS STATUS
01E2  48C9                ORI     X4002, A          OR COMMAND DATA WITH GROUP
01E3  7DF7                BST     TALK
01E4  380F                CFL     STATUS            OUTPUT DATA
01E5  7DC2                BST FAULT
01E6  340D                CFO     TSP11             RESTORE OPR
01E7  600E                CFB     TSP12             RETURN
                  * RIGHT SHIFT ACCUMULATOR NO PLACES SPEC IN SPIN
                            * RESULT IS LEFT IN ACC
01E8  6C13                RSHIFT  CFI     SPIN
01E9  7400                RSHIFT  DIS
01EA  79EC                CCB     DOIT
01EB  6000                CFB     RET               RETURN
01EC   5C10  DOIT         SHF     AR, 1
01ED   79E9               CCB     RSHIF1
                  *
                  * SUBROUTINES WHODAT - LEFT SHIFT X'1' LOGICAL BY INDEX
01EE  30A6  WHODAT        CFA     X1        PUT ONE INTO ACCUM
              *                             SHIFT SUBROUTINE
01EF  7400   SHIFT        DIS               DEC INDEX SKIP IF 0
01F0   79F2               CCB     RS        BRANCH TO SHIFT
01F1  6000                CFB     RET       RETURN TO MAIN
01F2  5CAO  RS            SHF     AL, AS, 1 LS ACC 1PLACE
01F3  79EF                CCB     SHIFT     BRANCH TO DEC CMD
                  *** SUBROUTINE TO SEND CMD TO FRONT PANEL FOR
                  *** RECEIVING DATA
01F4  3009  RECV1         CFA     TSP3      PICK UP LAMP GP
01F5  5CA8  RECV2         SHF     AL, AS, 9 POS STATUS
01F6  48DO                ORI     X8102, A  OR COMMAND DATA WITH GP
                  * TALK SUBROUTINE
```

Table 5-36. AP Program Listing-Continued

```
01F7  1400        TALK    CBO     ACC                 MOVE COMMAND 'TO OPERAND
01F8  30A5                CFA     X0                  INITIALIZE COUNT
01F9  50A6        TRYCMD  ADD     X1, A               INCREMENT COUNT
01FA  70EC                EQS     X40, A
01FB  79C2                CCB     FAULT                       DEVICE DEAD FOR 115 MICRO
01FC  18AO                CBL     OPR, C                      SEND COMMAND TO DEVICE
01FD  79F9                CCB     TRYCMD                      DEVICE DID NOT ANSWER
01FE  6000                CFB     RET                         DEVICE DID ANSWER
                  * CONS SWITCHES OVERRIDEN BY CPU
01FF  34BF        VARS1   CFO     XFF
0200  412E                AND     CON09, 0            SAVE RANGE OVERRIDE
0201  2022                STA     POT
0202  34BE                CFO     X7F
0203  4135                AND     CON02, 0            SAVE TTG OVERRIDE
0204  795B                CCB     VARS2
                  *
                  * SUBROUTINE SRCFIX -- THIS GUY IS ONLY ONE USED
                                       TO BUILD TRDTAB AND TCDTAB
                                       ESB UNARY SOURCE WORDS FOR TRACKS

                  * ENTRY BY BST, RETURN WITH CFB
                  * ON ENTRY        OPERAND         HAS     HOLE PLUGGER
                  *                 ACCUM           HAS     ESB PARTIAL PATTERN INVERTED
                  *                 INDEX           HAS GARBAGE -WHAT ELSE
                  *                 TMPWC           "  CATEGORY INDEX
                  *                 TMPWC1                  GETS HOLD PLUGGER
                  *                 TMPWC2          "  ESB PARTIAL READYTO GO
                  *                 TEMP            HAS SWITCH STATUS CODE
0205  2429        SRCFIX  STO     TMPWC1                  STORE PLUGGER
0206  1020                CBA     ACC, N                  MAKE ESB THING INTO ACUMULATOR
0207  202A                STA     TMPWC2                  SAVE FOR LATER
0208  6C27                CFI     TMPWC                   GET CAT  INDEX
0209  4B14                ORI     TMRDTAB, I, 0           PLUG HOLES
020A  340B                CFO     TEMP                    GET SWITCH SETTING
020B  4DE9                ESB     XFFFD, O                WANT TO UNPLUG??
020C  7AOE                CCB     SRCF1                   NO -JUST PUTAWAY
020D  402A                AND     TMPWC2                  YES-CUT SOME HOLES
020E  2214        SRCF1   STA     TRDTAB, I               PUTAWAY SYMBOL THING
020F  3029                CFA     TMPWC1                  HOLE PLUGGER AGAIN
0210  4A19                ORI     TCDTAB, I, A            USE IT WITH CARE
0211  4DEA                ESB     XFFFE, O                WANT TO UNPLUG
0212  7A14                CCB     SRCF2                   NO- 173RR NOT SEL THIS CAT
0213  402A                AND     TMPWC2                  OH YEAH
0214  2219                STA     TCDTAB, 9               PUTAWAY  AN CHAR THING
0215  6000        SRCF2   CFB     RET                     RETURN

                  *
                  * SUBROUTINE  FUNNY FIVES  UTILIZES FACT THAT
                                MPYX5 OF 2 BIT CODE MAPS 2T01 & 1+02
                                WITHOUT SCREWING UP OTHER GARBARGE

                  * EFFECTIVE PROGRAMMED MULTIPLY BY 5 OF 2 BIT SWITCH
```

Table 5-36. AP Program Listing-Continued

```
                    * STATUS CODE, INVERSION  & SHIFT   TO PROVIDE  ESB REG WITH
                    UNKNOWN/HOSTILE  BITS OF TRK MSGS <IE.  IIIIIIIIIII1HUI>
                    WHER E H/U ARE ZEROES FOR PASS ESB CASE
                    *
                    * BST IN AND WE'LL CFB BACK , RETURNS ANSWER IN ACCUM
0216    300B    FNY5Z   CFA     TEMP            SURE HOPE IT IS ONLY TWO BITS
0217    5CA1            SHF     AL, AS, 2       MP4 BY 4
0218    500B            ADD     TEMP            NOW WE HVE IT X 5
0219    40AB            AND     X6, A           SAVE JUST THE H AND U BITS
021A    1020            CBA     ACC, N          FLIP WHOLE MESS
021B    6000            CFB     RET             HERE I COME , GLAD IT IS  OVER
                    *
                    * STRANGE AS IT MAY SEEM THE FOLLOWING SHOULD
                    *  HANDLE  ALL SWITCHES REF'D FOR TOWAY
                    *
                    * THE FOLLOWING FUNNY STRING GENERATES BASIC CORRECT INDEX
                    * NUMBERS FOR ALL KINDS OF FUNNY SWITCHES AND THINGS
                    * ACCUMULATOR CONTAINS INITIAL INDEX ON ENTRY
021C    54A8    SW016   SUB     X3, A           SWITCH 16-18 BLOCK CORRECTION
021D    54A6    SW019B  SUB     X1, A                   "       19(&20)"        "
021E    54A6    SW030   SUB     X1, A                   "       30      "
021F    54AB    SW031   SUB     X6, A                   "       31-36   "                       "
0220    54A7    SW037   SUB     X2, A                   "       37-39   "               "
0221    54A7    SW082   SUB     X2, A                   "       82      "               "
                    *
                    * TOWAY SUBROUTINES
                    *
                    * TWO BRANCH SERVICE SUBROUTINE TO SUPPORT SWITCH NUMBERS
                    * 16-18, 19 , 30-39X33, AND MAY BE MORE, 82
                    *
                    * USES THE SWITCH FUNCTION TABLES LOBIT1, AND LOBITO
                    *       LOCATED IN UPPER FILE FROM
                    *  AND      STORES GARBAGE IN TABLE GARB IN  RAM FILE
                    *
                    * ACC CONTAINS LATEST INDXWC ON ENTRY
0222    2037    TOWAY1  STA     INDXWC          CORRECT INDEX NUMBER
0223    340B            CFO     TEMP
0224    4DEA            ESB     XFFFE, O        CHECK LO ORDER BIT
0225    54F7            SUB     MGICLO          REVERT TO TABLE LOBIT
0226    50F8            ADD     LBTDEL, A       POINT TO LOBIT1
0227    OCO0            CBI     ACC             LOAD INDEX
0228    32FF            CFA     ELBL, I         PICKUP CONSTANT
0229    6C37            CFI     INDXWC          GET INDEX AGAIN
022A    2238            STA     GARB, I         STORE IN RAM LOC
022B    791C            CCB     BRO3            THIS COMMON LAMP EXIT
                    *
                    * REGISTER4 SUBROUTINE -- RGSTR4 -- CLEARS UP BAD LAMP REFRESH
                    *  DUE TO MUTUAL EXCLUSIVITY OF SWITCHES 19-20, 22-23
                    * ENTER BY BST TO RGSTR4 , LEAVE BY CFB THROUGH RET
                    * ASSUMES: OPERAND HAS FIXED UP SWITHCH INDEX: 22-23 LOAD W/SWFUIN
                    *                                                 20      =       1
                    *                                                 19      =       0 = SWFUIN
```

Table 5-36. AP Program Listing-Continued

```
                        *       SWITCH 4 = 1 IF ENTER FROM 22-23 PROCESSOR
                        *                = 0 IF ENTER FROM 19-20 PROCESSORS
                        * ASSUMES LAMP OUTPUT ROUTINE  FOLLOWS
                        *
022C    300B  RGSTR4    CFA     TEMP            GET LAMP STATUS
022D    71A6            EQS     X1, 0           SHOULD WE SHIFT MASK??
022E    5CA1            SHF     AL, AS, 2       SHIFT FOR HIGHER RANK SWITCH
022F    200B            STA     TEMP            SAVE IT AWHILE
0230    300F            CFA     STATUS          PICKUP PATTERN
0231    0810            TSS     S4              WAS THIS SWITCH 22-23?
0232    5C15            SHF     AR, 6           YES - RIGHT JUSTIFY FIELD
0233    40E4            AND     XFFFO, A        BOMB LOWER "OTHER SWITCH" BITS
0234    480B            ORI     TEMP            PUT IN RIGHT CODE
0235    0810            TSS     S4              WAS THIS 22-23??
0236    5C25            SHF     AL, 6           YES- SHIFT BACK
0237    200F            STA     STATUS          RESTORE IT TO STATUS
0238    30B4            CFA     X14
0239    79DE            CCB     OUTPUT
                        *
                        *  LON & LOFF ARE USED TO LIGHT LAMP 48 WHENEVER A
                        * LINTICULAR SWITCH IS PUSHED.  48 WILL LIGHT ONLY
                        * FOR THE DURATION OF THE SWITCH PUSH.
                        *
023A    6CA5    LON     CFI     XO              SET UP INDEX
023B    0808            TSS     S3              IS THIS STATUS REPORT?
023C    791C            CCB     BRO3            BRANCH IF SO
023D    7A3F            CCB     ++2             BRANCH IF NOT
023E    6CA6            CFI     X1              SET UP INDEX
023F    34D2            CFO     X8302           GET COMMAND
0240    79F8            BST     TALK+1          YELL AT FRONT PANEL
0241    1100            CBA     LOS             GET LAMP INFO
0242    40E1            AND     XFFCF, A        TURN OFF 48
0243    4AA4            ORI     X30, A, I       TURN ON AGAIN IF I=O
0244    200F            STA     STATUS          SAVE LAMP INFO FOR OUTPUT
0245    30A6            CFA     X1              GET LAMP GROUP
0246    7DDE            BST     OUTPUT          SPIT IT BACK TO FROONT PANEL
0247    62FA            CFB     RETADD, I       FINISHED

                        ******************************************************
                        *   MESSAGE PROCESSING
                        ******************************************************

                        ** MAIN ROUTINE ************************************************
                        *   - RECOGNIZES MESSAGES BY TYPE
                        - PASSES CONTROL TO PROPER SUBROUTINE
                        *
0248    07DF             MAIN   RSW     SO, S1, S2, S3, S4, S5, S6, S7, S8, S9 RESET
                                       SWITCHES
0249    1580            MAO     CBO     HIS     COPY INPUT
024A    0100                    TSS     S9      NEW MESSAGE
024B    603B             MA1    CFB     TEST    BRANCH IF SO
                        *  TEST - A<TST> IN TEST ?MODE, - A<NORM> IN NORMAL MODE
024C    7A49            CCB     MAO             BRANCH IF NOT
```

Table 5-36. AP Program Listing-Continued

```
024D   4DDE  NORM          ESB   XFF7F, O        TEST MESSAGE?
024E   7A57                CCB   MA2             BRANCH IF NOT
024F   7A48                CCB   MAIN            BRANCH IF SO
0250   41BO  TST           AND   XF, O           SAVE 4 LSB'S
0251   70BO                EQS   XF, A           END OF FILE?
0252   7820                CCB   EOF             BRANCH IF SO
0253   70AB                EQS   X6, A           CCON MESSAGE?
0254   7A57                CCB   MA2             BRANCH IF SO
0255   4DDE                ESB   XFF7F, O        TEST MESSAGE?
0256   7A48                CCB   MAIN            BRANCH IF NOT
0257   2408  MA2           STO   MSG             SAVE MSG WORD
0258   41BO                AND   XF, O           SAVE 4 LSB'S
0259   5046                AND   CMPSEL, A       COMPRESSOR MTAB OFFSET
                *CMPSEL=O FOR COMPRESSOR ON, =16 FOR OFF
025A   0C00                CBI   ACC             PUT IN INDEX
025B   041F                RSW   SO, S1, S2, S3, S4      RESET SWITCHES
025C   6280                CFB   MTAB, I         BRANCH TO SUBROUTINE
                *
                ** AUX READ OUT ***********************************************************
025D   7FD6  ARO           BST   CONCK           FOR THIS CONSOLE?
025E   3C08                CFH   MSG             SEND MSG WORD IF SO
025F   6CB8                CFI   X1F             SET INDEX
0260   1D80  H2H           CBH   HIS             HI-SPEED TO HI-SPEEF)
0261   7400                DIS                   DECREMENT INDEX
0262   7A60                CCB   H2H             BRANCH IF NOT -1
0263   7A48                CCB   MAIN            RETURN
                *
                ** FIRE UNIT    ************************************************************
0264   603A  FIRE   CFB  FIRSEL        ALL OR SELECTED F. U.?
                * FIRSEL = FIRE1 IF ALL F. U. DISPLAYABLE, - FIRE2 IF
                * SELECTED F .U., = MAIN IF NO F .U.
0265   2COB  FIRE1  STH   TEMP1    SAVE 2ND WORD
0266   7A69         CCB   FIRE3    BRANCH
0267   7FD6  FIRE2  BST   CONCK    FOR THIS CONSOLE?
0268   2008         STA   TEMP1    SAVE 2ND WORD
0269   1180  FIRE3  CBA   FANSEL   ALL OR SELECTED A/N?
026A   6039
                * FANSEL = FIRE5 IF ALL A/N DISPLAYABLE, = FIRE4 IF
                * SELECTED A/N, = FIRE6 IF NO A/N
026B   4C17  FIRE4  ESB   CONMSK, A            DISPLAY A/N?
026C   7A6E         CCB   FIRE6    BRANCH IF NOT
026D   0004  FIRE5  SSW   S2       SET SWITCH FOR A/N
026E   2C00  FIRE6  STH   RET      PURGE 4TH WORD
026F   7FDA         BST   CSCALE   COPY/SCALE X & Y
0270   3408         CFO   MSG      COPY MSG WORD
0271   300B         CFA   TEMP1    COPY 2ND WORD
0272   6040         CFB   PARSEL   PARING LINES SELECTED?
                * PARSEL = FIRE8 IF SELECTED, = FIRE7 IF NOT
0273   40E0  FIRE7  AND   XFFCO, A  ZERO DISPLAY BITS
0274   200B         STA   TEMP1    SAVE 'EM
0275   0820  FIRE8  TSS   S5       TIME TO BLINK?
0276   7A90         BLINK BRANCH IF SO
```

Table 5-36. AP Program Listing-Continued

```
0277    40E5            AND   XFFF3, A          ZERO DISPLAY BITS
0278    1C80    FI1     CBH   OPR               SEND MSG WORD
0279    0804            TSS   S2                CHARS DISPLAYABLE?
027A    48AD            - ORI X8, A             SET CHAR DISPLAY BIT IF SO
027B    1C00            CBH   ACC               SEND 2ND WORD
027C    3CO9            CFH   X                 SEND X
027D    3COA            CFH   Y                 SEND Y
                * DETERMINE WHETHER OR NOT TO SEND 1ST LINE & DO IT
027E    7FC9            BST   COPY              COPY X & Y
027F    340B            CFO   TEMPI             COPY 2ND WORD
0280    4DE2            ESB   XFFDF, 0          DISPLAY LINE 1?
0281    7A85            CCB   F13               BRANCH IF NOT
0282    7FEO            BST   SCALE             SCALE X & Y
0283    3CO9            CFH   X                 SEND X
0284    3COA            CFH   Y                 SEND Y
                *  DETERMINE WHETHER OR NOT TO SEND 2ND LINE & DO IT
0285    7FC9    F13     BST   COPY              COPY X & Y
0286    340B            CFO   TEMPI             COPY 2ND WORD
0287    4DE3            ESB   XFFEF, 0          DISPLAY LINE 2?
0288    7A8C            CCB   F15               BRANCH IF NOT
0289    7FEO    F14     BST   SCALE             SCALE X & Y
028A    3C09    F14A    CFH   X                 SEND X
028B    3COA            CFH   Y                 SEND Y
                *  SEND ALPHANUMERICS
028C    6CA9    F15     CFI   X4                SET INDEX
028D    0804            TSS   S2                DISPLAY CHARS?
028E    7A60            CCB   H2H               BRANCH IF SO
028F    7A48            CCB   MAIN              BRANCH IF NOT
                * BLINK SYMBOL & LINES
0290    40AF    BLINK   AND   XC, A             ISOLATE BLINK BITS
0291    5CA1            SHF   AL, AS, 2         SHIFT 2 PLACES LEFT
0292    44BA            ORX   X33, A            FLIP BLINK BITS
0293    400B            AND   TEMP1, A          MODIFY DISPLAY BITS
0294    200B            STA   TEMP1             SAVE MODIFIED WORD
0295    4DDF            ESB   XFFBFMO           BLINK SYMBOL?
0296    7A78            CCB   FI1               RETURN IF NOT
0297    341)7           CFO   XA002             COPY MSG WORD FOR BLINK
0298    7A78            CCBQFI1                 RETURN

                ** MAP ROUTINE ****************************************
0299    4D1C    MAP     ESB   MAPMSK, O         THIS MAP DISPLAYABLE?
029A    7A48            CCB   MAIN              RETURN IF NOT
029B    1180    MAPO    CBA   HIS               GET 2ND WORD
029C    4CE2            ESB   XFFDF, A          BLINK MAP?
029D     7AAO           CCB   MAP1              BRANCH IF NOT
029E    0820            TSS   S5                TIME TO BLINK?
029F    7A48            CCB   MAIN              RETURN IF SO
02AO    7FC9    MAP1    BST   COPY              COPY X & Y
02A1    0801            TSS   SO                DISPLAYABLE?
02A2    7AAF            CCB   MAP6              BRANCH IF NOT
02A3    3C08            CFH   MSG               SEND MESSAGE WORD
02A4    7AA6            CCB   MAP4              BRANCH
```

Table 5-36. AP Program Listing-Continued

```
F2A5    7FCA  MAP3    BST     COP                 COPY X & Y
F                     *  RAW DATA MUST BE SENT
F2A6    7FEO  MAP4    BST     SCALE               SCALE X & Y
F2A7    3C09          CFH     X                   SEND X
F2A8    3COA          CFH     Y                   SEND Y
F2A9    0801          TSS     SO                  IS IT DISPLAYABLE?
F2AA    7ABO          CCB     MAP7                BRANCH IF NOT
F                   * DISPLAYABLE POINT JUST SENT
02AB    1580          CBO     HIS                 COPY X
02AC    OAOO          TSS     S9                  NEW MESSAGE?
02AD    7A4B          CCB     MA1                 RETURN IF SO
02AE    7AA5          CCB     MAP3                BRANCH IF NOT
                    * PREVIOUS POINT NOT DISPLAYABLE
02AF    0008  MAP6    SSW     S3                  REMEMBER NOT SCALED
02BO    0603  MAP7    RSW     SO, S1, S9          RESET SWITCH
02B1    1580          CBO     HIS                 COPY X
02B2    OAOO          TSS     S9                  NEW MESSAGE
02B3    7A4B          CCB     MA1                 RETURN IF SO
02B4    3009          CFA     X                   COPY OLD X
02B5    200D          STA     TEMPX               SAVE IT
02B6    300A          CFA     Y                   COPY OLD Y
02B7    200E          STA     TEMPY               SAVE IT
02B8    7FCA          BST     COP                 COPY X & Y
02B9    0801          TSS     SO                  DISPLAYABLE?
02BA    7AAF          CCB     MAP6                BRANCH IF NOT
                    * DATA DISPLAYABLE - PREVIOUS POINT WAS NOT
02BB    0200          SSW     S9                  SET SWITCH
02BC    3CO8          CFH     MSG                 SEND MSG WORD
02BD    7FEO          BST     SCALE               SCALE X & Y
02BE    3CO9          CFH     X                   SEND X
02BF    3COAS         CFH     Y                   SEND Y
02CO    0808          TSS     S3                  PREVIOUS POINT SCALED?
02C1    7AC5          CCB     MAP8                BRANCH IF NOT
02C2    3COD          CFH     TEMPX               SEND OLD X
02C3    3COE          CFH     TEMPY               SEND OLD Y
02C4    7ACB          CCB     MAP9                BRANCH
                    * OLD POINT MUST BE SCALED & SENT
02C5    300D  MAP8    CFA     TEMPX               COPY X
02C6    7FE9          BST     SCA                 SCALE IT
02C7    Lc00          CBH     ACC                 SEND IT
02C8    300E          CFA     TEMPY               COPY Y
02C9    7FE9          BST     SCA                 SCALE IT
02CA    1C00          CBH     ACC                 SEND IT
                    * DISPLAYABLE, NEEDS MSG WORD
02CB    040B  MAP9    RSW     SO, S1, S3      RESET SWITCHES
02CC    1580          XVO     HIS                 COPY X
02CD    OAOO          TSS     S9                  NEW MESSAGE?
02CE    7A4B          CCB     MA1                 BRANCH IF SO
02CF    0200          SSW     S9                  SET SWITCH
02DO    3CO8          CFH     MSG                 SEND MSG WORD
02D1    3C09          CFH     X                   SEND X
02D2    3COA          CFH     Y                   SEND Y
02D3    7AA5          CCB     MAP3                BRANCH
```

Table 5-36. AP Program Listing-Continued

```
                ** SAFE CORRIDOR ************************************************
02D4    6044    SAFE   CFB  SAFSEL        DISPLAYABLE?
                *  SAFSEL = A(MAPO)  IF DISPLAYABLE, = A(MAIN) IF NOT
                *
                ** TRACK MESSAGE *************************************
02D4    4DDF    TRACK ESB    XFFBF, O                    SIM TEST TRACK
02D6    7AD8          CCB    TR1                         BRANCH IF NOT
02D7    603C          CFB    SIMTST                      BRANCH IF SO
                * SIMTST = TR1 IS SIM TEST TRACKS DISPLAYABLE
                = MAIN IF NOT
02D8    1580  TR1     CBO    HIS                         GET 2ND WORD
02D9    41AC          AND    X7, 0                       SAVE ID
02DA    OCOO          CBI    ACC                         PUT IN INDEX
02DB    4D17          ESB    CONMSK, 0                   DISPLAY FORCED?
02DC    7AE5          CCB    TR2                         BRANCH IF NOT
                * FORCED DISPLAY
02DD    2C00          STH    RET                         PURGE 3RD WORD
02DE    7F2E          BST    VECTOR                      VEL OR TYG DISPLAYABLE?
02DF    0408          RSW    S3                          FORCE VEL IF NOTHING ELSE
02EO    2C00          STH    RET                         PURGE 6TH WORD
02E1    2COD          STH    TEMPX                       . SAVE VEL
02E2    2COE          STH    TEMPY                       . COMPONENTS
02E3    7FDA          BST    CSCALE                      COPY/SCALE X &S Y
02E4    7BOO          CCB    TR6                         BRANCH
                * DISPLAY NOT FORCED
02E5    4D21    TR2   ESB    THREAT, O                   HIGH ENOUGH THREAT?
02E6    6041          CFB    THRSEL                      BRANCH IF NOT
                * THRSEL = MAIN IF SELECTED, - TR2A IF NOT
02E7    1180    TR2A  CBA    HIS                         GET 3RDF WORD
02E8    4E14          ESB    TRDTAB, I, A                SOURCE SELECTED?
02E9    7A48          CCB    MAIN                        BRANCH IF NOT
02EA    603E          CFB    TANSEL                      ALPHANUMERICS?
                * TANSEL = TR3 IF SELECTED, - TR4 IF NOT
02EB    4E19    TR3   ESB    TCDTAB, I, A                CHAR DISPLAYABLE?
02EC    0004    TR4   SSW    S2                          SET SWITCH IF NOT
02ED    1180          CBA    HIS                         COPY 4TH WORD
02EE    200B          STA    TEMP1                       SAVE IT
02EF    7F2F          BST    VECTOR+1                    VEL OR TTG DISPLAYABLE?
02FO    4D1F          ESB    TRVEC, O                    VEL DISPLAYABLE?
02F1    7AF3          CCB    *+2                         BRANCH IF NOT
02F2    0408          RSW    S3                          RESET SWITCH
02F3    300B          CFA    TEMP1                       GET 4TH WORD AGAIN
02F4    40BE          AND    X7F, A                      GET ALTITUDE STUFF
02F5    1400          CBO    ACC                         PUT IN OPERAND
02F6    6431          MCS    ALB                         ALT > LOWER BOUND?
02F7    6432          MCS    AUB                         ALT > UPPER BOUND?
02F8    603D          CFB    ALTSEL                      BRANCH IF NOT IN RANGE
                *  ALTSEL = MAIN IF SELECTED,    =      TR5 IF NOT
02F9    1580    TR5   CBO    HIS                         COPY VELOCITY
02FA    642F          MCS    VLB                         SPEED > LOWER BOUND?
02FB    6430          MCS    VUB                         SPEED > UPPER BOUND?
```

Table 5-36. AP Program Listing-Continued

```
02FC  6042          CFB   SPDSEL          RETURN IF NOT IN RANGE
                * SPDSEL = MAIN IF SELECTED, = TR5A IF NOT
02FD  2COD  TR5A    STH   TEMPX           . SAVE VEL
02FE  2COE          STH   TEMPY           . COMPONENTS
02FF  7FDA          BST   CSCSALE         COPY/SCALE X & Y
                * TRACK IS DISPLAYABLE
0300  3408  TR6     CFO   MSG             COPY MSG WORD
0301  49A4          ORI   X30,O           SET DISPLAY BITS
0302  0820          TSS   S5              TIME TO BLINK?
0303  7B27          CCB   TRBLNK          BRANCH IF SO
0304  0804  TR7     TSS   S2              DISPLAY CHARS?
0305  40E2          AND   XFFDF,A         RESET BIT IF NOT
0306  0808          TSS   S3              DISPLAY LINE?
0307  40E3          AND   XFFEF,A         RESET BIT IF NOT
0308  1C00          CBH   ACC             SEND MSG WORD
0309  0808          TSS   S3              DISPLAY LINE?
030A  7B21          CCB   TR11            BRANCH IF NOT
030B  0810          TSS   S4              TIME TO GO?
030C  7B1B          CCB   TR10            BRANCH IF NOT
030D  340D          CFO   TEMPX           COPY VEL X
030E  7F3B          BST   CONVRT          CONVERT TO TTG
030F  50CO          ADD   X400,A
0310  200D          STA   TEMPX           SAVE IT
0311  340E          CFO   TEMPY           COPY VEL Y
0312  7F3B          BST   CONVRT          CONVERT TO TTG
0313  50CO          ADD   X400,A
0314  200E          STA   TEMPY           SAVE IT
0315  340D  TR9     CFO   TEMPX           COPY TTG X
0316  64C2          MCS   XFFF            TOO BIG?
0317  7B42          CCB   SHFR            SCALE DOWN IF SO
0318  340E          CFO   TEMPY           COPY TTG Y
0319  64C2          MCS   XFFF            TOO BIG?
031A  7B42          CCB   SHFR            SCALE DOWN IF SO
031B  7B42  TR10    CFA   TEMPX           COPY X COMPONENT
031C  5009          ADD   X,A             ADD X
031D  1C00          CBH   ACC             SEND IT
031E  300E          CFA   TMEPY           COPY Y COMPONENT
031F  500A          ADD   Y,A             ADD Y
0320  1C00          CBH   ACC             SEND IT
0321  3CO9  TR11    CFH   X               SEND X
0322  3COA          CFH   Y               SEND Y
0323  0804          TSS   S2              DISPLAY CHARS?
0324  7A48          CCB   MAIN            BRANCH IF NOT
0325  6CA9          CFI   X4              SET INDEX
0326  7A60          CCB   H3H             BRANCH TO ARO ROUTINE
0327  4DE2  TRBLNK  ESB   XFFDF,O         BLINK SYMBOL?
0328  7B2A          CCB   TRB1            BRANCH IF NOT
0329  30C5          CFA   X2              035    REPLACE SYMBOL IF SO
032A  4DE3  TRB1    ESB   XFFEF,O         BLINK LINE
032B  7B04          CCB   TR7             BRANCH IF NOT
032C  0008          SSW   S3              SET SWITCH IF SO
032D  7B04          CCB   TR7             BRANCH
```

Table 5-36. AP Program Listing-Continued

```
032E  1180  VECTOR CBA   HIS          COPY 4TH WORD
032F  0010        SSW   S4           SET SWITCH
0330  4C17        ESB   CONMSK,A     VECTOR FORCED?
0331  0008        SSW   S3           SET SWITCH IF NOT
0332  1180  VECT1 CBA   HIS          COPY 5TH WORD
0333  4C17        ESB   CONMSK,A     TTG FORCED?
0334  7B37        CCB   VECT2        BRANCH IF NOT
0335  0418        RSW   S3,S4        RESET SWITCHES
0336  6000        CFB   RET          RETURN
0337  4D20  VECT2 ESB   TRTTG,0      TTG SELECTED
0338  6000        CFB   RET          RETURN IF NOT
0339  0418        RSW   S3,S4        RESET SWITCHES
033A  6000        CFB   RET          RETURN
033B  5CC2  CONVRT  SHF   OL,AS,3    SHIFT 3 PLACES
033C  3052        CFA   SP8S         PICK UP TTG SETTING
033D 4CC1         ESB   X7FF,A       . SCALE
033E  7B40        CCB   *+2          . VELOCITY
033F  5CC2        SHF   OL,AS,3      . VECTOR
0340  5823        MPY   TTG          MULTIPLY BY TTG
0341  7BE9        CCB   SCA          SCALE IT
0342  300D  SHFR  CFA   TEMPX        . DIVIDE
0343  5C90        SHF   AR,AS,1      . TTG X
0344  200D        STA   TEMPX        . AND
0345  300E        CFA   TEMPY        . TTG Y
0346  5C90        SHF   AR,AS,1      . BY
0347  200E        STA   TEMPY        . TWO
0348  7B15        CCB   TR9          RETURN
                  *
                  ** CONSOLE CONTROL MESSAGE **********************************
0349  7FD6  CCON  BST   CONCK        FOR THIS CONSOLE
034A  4DE3        ESB   XFFEF, O     INTERRUPT?
034B  7B4E        CCB   CC1          BRANCH IF NOT
034C  0100        SSW   S8           . DO IT
034D 0500         RSW   S8           . IF SO
                  *
                  * READ CONSOLE CONTROL MESSAGE INTO RAM FILE FOR PROCESSING
                  * DURING SWITCH PROCESSING TIME --DC CONSOLE CONTROL SENT
                  * BY SWITCH PROCESSOR
                  *
034E  2436  CC1   STO   CON01        STORE MSG WORD
034F  2           035   STA          CON02 STORE 2ND WORD
0350  6CAE        CFI   X9           INITIALIZE INDEX
0351  2E2B        STH   CONCON,I     ANOTHER WORD
0352  7400        DIS                ANY MORE??
0353  7B51        CCB   *-2          PICKUP ANOTHER FRPM INPUT
0354  681E        DFS   BLINKR       DECREMENT BLINK TIMER
0355  7A48        CCB   MAIN         RETURN IF NOT -1
0356  30AE        CFA   X9           . RESET
0357  201E        STA   BLINKR       . BLINKR
0358  0820        TSS   S5           SWITCH 5 SET?
0359  7B5C        CCB   CC2          BRANCH IF SO
035A  0020        SSW   S5           SET SWITCH 5
```

Table 5-36. AP Program Listing-Continued

```
035B  7A48          CCB   MAIN                RETURN
035C  0420  CC2     RSW   S5                  RESET SWITCH 5
035D  7A48          CCB   MAIN                RETURN
0     *
0     * TEST MESSAGE
0     *             - PROVIDES A DOU LOOP TEST.  THE SECOND WORD IN THE
0     *             TWO WORD MESSAGE IS RETURNED TO THE CPU IN FEEDBACK.
0     *
035E  2C4F  TSTMSG  STH   FLAG                SAVE
035F  2C50          STH   TEST1               TEST
0360  2C51          STH   TEST2               BITS AND
0361  7A48          CCB   MAIN                RETURN
      *
      ** HOOK MARKER MESSAGE **********************************
0362  HOOK  EQU   *
      *
      ** POINTER MESSAGE ***************************************
0362  7FD6  POINT BST   CONCK               FOR THIS CONSOLE
0363  7FDA        BST   CSCALE              COPY/SCALE X & Y
0364  3C08        CFH   MSG                 SEND MSG WORD
0365  7A8A        CCB   FI4A                BRANCH
      *
      ** FIXED POINT MESSAGE ***********************************
0366  1180  FIX   CBA   HIS                 COPY 2ND WORD
0367  4C17        ESB   CONMSK,A            DISPLAY?
0368  6045        CFB   FIXSEL              RETURN IF NOT
      *  FIXSEL - FIX1 IF SELECTED, - MAIN IF NOT
0369  7FDA  FIX1  BST   CSCALE              COPY/SCALE X & Y
036A  3008        CFA   MSG                 COPY MSG WORD
036B  4CE3        ESB   XFFEF               BLINK SYMBOL?
036C  7B6F        CCB   FIX2                BRANCH IF NOT
036D  0820        TSS   S5                  TIME TO BLINK?
036E  30D8        CFA   XAOOA               REPLACE MSG WORD IF SO
036F  1C00  FIX2  CBH   ACC                 SEND MSG WORD
0370  3C09        CFH   X                         SEND X
0371  3COA        CFH   Y                         SEND Y
0372  7BC5        CCB   TMK4                13RANCH
      *
      ** GEOREF MESSAGE ***************************************
0373  0002  GEO   SSW   S1                  SET SWITCH
0274  4D1C        ESB   MAPMSK,O            THIS MAP DISPLAYABLE?
0375  7A48        CCB   MAIN                BRANCH IF NOT
0376  2COB  GEO1  STH   TEMP1               SAVE 2ND WORD
0377  7FC9        BST   COPY                COPY X & Y
0378  340B        CFO   TEMP1               COPY 2ND WORD
0379  4D19        ESB   GEOMSK,O            THIS POINT DISPLAYABLE?
037A  0801        TSS   SO                  ARE YOU SURE???
037B  7B83        CCB   GEO2                BRANCH IF NOT
037C  0802        TSS   S1                  SWITCH 1 SET
037D  3C08        CFH   MSG                 SEND MSG WORD
037E  0783        RSW   SO,S1,S7,S8,S9      RESET SWITCHES
037F  3COB        CFH   TEMP1               SEND 2ND WORD
```

Table 5-36. AP Program Listing-Continued

```
0380  7FEO          BST   SCALE              SCALE X & Y
0381  3C09          CFH   X                  SEND X
0382  3COA          CFH   Y                  SEND Y
0383  0401  GEO2    RSW   SO                 RESET SWITCH
0384  1580          CBO   HIS                COPY NEXT WORD
0385  7108          EQS   MSG,O              SAME AS LAST TIME???
0386  7B76          CCB   GEO1               BRANCH IF SO
0387  7A4A          CCB   MAO+1              BRANCH IF NOT
                    *
                    ** JAM STROBE MESSAGE *********************************
0388  6043  JAM     CFB   JAMSEL             JAM STROBES SELECTED
                    * JAMSEL = A(JAMO) IF DISPLAYABLE, = A(MAIN) IF NOT
0389  6CA9  JAMO    CF1   X4                       SAVE
038A  2E4A          STH   TEMPJS,I                 THE
038B  7400          DIS                            TEN
038C  7B8A          CCB   *-2                      ALPHAS
038D  7FC9          BST   COPY               COPY X & Y
038E  0801          TSS   S0                 DISPLAYABLE?
038F  7BAB          CCB   JAM1               BRANCH IF NOT
                    * ALPHANUMERICS ARE DISPLAYABLE - SEND THEM
0390  3CD8          CFH   XA00A              SEND FXD PNT MSG TYPE
0391  30AD          CFA   X8                 DO NOTHING
0392  7FEO          BST   SCALE              SCALE X & Y
0393  3CO9          CFH   X                        SEND X
0394  3COA          CFH   Y                        SEND Y
0395  6CA9          CFI   X4                       SEND
0396  3E4A          CFH   TEMPJS,I                 THE
0397  7400          DIS                            TEN
0398  7B96          CCB   *-2                      ALPHAS
                    *  ALPHANUMERICS JUST SENT
0399  3009          CFA   X                  COPY X
039A  200B          STA   TEM1               SAVE IT
039B  300A          CFA   Y                  COPY Y
039C  200C          STA   TEMP2              SAVE IT
039D  7FC9          BST   COPY               COPY X & Y
039E  7FEO          BST   SCALE              SCALE X & Y
039F  0200          SSW   S9                 SET SWITCH
03AO  3CCF          CFH   X800E              SEND CMAP MSG TYPE
03A1  3COB          CFH   TEMP1              SEND X
03A2  3COC          CFH   TEMP2              SEND Y
03A3  3C09          CFH   X                  SEND X
03A4  3COA          CFH   Y                  SEND Y
03A5  0200          SSW   S9                 SET SWITCH 9
03A6  3CCF          CFH   X800E              SEND CMAP MSG TYPE
03A7  3COB          CFH   TEMP1              SEND X
03A8  3COC          CFH   TEMP2              SEND Y
03A9  7FC9          BST   COPY               COPY X & Y
03AA  7A89          CCB   F14                BRANCH
                    * ALPHANUMERICS NOT DISPLAYABLE
03AB  34CF  JAM1    CFO   X800E              . CHANGE MSG TYPE
03AC  2400          STO   MSG                . TO CLUTTER MAPPER
03AD  0401          RSW   SO                 RESET SWITCH
```

Table 5-36. AP Program Listing-Continued

```
03AE    7AA0            CCB   MAP1              BRANCH TO MAP ROUTINE
0               *
0               ** TRACK MARKER MESSAGE ***********************************************
03AF    6038    TMKR    CFB   TMRSEL            ALL TMRKS SELECTED?
0               * TMRSEL - TMK1 IF ALL TMKRS DISPLAYABLE, = TMK2 IF
0               * SELECTED TMKRS, = MAIN IF NO TMKRS
03BO0   2C00    TMK1    STH   RET               PURGE 2ND WORD
03B1    7BB3            CCB   TMK3              BRANCH
03B2    7FD6    TMK2    BST   CONCK             FOR THIS CONSOLE?
03B3    2C0B    TMK3    STH   TEMP1             SAVE 3RD WORD
03B4    2C00            STH   RET               PURGE 4TH WORD
03B5    7FDA            BST   CSCALE            COPY/SCALE X & Y
03B6    3008            CFA   MSG               COPY MSG WORD
03B7    4CE3            ESB   XFFEF,A           BLINK SYMBOL?
03B8    7BBB            CBB   TMK               BRANCH IF NOT
03B9    0820            TSS   S5                TIME TO BLINK?
03BA    30C6            CFA   X200D             REPLACE MSG WORD IF SO
03BB    40DD    TMK     AND   XFFOF,A           ZERO DISPLAY BITS
03BC    340B            CFO   TEMP1             COPY 3RD WORD
03BD    4D17            ESB   CONMSK,O          DISPLAY CHARACTERS?
03BE    7BC0            CCB   TMKO              BRANCH IF NOT
03BF    48B1            ORI   X10,A            SET CHAR BIT IF SO
03CO    1C00    TMK0    CBH   ACC               SEND MSG WORD
03C1    3C09            CFH   X                 SEND X
03C2    3COA            CFH   Y                 SEND Y
03C3    4D17            ESB   CONMSK,O          DISPLAY CHARACTERS?
03C4    7A48            CCB   MAIN              BRANCH IF NOT
03C5    6CA9    TMK4    CFI   X4                SET INDEX
03C6    7A60            CCB   H2H               BRANCH TO ARO ROUTINE
                *
                ** CLUTTER MAPPER ******************************************************
03C7    7FD6    CMAP    BST   CONCK             FOR THIS CONSOLE
03C8    7AAO            CCB   MAP1              BRANCH TO MAP ROUTINE
                *
                ** COPY X & Y ROUTINE ***************************************************
03C9    1580    COPY    CBO   HIS               COPY X
03CA    5534    COP     SUE   XOFF,O            SUBTRACT OFFSET
03CB    1400            CBO   ACC               PUT IN OPERAND
03CC    6424            MCS   WINDOW            DISPLAYABLE?
03CD    0001            SSW   SO                SET SWITCH IF NOT
03CE    2409            STO   X                 SAVE X
03CF    1180            CBA   HIS               COPY Y
03DO    5433            SUB   YOFF,A            SUBTRACT OFFSET
03D1    1400            CBO   ACC               PUT IN OPERAND
03D2    6424            MCS   WINDOW            DISPLAYABLE?
03D3    001             SSW   SO                SET SWITCH IF NOT
03D4    240A            STO   Y                 SAVE Y
03D5    6000            CFB   RET               RETURN
                *
                ** CONSOLE CHECK *******************************************************
03D6    1180    CONCK   CBA   HIS               COPY 2ND WORD
03D7    4C17            ESB   CONMSK,A          FOR THIS CONSOLE?
```

Table 5-36. AP Program Listing-Continued

```
03D8  7A48          CCB   MAIN          BRANCH IF   NOT
03D9  6000          CFB   RET           RETURN IF   SO
                    *
                    ** COPY & SCALE ROUTINE ************************************
03DA  3000  CSCALE  CFA   RET           COPY RETURN ADDR
03DB  2007          STA   RET2          SAVE IT
03DC  7FC9          BST   COPY          COPY X & Y
03DD  0801          TSS   SO            DISPLAYABLE?
03DE  7A48          CCB   MAIN          BRANCH IF   NOT
03DF  7BE2          CCB   SCAL          BRANCH IF   SO
                    *
                    ** SCALE ROUTINE ***************************************
03EO  3000  SCALE   CFA   RET           COPY RETURN ADDR
03E1  2007          STA   RET2          SAVE IT
03E2  3009  SCAL    CFA   X             COPY X
03E3  7FE9          BST   SCA           SCALE X
03E4  2009          STA   X             SAVE IT
03E5  300A          CFA   Y             COPY Y
03E6  7FE9          BST   SCA           SCALE Y
03E7  200A          STA   Y             SAVE IT
03E8  6007          CFB   RET2          RETURN
03E9  6C25  SCA     CFI   RANGE         SET INDEX
03EA  62A0          CFB   SHTAB,I       BRANCH
                    * SHTAB = SH3,SH2,SH1,SH0
03EB  5C92  SH3     SHF   AR,AS,3       SHIFT ACCUM RIGHT
03EC  7BF2          CCB   SHO           BRANCH
03ED  5C90  SH2     SHF   AR,AS,1       SHIFT ACCUM RIGHT
03EE  1400          CBO   ACC           PUT VALUE IN OPERAND
03EF  5822          MPY   POT           MULTIPLY
03FO  7BF2          CCB   SH0           BRANCH
03F1  5C90  SH1     SHF   AR,AS,1       SHIFT ACCUM RIGHT
03F2  54C0  SH0     SUB   X400,A        SUBTRACT RADIUS
03F3  6000          CFB   RET           RETURN
03FA                SPA   #3FA
03FA  2002  DOULPT  STA   SP8           SAVE FOR OUTPUT
03FB  2052          STA   SP8S          SAVE FOR CONVRT
03FC  795F          CCB   #15F          RETURN TO TTG
                    *
                          ************************************************
                          * STORAGE & CONSTANTS
                          ************************************************
F     0000          FILE  SFA   *
F     0000          RET   DS    1         RETURN ADDR
F     0001          ERROR DS    1         ERROR ENTRY GUY
F     0002          SP8   DS    1       HOLDS COMBINED TTG AND VRS
F     0003          LOCY  DS    1       HOLDS Y FORCE STICK
F     0004          LOCX  DS    1       HOLDS X FORCE STICK
F     0005          SO1   DS    1
F     0006          SP3   DS    1       HOLDS STATUS WORD
F     0007          RET2  DS    1       RETURN SAVE AREA
F     0008          MSG   DS    1         MESSAGE WORD SAVE AREA
F     0009          X     DS    1         X STORAGE
```

Table 5-36. AP Program Listing-Continued

```
F     000A          Y          DS    1                 Y STORAGE
F     000B          TEMP1      DS    1                 .
F     000C          TEMP2      DS    1                 . TEMP
F     000D          TEMPX      DS    1                 . STORAGE
F     000E          TEMPY      DS    1
F     000E          TSP12      EQU   TEMPY
F     00OB          TEMP       EQU   TEMP1
F     0008          TSP2       EQU   MSG
F     0009          TSP3       EQU   X
F     00OA          TSP4       EQU   Y
F     0007          TSP5       EQU   RET2
F     00OC          TSP10      EQU   TEMP2
F     00OD          TSP11      EQU   TEMPX
F     00OF          STATUS     DS    1
F     0010          SP2        DS    1                 HOLDS OLD SWITCH CODE
F     0011          SP4        DS    1
F     0012          SP9        DS    1                 HOLDS CURRENT SW FDBK CODE
F     0013          SPIN       DS    1                 HOLDS SHIFT INDEX
F     *
F     0014          TRDTAB     DS    5                 TRACK DISPLAY TABLE
                    * TRDTAB(1) FOR DISPLAY OF FRIENDLY TRACKS
                    * TRDTAB(2) FOR DISPLAY OF UNKNOWN TRACKS
                    * TRDTAB(4) FOR DISPLAY OF HOSTILE TRACKS
F     0014          PHS        EQU   TRDTAB           PREVIOUS HAPPENING SAVE
F     0017          CONMSK     EQU   TRDTAB+3          CONSOLE MASK
                    * CONMSK IS ALL ONES EXCEPT FOR A ZERO FOR THE CONSOLE NO.
F     0019          TCDTAB     DS    5                 TRACK DISPLAY TABLE
                    * TCDTAB(1) FOR DISPLAY OF A/N FOR FRIENDLY TRACKS
                    * TCDTAB(2) FOR DISPLAY OF A/N FOR UNKNWOWN TRACKS
                    * TCDTAB(4) FOR DISPLAY OF A/N FOR HOSTILE TRACKS
F     0019          GEOMSK  EQU   TCDTAB              GEOREF      MASK
                    * GEOMSK = X'FF7F' IF ON X1 SCALE, =X'FFFF' OTHERWISE
F     001C          MAPMSK  EQU   TCDTAB+3            MAPMSK
                    * MAPMSK IS ALL ONES EXCEPT ZEROS FOR IMAP NUMBERS
F     001E          BLINKR     DS    1                 BLINK COUNTER
F     001F          TRVEC      DS    1                 TRACK VECTOR DISPLAY
                    *TRVEC INDICATES DISPLAY OF  VECTORS FOR FRIEND, UNKNOWN,
                    * OR HOSTILE TRACKS WITH 0 IN 1ST, 2ND, OR 3RD LSB.
F     0020          TRTTG      DS    1                 TRACK TIME TO GO
                    *  TRTTG INDICATES DISPLAY OF      TTG FOR FRIEND, UNKNOWN,
                    * OR HOSTILE TRACKS WITH 0 IN 1ST, 2ND, OR 3RD LSB
F     0021          THREAT     DS    1                 THREAT MASK
F     0022          POT        DS    1                 VARIABLE RANGE SETTING
F     0023          TTG        DS    1                 TTG MULTIPLIER
F     0024          WINDOW DS    1                   DISPLAYABILITY WINDOW
                    * WINDOW = X'IF90' ON X1, X'FC8' ON X2, X'7E4' ON X4,
                    * X'3F2' ON X8, OR X'7EO'/POT ON RUBBER RANGE
F     0025          RANGE      DS    1
                    *  RANGE = 0 ON X1, 1 ON X2, 2 ON X4, OR 3 ON X8 RANGE
F     0026          SWFUIN     DS    1                 SWITCH FUNCTION INDEX-SWITCH PROC
F     0027          TMPWC      DS    1                 SCRATCH      -SWITCH PROC
F     0028          SRCMTR     DS    1                 SOURCE MASTER     -ALL
```

Table 5-36. AP Program Listing-Continued

```
F     0029          TMPNC1  DS    1          SCRATCH     --SWITCH PROC
F     002A          TMPWC2  DS    1          SCRATCH     -SWITCH PROC
F                   *
F                   * CONSOLE CONTROL MESSAGE PROCESSING DURING SWITCH PROCESSING
F                   * TIME ASSUMES THAT 12 WORD ARRAY STORED IN RAM FILE LOCATIONS
F                   * AS FOLLOWS IN MESSAGE FORMAT XCEPT FOR CONTROL BIT 16 OF        CONI01
F     002B          CONCON  EQU   *
F     002B          CON12   DS    1          MASTER SOURCE IN
F     002C          CON11   DS    1          WINDOW-GOOD ONLY IN RUBBER RANGE
F     002D          CON10   DS    1          FLOOD INPUT
F     002E          CON09   DS    1          RANGEOVER, THREAT, CONPRESSOR RANGE
F     002F          VLB     EQU   *
F     002F          CON08   DS    1          SPEED LOWER BOUND
F     0030          VUB     EQU   *
F     0030          CON07   DS    1          SPEED UPPER BOUND
F     0031          ALD     EQU   *
F     0031          CON06   DS    1          ALT    LOWER BOUND
F     0032          AUB     EQU   *
F     0032          CON05   DS    1          ALT    UPPER BOUND
F     0033          YOFF    EQU   *
F     0033          CON04   DS    1          Y OFFSET
F     0034          XOFF    EQU   *
F     0034          CON03   DS    1          X OFFSET
F     0035          CON02   DS    1          TTG & CONSOLE ADDRESS
F     0036          CONO1   DS    1          MESSAGE TYPE & SWITCH ACTION INPUT
F     0037          INDXWC  DS    1          INDEX NUMBER      -SWITCH PROC
*
F     0038          GARB    EQU   *                 GARB TABLE START DEFINITION
F     0038          TMRSEL  DS    1
F     0039          FANSEL  DS    1
F     003A          FIRSEL  DS    1
F     003B          TEST    DS    1
F     003C          SIMST   DS    1
F     003D          ALTSEL  DS    1
F     003E          TANSEL  DS    1
F     000F                  DS    1                DONT USE
F     0040          PARSEL  DS    1
F     0041          THRSEL  DS    1
F     0042          SPDSEL  DS    1
F     0043          JAMSEL  DS    1
F     0044          SAFSEL  DS    1
F     0045          FIXSEL  DS    1
F     0046          CMPSEL  DS    1
F     0047          RONRO   DS    1                RADAR ONLY OFFSET CONNECTOR
                    * RONRO=ROOFF FOR RADAR ONLY,=ROCENT RDR CENTERED
                    *       =NRMOF FOR NOT RADAR ONLY MODE
F     0048          CNTRL   DS    1                UNARY CONTROL BITS FROM CONCON
                                                   MSG
                    *
F     0049          RDRO    DS    1                RADAR ONLY EOF    MAIN CONNECTOR
F     004A          TEMPJS  DS    5
F     004F          FLAG    DS    1
F     0050          TEST1   DS    1
```

Table 5-36. AP Program Listing-Continued

```
F    0051          TEST2    DS    1
F    0052          SP8S     DS    1
F    0080                   SFA   #80              128-255 IS PROM
F    0080    0248  MTAB     DC    MAIN,ARO,FIRE,MAP,SAFE,TRACK
F    0081    025D
F    0082    0264
F    0083    0299
F    0084    02D4
F    0085    02D5
F    0086    0349           DC    CCON,HOOK,TSTMSG,POINT,FIX
F    0087    0362
F    0088    035E
F    0089    0362
F    008A    0366
F    008B    0373           DC    GEO,JAM,TMKR,CMAP,EOF
F    008C    0388
F    008D    03AF
F    008E    03C7
F    008F    0020
F    0090    0248  MTAB1    DC    MAIN,MAIN,MAIN,MAIN,MAIN,MAIN
F    0091    0248
F    0092    0248
F    0093    0248
F    0094    0248
F    0095    0248
F    0096    0349           DC    CCON,HOOK,TSTMSG,POINT,MAIN
F    0097    0362
F    0098    035E
F    0099    0362
F    009A    0248
F    009B    0248           DC    MAIN,MAIN,MAIN,MAIN,EOF
F    009C    0248
F    009D    0248
F    009E    0248
F    009F    0020
F    00A0    03EB  SHTAB    DC    SH3,SH2,SH1,SHO
F    00A1    03ED
F    00A2    03F1
F    00A3    03F2
F    00A4    03F2
F    00A4    0030  X30      DC    #30                    ** MUST BE
F    00A5    0000  XO       DC    0                      ** IN ORDER
F    00A6    0001  X1       DC    1
F    00A7    0002  X2       DC    2
F    00A8    0003  X3       DC    3
F    00A9    0004  X4       DC    4
F    00AA    0005  X5       DC    5
F    00AB    0006  X6       DC    6
F    00AC    0007  X7       DC    7
F    00AD    0008  X8       DC    8
F    00AE    0009  X9       DC    9
F    00AF    000C  XC       DC    12
```

Table 5-36. AP Program Listing-Continued

```
F    00B0    000F    KF      DC   15
F    00B1    0010    X10     DC   16
F    00B2    0012    X12     DC   18
F    00B3    0013    X13     DC   19
F    00B4    0014    X14     DC   #14
F    00B5    0015    X15     DC   #15
F    00B6    0019    X19     DC   #19
F    0087    0020    X20     DC   #20
F    00B8    001F    X1F     DC   #1F
F    00B9    00D9    XD9     DC   #D9
F    00BA    0033    X33     DC   #33
F    00BB    003F    X3F     DC   63
F    00BC    006F    X6F     DC   111
F    00BD    0074    X74     DC   #74
F    00BE    007F    X7F     DC   #7F        127 IS SWITCH LIMIT
F    00BF    00FF    XFF     DC   #FF
F    00CO    0400    X400    DC   #400
F    00OC1   07FF    X7FF    DC   #7FF
F    00C2    0FFF    XFFF    DC   #FFF
F    00C3    1110    X1110   DC   #1110
F    00C4    1F88    X1F88   DC   #1F88
F    00C5    2035    X2035   DC   #2035
F    00C6    200D    X200D   DC   #200D
F    00C7    2B2G    X2B2B   DC   #2B28
F    00C8    4000    X4000   DC   #4000      ACTION CODE = AN
F    00C9    4002    X4002   DC   #4002
F    00CA    5550    X5550   DC   #5550
F    00CB    7F00    X7F00   DC   #7F00      SEVEN   GRAY OY) BINARY
F    00CC    7FF0    X7FF0   DC   #7FF0
F    00CD    7FFF    X7FFF   DC   #7FFF
F    00CE    8000    X8000   DC   #8000      ACTION CODE = NO SWITCH
F    00CF    800E    X800E   DC   #800E
F    00D0    8102    X8102   DC   #8102
F    00D1    8181    X8181   DC   #8181      FSTK MAG MASK
F    00D2    8302    X8302   DC   #8302
F    00D3    8402    X8402   DC   #8402      VAR RANGE CMD
F    00D4    8602    X8602   DC   #8602      FORCE STICK CMD
F    00D5    8802    X8802   DC   #8802      TIME TO GO CMD
F    00D6    8E02    X8E02   DC   #8E02      SWITCH COMMAND
F    0017    A002    XA002   DC   #A002
F    00D8    A00A    XA00A   DC   #A00A
F    00D9    C000    XC000   DC   #C000      ACTION CODE = CONS SWITCH
F    00DA    DFFF    XDFFF   DC   #DFFF
F    00DB    F7FF    XF7FF   DC   #F7FF      CHECK FOR RELOAD OF VIDCP
F    00DC    FF00    XFF00   DC   #FF00
F    00DD    FFOF    XFFOF   DC   #FFOF
F    00DE    FF7F    XFF7F   DC   #FF7F
F    00DF    FFBF    XFFBF   DC   #FFBF
F    00E0    FFC0    XFFC0   DC   #FFCO
F    00E1    FFCF    XFFCF   DC   #FFCF
F    00E2    FFDF    CFFDF   DC   #FFDF
F    00E3    FFEF    XFFEF   DC   #FFEF
```

Table 5-36. AP Program Listing-Continued

```
F    00E4   FFF0   XFFF0   DC   #FFFO
F    00E5   FFF3   XFFF3   DC   #FFF3
F    00E6   FFF8   XFFF8   DC   #FFF8
F    00E7   FFFB   XFFFB   DC   #FFFB
F    00E8   FFFC   XFFFC   DC   #FFFC
F    00E9   FFFD   XFFFD   DC   #FFFD
F    00EA   FFFE   XFFFE   DC   #FFFE          MASK          - SWITCH PROC
F    00EB   FFFF   XFFFF   DC   -1
F    00EC   0040   X40     DC   #40            ** MUST
F    00ED   0080   X80     DC   #80            ** BE
F    00EE   0100   X100    DC   #100           ** IN
F    00EF   0200   X200    DC   #200           ** ORDER
F    00F0   0147   NRMOF1  DC   NRMOF          NOT RADAR ONLY OFFSETS
F    00F1   013A   R00F    DC   R00FF
F    00F2   0021   TABL2   DC   MANADD-IFILE
F    00F2   00BO   114     DC   14+MANADD-ELBL
F    00F4   00B2   116     DC   16+MANADD-ELBL
F    00F5   00OC1  131     DC   31+MANADD-ELBL
F    00F6   00C2   I32     DC   32+MANADD-ELBL
F    00F7   0010   MGICLO  DC   LOBIT1-LOBIT0
F    00F8   00D3   LBTDEL  DC   LOBIT1-ELBL
F    00F9   00E3   ALGOFF  DC   ALITAB-ELBL
F    00FA   010C   RETADD  DC   BR03,BLANK1
F    00FB   0010
F    00FC   001B   ATIME   DC   TIME
F    00FD   0250   ROTST   DC   TST
F    00FF          ELBL    SFA  255
F    0180          IFILE   SFA  384           INDEXED FILE (384-511)
F    0180   8EOl1          DC   #8E01         I=O    SWITCH 1-12
F    0181   A60D           DC   #A60D         I=1    SWITCH 13-15
F    0182   A30D           DC   #A30D         I=2    SWITCH 16-18
F    0183   A70D           DC   #A70D         I=3    SWITCH 19
F    0184   A20D           DC   #A20D         I=4    SWITCH 20
F    0185   A50D           DC   #A50D         I=5    SWITCH 21
F    0186   A70D           DC   #A70D         I=6    SWITCH 22-23
F    0187   A70D           DC   #A70D         I=7    SWITCH 24
F    0188   BC19           DC   #BC19         I=8    SWITCH 25
F    0189   B019           DC   #BD19         I=9    SWITCH 26
F    018A   B819           DC   #B819         I=10   SWITCH 27-29
F    018B   8819           DC   #B819         I=11   SWITCH 30
F    018C   B819           DC   #B819         I=12   SWITCH 31-36
F    018D   3825           DC   #3825         I=13   SWITCH 37-39
F    018E   0828           DC   #0828         I=14   SWITCH 40-51
F    018F   0080           DC   #80           I=15   SWITCH 52-63
F    0190   0080           DC   #80           I=16   SWITCH 64
F    0191   41)41          DC   #4D41         I=17   SWITCH 65
F    0192   4841           DC   #4841         I=18   SWITCH 66-70
F    0193   0080           DC   #80           I=19   SWITCH 71  ILLEGAL
F    0194   3045           DC   #3045         I=20   SWITCH 72-74
F    0195   0080           DC   #80           I=21   SWITCH 75-79
F    0196   CB50           DC   #CB50         I=22   SWITCH 80
F    0197   CB50           DC   #CB50         I=23   SWITCH 81-82
```

Table 5-36. AP Program Listing-Continued

```
F    0198   2153                DC   #2153            I=24 SWITCH 83-86
F    0199   2253                DC   #2253            I=25 SWITCH 87
F    019A   2153                DC   #2153            I=26 SWITCH 88
F    019B   2053                DC   #2053            I=27 SWITCH 89-94
F    019C   385C                DC   #385C            I=28 SWITCH 95-97LLEGAL
F    019D   0080                DC   #80              I=29 SWITCH 98-109
F    019E   0080                DC   #80              I=30 SWITCH 110 ILLEGAL
F    019F   186C                DC   #186C            I=31 SWITCH 111-116
F    01A0   0080                DC   #80              I=32 SWITCH 117-127
F    01A1   C0E1   MANADD       DC   SW001+#COO0      I=0     SW001-12
F    01A2   3031                DC   SW013+#3000      I=1     SW013-15
F    01A3   321C                DC   SW016+#3000
F    01A4   10EE                DC   SWO19+#1000      I=3     SW019
F    01A5   10ED                DC   SW010+#1000      I=4     SW020
F    01A6   10F3                DC   SW021+#1000      I=5     SW021
F    01A7   2109                DC   SW022+#2000      I=6     SW022-23
F    01A8   10F6                DC   SW024+#1000      I=7     SW024
F    01A9   111C                DC   BR03+#1000       I=8             SW025
F    01AA   10FA                DC   SW026+#1000      I=9     SW026
F    01AB   30FE                DC   SW027+#3000      I=10    SW027
F    01AC   121E                DC   SW030+#1000      I=11    SW030
F    01AD   621F                DC   SW031+#6000      I=12    SW031
F    01AE   3220                DC   SW037+#3000      I=13    SW037
F    0l1AF  C11C                DC   BR03+#C000       I=14    SW040-51 DUMMY
F    01B0   C23A                DC   LON+#C000        I=15    SW052-63 DUMMY
F    01B1   111C                DC   BR03+#1000       I=16            SW064
F    01B2   111C                DC   BR03+#1000       I=17    SW065
F    01B3   511C                DC   BR03+#5000       I=18    SW066-70
F    01B4   11BB                DC   FAULTY+#1000     I=19            SW071
F    01B5   311C                DC   BR03+#3000       I=20            SW072
F    01B6   511C                DC   BR03+#5000       I=21            SW075
F    01B7   111C                DC   BR03+#1000       I=22    SW080
F    01B8   211A                DC   SW081+#2000      I=23    SW081-82 (82 ONLY REALLY)
F    01B9   411C                DC   BR03+#4000       I=24            SW083
F    01BA   111C                DC   BR03+#1000       I=25            SW087
F    01BB   111C                DC   BR03+#1000       I=26            SW088
F    01BC   611C                DC   BR03+#6000       I=27    SW089-94
F    01BD   311C                DC   BR03+#3000       I=28    SW095-97
F    01BE   C11C                DC   BR03+#COO0       I=29            SW098
F    01BF   11BB                DC   FAULTY+#1000     I=30            SW110
F    01C0   611C                DC   BR03+#6000       I=31            SW111
F    01C1   B1BB                DC   FAULTY +#B0O0    I=32            SW117
                     *
                     * SPECIAL TOWAY TABLES USED BY TOWAY DURING SWITCH PROCESSING ET AL
                     *
                     *TABLE          CONSTANT        SWITCH,I, MEANING
F    01C2   03B2   LOBIT0       DC   TMK2            16      0       SELECTED EM
F    01C3   026B                DC   FIRE4           17      1       SELECTED FUAN CHARS
F    01C4   0267                DC   FIRE2           18      2               SELECTED FU
F    01C5   024D                DC   NORM            19-20   3               NOT TEST MESSAGE
F    01C6   0248                DC   MAIN            30      4               NOT SIM TEST
F    01C7   02F9                DC   TR5             31      5               NOT ALTITUDE
```

Table 5-36. AP Program Listing-Continued

```
F   01C8  02EC          DC  TR4          32  6   NOT AN (TRACKS)
F   01C9                DS  1            33  7   **** NOT USED
F   01CA  0273          DC  FIRE7        34  8   NOT PAIRING LINE
F   01CB  02E7          DC  TR2A         35  9   NOT THREAT TEST
F   01CC  02FD          DC  TR5A         36  10  NOT SPEED TEST
F   01CD  0248          DC  MAIN         37  11  NOT JAM STROBE
F   01CE  0248          DC  MAIN         38  12  NOT SAFE CORRIDOR
F   01CF  0248          DC  MAIN         39  13  NOT ALL FIXED POINTS
F   01D0                DC  16           82  14  COMP VIDEO OFF
F   01D1  013F          DC  ROCENT       24  15  RDR ONLY-CENTER SWEEP
F   01D2  03B2  LOBIT1   DC  TMK2         16  0   SELECTED EM
F   01D3  026B          DC  FIRE4        17  1   SELECTED FUAN  CHARS
F   01D4  0267          DC  FIRE2        18  2   SELECTED FU
F   01D5  0250          DC  TST          19  3   TEST MSG ENABLE
F   0106  02D8          DC  TR1          30  4   SIM TEST ENABLE
F   01D7  0248          DC  MAINS        31  5   ALT TEST ENABLE
F   01D8  02EB          DC  TR3          32  6   AN (TRACK) ENABLE
F   01D9                DC  1            33  7   ******************UNUSED
F   01DA  0275          DC  FIRE8        34  8   PAIRING LINE ENABLE
F   01DB  0248          DC  MAIN         35  9   TTHREAT TEST ENABLE
F   01DC  0248          DC  MAIN         36  10  SPEED TEST ENABLE
F   01DD  0389          DC  JAMO         37  11  JAM SAFE CORRIDORENABLE
F   01DF  0369          DC  FIX1         39  13  ALL FIXED PTSENABLE
F   01E0  0000          DC  0            82  14  COMP  VIDOO ON
F   01E1  013A          DC  ROOFF        24  15  RDR ONLY-OFFSET SWEEP
                * ALGTAB SWITCH SUBSCRIBERS—BY INDEX NUMBER (X)&FUNCTION
                * INDEX         SWITCHES
                * (0)           27-39,66-70,72-74,81,82,89-97,111-116      INIT OFF
                * (1)             83-86,88                                 INIT LOWER ON
                * (2)           87-20                                      INIT UPPER ON
                * (3)           16-18,80                                   INIT BOTH OFF
                * (4)           25,(75-79),(98-109),(64)                   ALWAYS OFF
                * (5)           21,26,65                                   INIT BOTH OFF
                * (6)           1-15                                       INIT BOTH OFF
                * (7)           22-23,19,24                                INIT UPPER ON
F   01E2  CCOO  ALGTAB   DC  #CCO0        (0) 2   STATE SINGLE LEGEND
F   01E3  9951          DC  #9951        (1) 2   STATE SPLIT (INIT LOWER)
F   01E4  79A2          DC  #79A2        (2) 3   STATE SPLIT NEVER OFF
F   01E5  9200          DC  #9200        (3) 3   STATE SPLIT WITH OFF
F   01E6  0000          DC  #0000        (4) BACKGROUND ONLY
F   01E7  9C00          DC  #9C00        (5) 4   STATE SPLIT LEGEND
F   01E8  B200          DC  #B200        (6) 3   STATE INCL OFF
F   01E9  66A2          DC  #66A2        (7) 2   STATE SPLIT (INIT UPPER)
F   01EA                END

    0151  AGHIN
F   0031  ALB
F   00F9  ALGOFF
F   01E2  ALGTAB
F   003D  ALTSEL
    025D  ARO
```

Table 5-36. AP Program Listing-Continued

F	OOFC	ATIME
F	0032	AUB
	0099	BIT16
	01A3	BITDBL
	01A4	BITDBM
	01A6	BITDBN
	01A9	BITDBO
	0013	BLANK
	0010	BLANK1
	000D	BLANK2
	0290	BLINK
F	001E	BLINKR
	00D2	BR01
	0121	BR02
	011C	BR03
	017D	CBOUT
	034E	CC1
	035C	CC2
	0349	CCON
	03C7	CMAP
F	0046	CMPSEL
F	0048	CNTRL
F	0036	CON01
F	0035	CON02
F	0034	CON03
F	0033	CON04
F	0032	CON05
F	0031	CON06
F	0030	CON07
F	002F	CON08
F	002E	CON09
F	002D	CON10
F	002C	CON11
F	002E	CON12
	03D6	CONCK
F	002B	CONCON
F	0017	CONMSK
	0070	CONSW1
	0018	CONSW2
	01B1	CONSW6
	01B6	CONSW7
	00A5	CONSW8
	012B	CONV
	033B	CONVRT
	03CA	COP
	03C9	COPY
	0055	CPUCON
	03DA	CSCALE
	009E	DIFGEN
	01EC	DOIT
	03FA	DOULPT
F	OOFF	ELBL

Table 5-36. AP Program Listing-Continued

	0020	EOF
	0023	EOF1
F	0001	ERROR
F	0039	FANSEL
	01C2	FAULT
	01BB	FAULTY
	0278	FI1
	0285	FI3
	0289	FI4
	028A	FI4A
	028C	FI5
F	0000	FILE
	0264	FIRE
	0265	FIRE1
	0267	FIRE2
	0269	FIRE3
	026B	FIRE4
	026D	FIRE5
	026E	FIRE6
	0273	FIRE7
	0275	FIRE8
F	003A	FIRSEL
	0366	FIX
	0369	FIX1
	036F	FIX2
F	0045	FIXSEL
F	004F	FLAG
	004E	FLOOD
	0216	FNY5Z
	0122	FSTK
F	0038	GARB
	0373	GEO
	0376	GEO1
	0383	GEO2
F	0019	GEOMSK
	0260	H2H
	0362	HOOK
F	00F3	I14
F	00F4	I16
F	00F5	I31
F	00F6	I32
F	0180	IFILE
F	0037	INDXWC
	0388	JAM
	0389	JAMO
	03AB	JAM1
F	0043	JAMSEL
	010F	KBD1
F	00F8	LBTDEL
	0167	LDCON
	01C5	LENT
	0082	LIGHTS

Table 5-36. AP Program Listing-Continued

F	01C2	L0BIT0
F	01D2	L0BIT1
F	0004	L0CX
F	0003	L0CY
	023E	L0FF
	023A	L0N
	0249	MA0
	024B	MA1
	0257	MA2
	0248	MAIN
F	01A1	MANADD
	0299	MAP
	029B	MAP0
	02A0	MAP1
	02A5	lMAP3
	02A6	MAP4
	02AF	MAP6
	02B0	MAP7
	02C5	MAP8
	02CB	MAP9
F	001C	MAPMSK
F	00F7	MGICL0
F	0008	MSG
F	0080	MTAB
F	0090	MTAB1
	024D	N0RM
	0198	NRDR0
	0147	NRM0F
F	00F0	NRM0F1
	01DE	0UTPUT
F	0040	PARSEL
F	0014	PHS
	0362	P0INT
F	0022	P0T
	0141	PUT0FF
	0000	PWR0N
F	0025	RANGE
F	0049	RDR0
	01F4	RECV1
	01F5	RECV2
F	0000	RET
F	0007	RET2
F	00FA	RETADD
	022C	RGSTR4
	0195	RNGPUT
	013F	R0CENT
F	0047	R0NR0
F	00F1	R00F
	013A	R00FF
F	00FD	R0TST
	01F2	RS
	01E9	RSHIF1

Table 5-36. AP Program Listing-Continued

	01E8	RSHIFT
	019D	RUBRNG
	02D4	SAFE
F	0044	SAFSEL
	00DF	SAVE
	00DA	SAVST
	03E9	SCA
	03E2	SCAL
	03E0	SCALE
	03F2	SH0
	03F1	SH1
	03ED	SH2
	03EB	SH3
	0342	SHFR
	01EF	SHIFT
F	00A0	SHTAB
F	003C	SIMTST
F	0005	SP1
F	0010	SP2
F	0006	SP3
F	0011	SP4
F	0002	SP8
F	0052	SP8S
F	0012	SP9
F	0042	SPDSEL
F	0013	SPIN
	00C9	SPINBK
	020E	SRCF1
	0214	SRCF2
	0205	SRCFIX
F	0028	SRCMTR
	003F	SRCRET
	00BC	STAT1
	00C2	STAT2
	00B6	STATFX
F	000F	STATUS
	0096	SUB1
	0079	SUBLUP
	00E1	SW001
	00E4	SW001A
	00EA	SW001B
	0031	SW013
	0032	SW013A
	021C	SW016
	00EE	SW019
	021D	SW019B
	00ED	SW020
	00F3	SW021
	0109	SW022
	00F6	SW024
	00FA	SW026
	00FE	SW027

Table 5-36. AP Program Listing-Continued

	021E	SW030
	021F	SW031
	0220	SW037
	011A	SW081
	0221	SW082
F	0026	SWFUIN
	0061	SWPIK
F	00F2	TABL2
	01F7	TALK
F	003E	TANSEL
F	0019	TCDTAB
F	000B	TEMP
F	000B	TEMP1
F	000C	TEMP2
F	004A	TEM_PJS
F	000D	TEMPX
F	000E	TEMPY
F	0038	TEST
F	0050	TEST1
F	0051	TEST2
F	0021	THREAT
	0044	THRET
F	0041	THRSEL
	001B	TIME
	03BB	TMK
	03C0	TMK0
	03B0	TP4K1
	03B2	TMK2
	03B3	TMK3
	03C5	TMK4
	03AF	TMKR
F	0027	TMPWC
F	0029	TMPWC1
F	002A	TMPWC2
F	0038	TMRSEL
	0222	T0WAY1
	0208	TR1
	031B	TR10
	0321	TR11
	02E5	TR2
	02E7	TR2A
	02EB	TR3
	02EC	TR4
	02F9	TR5
	02FD	TR5A
	0300	TR6
	0304	TR7
	0315	TR9
	0205	TRACK
	032A	TRB1
	0327	TRBLNK
F	0014	TRDTAB

Table 5-36. AP Program Listing-Continued

F	0020	TRTTG
F	001F	TRVEC
	01F9	TRYCMD
F	000C	TSP10
F	000D	TSP11
F	000E	TSP12
F	0008	TSP2
F	0009	TSP3
F	000A	TSP4
F	0007	TSP5
	0250	TST
	035E	TSTMSG
F	0023	TTG
	0138	VARS
	01FF	VARS1
	015B	VARS2
	0332	VECT1
	0337	VECT2
	032E	VECTOR
F	002F	VLB
F	0030	VUB
	0lEE	WHODAT
F	0024	WINDOW
F	0009	X
F	00A5	X0
F	00A6	X1
F	00B1	X10
F	00EE	X0100
F	00C3	X1110
F	00B2	X12
F	00B3	X13
F	00B4	X14
F	00B5	X15
F	00B6	X19
F	00B8	X1F
F	00C4	X1F88
F	00A7	X2
F	00B7	X20
F	00EF	X200
F	00C6	X200D
F	00C5	X2035
F	00C7	X2B2B
F	00A8	X3
F	00A4	X30
F	00BA	X33
F	00BB	X3F
F	00A9	X4
F	00EC	X40
F	00C0	X400
F	00C8	X4000
F	00C9	X4002
F	00AA	X5

Table 5-36. AP Program Listing-Continued

F	00CA	X5550
F	00AB	X6
F	00BC	X6F
F	00AC	X7
F	00BD	X74
F	00BE	X7F
F	00CB	X7F00
F	00C1	X7FF
F	00CC	X7FF0
F	00CD	X7FFF
F	00AD	X8
F	00ED	X80
F	00CE	X8000
F	00CF	X800E
F	00D0	X8102
F	00D1	X8181
F	00D2	X8302
F	00D3	X8402
F	00D4	X8602
F	00D5	X8802
F	00D6	X8E02
F	00AE	X9
F	00D7	XAA02
F	00D8	XA00A
F	00AF	XC
F	00D9	XC000
F	00B9	XD9
F	00DA	XDFFF
F	00B0	XF
F	00DB	XPD7FF
F	00BF	XFF
F	00DC	XFF00
F	00DD	XFF0F
F	00DE	XFF7F
F	00DF	XFFBF
F	00E0	XFFC00
F	00E1	XFFCF
F	00E2	XFFDF
F	00E3	XFFEF
F	00C2	XFFF
F	00E4	XFFF0
F	00E5	XFFF3
F	00E6	XFFF8
F	00E7	XFFFB
F	00E8	XFFFC
F	00E9	XFFFD
F	00EA	XFFFE
F	00EB	XFFFF
F	0034	X0FF
F	000A	Y

Table 5-37. DC Program Listing

```
0000    30A3          CFA   VMSB          INITIALIZE
0001    200B          STA   VIDEO         VIDEO
0002    05EO          RSW   S5,S6,S7,S8   RESET SWITCHES
0003    793E          CCB   CENTER        BRANCH
                      *
0004    0600  MAIN     RSW   S9            RESET SWITCH 9
0005    5840  MA1      TXS   S6            INPUT READY?
0006    7D31          BST   INPUT         BRANCH IF NOT
0007    1580          CBO   HIS           HI-SPEED INTO OPERAND
0008    OAOO0         TSS   S9            NEW MESSAGE
0009    780D          CCB   MA4           BRANCH IF SO
000A    5880          TXS   S7            RADAR READY?
000B    7D62          BST   RADAR         BRANCH IF SO
000C    7805          CCB   MA1           BRANCH IF NOT -1
000D    240E  MA4      STO   MSG           SAVE MSG WORD
000E    41B5          AND   XF,O          KEEP 4 LSB'S
000F    OCO           CBI   ACC           ACCUMULATOR INTO INDEX
0010    061F          RSW   S0,S1,S2,S3,  RESET SENSE SWITCHES
                            S4,S9
0011    6280          CFB   MTAB,I        INDEXED BRANCH TO ROUTINE

                            ** AUX READ OUT MESSAGE

0012    41BB  ARO     AND   X7F,O             ISOLATE
0013    5C93          SHF   AR,AS,4           LINE NO.
0014    OCO           CBI   ACC       PUT IN INDEX
0015    3697          CFO   LINY,I    GET Y
0016    2402          STO   Y         STORE IT
0017    3496          CFO   LINX      GET X
0018    2401          STO   X         STORE IT
0019    7D29          BST   D1        START DEFLECTION
001A    6CB7          CFI   X1F       SET INDEX=31
001B    7833          CCB   AR4       BRANCH
001C    5880  AR1      TXS   S7T2      RADAR READY?
001D    7832          CCB   AR3       DO RADAR THING
001E    3C15  AR2      CFH   VTAB+6    VIDEO WORD TO HI-SPEED
001F    2A40          CCL   VNAB      VIDEO ENABLE
0020    3401          CFO   X         COPY X
0021    51B8          ADD   X24,0     INCREMENT IT
0022    2001          STA   X         SAVE IT AGAIN
0023    1580          CBO   HIS       HI-SPEED INTO OPERAND
0024    lC80          CBH   OPR       CHAR TO HI-SPEED
0025    5811          TXH   S4        HAIIG TIL END OF CHAR
0026    2B00          CCL   SOC       START CHAR
0027    3CD5          CFH   XTAB      TAB TO HI-SPEED
0028    2802          CCL   TABNAB    TAB ENABLE
0029    5CC7          SHF   OL,AS,8   SHIFT CHAR
002A    lC80          CBH   OPR       CHAR TO HI-SPEED
002B    5811          TXH   S4        HANG TIL END OF CHAR
002C    2B00          CCL   SOC       START CHAR
```

Table 5-37. DC Program Listing-Continued

```
002D  3CD5        CFH   XTAB          TAB TO HIGH SPEED
002E  2802        CCL   TABNAB        TAB ENABLE
002F  7400        DIS                 DECREMENT INDEX
0030  781C        OCB   AR1           BRANCH IF NOT -1
0031  7804        CCB   MAIN          RETURN
0032  7D62  AR3   BST   RADAR         DO RADAR THING
0033  5821  AR4   TXH   S5            HANG TIL DEFL FINISHED
0034  5003        SHF   4             TIME
0035  781E        CCB   AR2           BRANCH
                  *
                                      ** FIRE UNIT MESSAGE
0036  2COA  FIRE  STH   TEMP          SAVE 2ND WORD
0037  7D27        BST   DEFL          START DEFLECTION
0038  340A        CFO   TEMP          COPY 2ND WORD
0039  41B9        AND   X3F,O         ZERO UNUSED BITS
003A  5C93        SHF   AR,AS,4       SHIFT RIGHT 4
003B  OCO0        CBI   ACC           ACCUM TO INDEX
003C  6290        CFB   FTAB1,I       INDEXED BRANCH
                  *** FTAB1 - F11,F17,F13,F13
003D  5821  F11   TXH   S5            HANG TIL DEFL FINISHED
003E  0008        SSW   S3            SET SWITCH 3
003F  7841        CCB   F12           BRANCH
0040  7D43  F19   BST   DXDY          FIND DX,DY, AND LENGTH
0041  3C10  F12   CFH   VTAB+1        VIDEO TO HI-SPEED
0042  340A        CFO   TEMP          GET 2ND WORD
0043  4DC9        ESB   XFFE7,0       DISPLAY CHAR?
0044  0010        SSW   S4            SET SWITCH 4 IF NOT
0045  78A2        CCB   TR1+1         GO TO TRAK ROUTINE
0046  3011  F13   CFA   VTAB+2        COPY VIDEO WORD
0047  4DCA        ESB   XFFFD,O       DASH LINE 1?
0048  784A        CCB   FI5           BRANCH IF NOT
0049  48B3  F14   ORI   X200,A        SET DASH BIT
004C  200B  F15   STA   VIDEO         SAVE VIDEO WORD
004B  2C06        STH   TX            SAVE END X
004C  2C07        STH   TY            SAVE END Y
004D  6292        CFB   FTAB2,I       INDEXED BRANCH
                  *** FTAB2 - F13,F13,F19,F16
004E  7D43  F16   BST   DXDY          FIND DX,DY, & LENGTH
0041  3COB        CFH   VIDEO         VIDEO TO HI-SPEED
0050  2A40        CCL   VNAB          VIDEO ENABLE
0051  3C03        CFH   DX            DX TO HI-SPEED
0052  2805        CCL   DXNAB         DX-ENABLE
0053  3C04        CFH   DY            DY TO HI-SPEED
0054  2804        CCL   DYNAB         DY-ENABLE
0055  3C05        CFH   LEN           LENGTH TO HI-SPEED
0056  2803        CCL   LNAB          LENGTH ENABLE
0057  0000        NOP
0058  2806        CCL   SOL           START LINE
0059  7D29        BST   D1            START DEFL
005A  3011  F17   CFA   VTAB+2        COPY VIDEO WORD
005B  340A        CFO   TEMP          GET 2ND WORD
005C  6CA8        CFI   X2            SET INDEX-2
005D  4DE1        ESB   XFFFE,O       DASH LINE 2?
005E  784A        CCB   F15           BRANCH IF NOT
005F  7849        CCB   F14           BRANCH
                  *
                                      ** MAP MESSAGE
0060  3012  MAP   CFA   VTAB+3        VIDEO WORD INTO ACCUM
```

Table 5-37. DC Program Listing-Continued

```
0061  4DC7        ESB  XFFDF,O   EXAMINE MAP BIT
0062  3013        CFA  VTAB+4    VIDEO INTO ACCUM IF MAP 2
0063  4DC8        ESB  XFFEF,O   DASH MAP?
0064  7866        CCB  *+2       BRANCH IF NOT
0065  48BE        ORI  X200,A    SET DASH BIT IF SO
0066  200B  MAP0  STA  VIDEO     SAVE VIDEO WORD
0067  7D27        BST  DEFL      START DEFLECTION
0068  3C00B       CFH  VIDEO     VIDEO TO HI-SPEED
0069  2A40        CCL  VNAB      VIDEO ENABLE
006A  5840  MAP1  TXS  S6        INPUT READY?
006B  7D36        BST  IN1       BRANCH IF NOT
006C  1580        CBO  HIS       READ WORD
006D  0A00        TSS  S9        SWITCH 9 SET?
006E  780D        CCB  MA4       BRANCH IF SO
006F  2406        STO  TX        SAVE X
0070  2C07        STH  TY        SAVE Y
0071  7D43        BST  DXDY      FIND DX,DY, & LENGTH
0072  3C03  MAP2  CFH  DX        DX TO HI-SPEED
0073  5811        TXH  S4        HAND IF BUSY PAINTING
0074  2805        CCL  DXNAB     DX-ENABLE
0075  3C04        CFH  DY        DY TO HI-SPEED
0076  2804        CCL  DYNAB     DY-ENABLE
0077  3C05        CFH  LEN       LENGTH TO HI-SPEED
0078  2803        CCL  LNAB      LENGTH ENABLE
0079  3006        CFA  TX        COPY END X
007A  2806        CCL  SOL       START LINE
007B  2001        STA  X               SAVE AS BEGIN X
007C  3007        CFA  TY        COPY END Y
007D  2002        STA  Y               SAVE AS BEGIN Y
007E  5880        TXS  S7        RADAR READY
007F  7D62        BST  RADAR     BRANCH IF SO
0080  786A        CCB  MAP1      RETURN FOR NEXT LINE
                  *
                               ** SAFE CORRIDOR MESSAGE
0081  3014  SAFE  CFA  VTAB+5    GET VIDEO WORD
0082  4DC8        ESB  XFFEF,O   EXAMINE DASH LINE
0083  7885        CCB  SA1       BRANCH IF NOT SET
0084  48BE        ORI  X200,A    SET DASH BIT
0085  200B  SA1   STA  VIDEO     SAVE VIDEO WORD
0086  7D27        BST  DEFL      START DEFLECTION
0087  2C06        STH  TX        SAVE END X
0088  2C07        STH  TY        SAVE EFND Y
0089  7D43        BST  DXDY      FIND DY,DY, & LENGTH
008A  3COB        CFH  VIDEO     SEND VIDEO WORD
008B  2A40        CCL  VNAB      VIDEO ENABLE
008C  3COE        CFH  MSG       SYMBOL TO HI-SPEED
008D  2B00        CCL  SOC       START SYMBOL
008E  7872        CCB  MAP2      BRANCH TO MAP ROUTINE
                  *
                               ** TRACK MESSAGE
008F  4DC7  TRAK  ESB  XFFDF,O   DISPLAY CHAR?
0090  0010        SSW  S4        SET SWITCH 4 IF NOT
0091  300F        CFA  VTAB      COPY VIDEO WORD
0092  200B        STA  VIDEO     SAVE IT
0093  4DC8        ESB  XFFEF,O   DISPLAY VECTOR?
0094  78FB        CCB  P02       BRANCH IF NOT
0095  2C06        STH  TX        SAVE X (TEMPORARY)
0096  2C07        STH  TY        SAVE Y (TEMPORARY)
```

Table 5-37. DC Program Listing-Continued

```
0097    2C01          STH   X          STORE HI-SPEED
0098    2C02          STH   Y          STORE HI-SPEED
0099    3C01          CFH   X          X TO HI-SPEED
009A    5811          TXH   S4         HAND IF BUSY PAINTING
009B    2809          CCL   BXNAB      X-ENABLE (BOOST)
009C    3C02          CFH   Y          Y TO HI-SPEED
009D    2808          CCL   BYNAB      Y-ENABLE (BOOST)
009E    5880          TXS   S7         RADAR READY?
009F    7D62          BST   RADAR      BRANCH IF SO
00AG    7D43          BST   DXDY       FIND DX,DY, & LENGTH
00A1    3COB  TR1     CFH   VIDEO      VIDEO WORD TO HI-SPEEJ
00A2    2A40          CCL   VNAB       VIDEO ENABLE
00A3    3COE          CFH   MSG        CHAR TO HI-SPEED
00A4    2BOO          CCL   SOC        START CHAR
00A3    3401  CHAR    CFO   X          X INTO OPERAND
00A6    64BA          MCS   X66        WILL A/N BE OFF SCREEN?
00A7    0810          TSS   S4         NO, IS SWITCH 4 SET?
00A8    78BA          CCB   TR2        YES - DON'T PAINT THEM
00A9    3CCB          CFH   CTAB       TAB TO HIGH SPEED
00AA    2802          CCL   TABNAB     TAB ENABLE
00AB    6CA9          CFI   X4         SET INDEX
00AC    1580  CH1     CBO   HIS        COPY TWO CHAR
00AD    1C80          CBH   OPR        CHAR TO HI-SPEED
00AE    5811          TXH   S4         HANG TIL END OF CHAR
00AF    2BOO          CCL   SOC        START CHAR
00B0    3ECC          CFH   CTAB1,I    TAB TO HIGH SPEED
00B1    2802          CCL   TABNAB     TAB ENABLE
00B2    5CC7          SHF   OL,AS,8    SHIFT CHAR
00OB3   1C80          CBH   OPR        CHAR TO HI-SPEED
00B4    5811          TXH   S4         HANG TIL END OF CHAR
00B5    2B00          CCL   SOC        START CHAR
006     3ED1          CFH   CTAB2,I    TAB TO HIGH SPEED
00B7    2802          CCL   TABNAB     TAB ENABLE
00B8    7400          DIS              DECREMENT INDEX
00B9    78AC          CCB   CH1        BRANCH IF NOT -1
00BA    0808  TR2     TSS   S3         SWITCH 3 SET?
00BB    7804          CCB   MAIN       BRANCH IF SO
00BC    3C05          CFH   LEN        LENGTH TO HI-SPEED
00BD    5811          TXH   S4         HANG TIL END OF CHAR
00BE    2803          CCL   LNAB       LENGTH ENABLE
00BF    3C03          CFH   DX         DX TO HI-SPEED
00CO    2805          CCL   DXNAB      DX-ENABLE
00C1    3C04          CFH   DY         DY TO HI-SPEEI)
00C2    2804          CCL   DYNAB      DY-ENABLE
00C3    3COB          CFH   VIDEO      VIDEO WORD TO HI-SPEED
00C4    2A40          CCL   VNAB       VIDEO ENABLE
00C5    0000          NOP
00C6    2806          CCL   SOL        START LINE
00C7    7804          CCB   MAIN       RETURN
                *
                              ** CONSOLE CONTROL MESSAGE
00C8    5880  CCON    TXS   S7         RADAR READY?
00C9    7D62          BST   RADAR      BRANCH IF SO
00CA    6CA7          CFI   X1         SET INDEX
00CB    1180  CC1     CBA   HIS        HI-SPEED INTO ACCUM
00CC    4CC5          ESB   XFT7FF     BIT 11 SET?
00CD    44BF          ORX   X7FF,A     FLIP BITS 0-10 IF NOT
00CE    48C4          ORI   XCOOO,A    SET BITS 14-15
```

Table 5-37. DC Program Listing-Continued

```
00CF  2208        STA   RY,1          STORE X OR Y
00D0  7400        DIS                       DECREMENT INDEX
00D1  78CB        CCB   CC1           BRANCH IF NO -1
00D2  1580        CBO   HIS           GET RATE/RANGE WORD
00D3  41B0        AND   X3,0          SAVE 2 LSB'S
00D4  0C00        CBI   AOC           PUT IN INDEX
00D5  41C3        AND   X7FFF,O       ZERO MSB
00D6  5C92        SHF   AR,AS,3       SHIFT ACCUM RIGHT 3 PLACES
00D7  4A9F        ORI   RANGE,I,A     COMBINE RATE & RANGE
00D8  7DD8        BST   PATCH3
001)9 2807        CCL   RNAB          ENABLE RATE/RANGE
00DA  5880        TXS   S7            RADAR READY?
00DB  7D62        BST   RADAR         BRANCH IF SO
00DC  36A3        CFO   VMSB,I        PUT VIDEO MSG'S IN OPERAND
00DD  6CAA        CFI   X8            SET INDEX - 8
00DE  4BA7  CC2   ORI   VLSB,I,O      ADD LSB'S TO VIDEO WORD
00DF  220F        STA   VTAB,I        STORE IT
00EO  34A6        CFO   VMSB+3
00E1  7400        DIS                 DECREMENT INDEX
00E2  78DE        CCB   CC2           BRANCH IF NOT -1
00E3  30DF        CFA   XFFFF               GET NUMBER TO
00E4  200D        STA   TIME                RESET COUNTER
00E5  04C0        RSW   S6,S7         RESET SWITCHES
00E6  0820        TSS   S5                  CHECK FOR
00E7  0080        ESW   S7                  SWEEP
00E8  0020        SSW   S5                  LOST
00E9  30EA        CFA   XFCOO
00EA  2001        Y
00EC  2018        STA   RADAR SWITCH TURN RADAR ON
00ED  793E        CCB   CENTER      BRANCH
                  *
                        ** HOOK MARKER MESSAGE
00EE  3416  HOOK  CFO   VTAB+7      GET VIDEO WORD
00EF  240B        STO   VIDEO       SAVE IT
00F0  2C01        STH   X           GET X
00F1  1180        CBA   HIS         GET Y
00F2  40C3        AND   X7FFF,A     ZERO MSB
00F3  2002        STA   Y           SAVE IT
00F4  7D29        BST   D1          START DEFLECTION
00F5  0010        SSW   S4          SET SWITCH 4
00F6  78FC        CCB   PO3         BRANCH TO POINT ROUTINE
                  *
                        ** TRACK MARKER MESSAGE
00F7  4DC8  TMKR  ESB   XFFEF,O     DISPLAY CHARACTERS?
                  *
                        ** POINTER MESSAGE
00F8  0010  POINT SSW   S4          SET SWITCH IF NOT
                  *
                        ** FIXED POINT MESSAGE
00F9  3414  FIX   CFO   VTAB+5      GET VIDEO WORD
00FA  240B  PO1   STO   VIDEO       STORE VIDEO WORLD
00FB  7D27  PO2   BST   DEFL        START DEFLECTION
00FC  5821  PO3   TXH   S5          HANG TIL DEFL FINISHED
00FD  5C08        SHF   9           TIME
00FE  0008        SSW   S3          SET SWITCH 3
00FF  78A1        CCB   TR1         BRANCH TO TRAK ROUTINE
```

Table 5-37. DC Program Listing-Continued

```
                                                ** GEOREF MESSAGE
0100    2COA    GE0     STH     TEMP            SAVE 2ND WORD
0101    7D27            BST     DEFL            START DEFLECTION
0102    3012            CFA     VTAB+3          GET VIDEO WORD
0103    340E            CFO     MSG             COPY MSG WORD
0104    4DZ7            ESB     XFFDF,O         EXAMINE MAP BIT
0105    3013            CFA     VTAB+4          GET VIDEO IF MAP 2
0106    200B            STA     VIDEO           SAVE IT
0107    3COB            CFH     VIDEO           VIDEO WORD TO HI-SPEED
0108    2A40            CCL     VNAB            VIDEO ENABLE
0109    5821    GE1     TXH     S5              HANG TIL DEFL FINISHED
010A    5C06            SHF     7               TIME
010B    300A            CFA     TEMP            COPY CHARS
010C    3COE            CFH     MSG             SYMBOL TO HI-SPEED
010D    3401            CFO     X               COPY X
010E    64B8            MCS     X24             WILL A/N BE OFF SCREEN?
010F    7911            CCB     *+2             BRANCH IF NOT
0110    791C            CCB     GE2             BRANCH IF SO
0111    2B00            CCL     SOC             START SYMBOL
0112    3CD6            CFH     GEOTAB          TAB TO HIGH SPEED
0113    2802            CCL     TABNAB          TAB ENABLE
0114    1C00            CBH     ACC             CHAR TO HI-SPEED
0115    5CA7            SHF     AL,AS,8         SHIFT CHAR
0116    5811            TXH     S4              HANG TIL END OF CHAR
0117    2BOO            CCL     SOC             START CHAR
0118    3CD5            CFH     XTAB            TAB TO HIGH SPEED
0119    2802            CCL     TABNAB          TAB ENABLE
011A    1CO0            CBH     ACC             CHAR TO HI-SPEED
011B    5811            TXH     S4              HANG TIL END OF CHAR
011C    2B00    GE2     CCL     SOC             START CHAR
011D    5840            TXS     S6              INPUT READY?
011E    7D31            BST     INPUT           BRANCH IF NOT
011F    1880            CBO     HIS             GET WORD
0120    0A00            TSS     89              SWITCH 9 SET?
0121    780D            CCB     MA4             BRANCH IF SO
0122    240A            STO     TEMP            STORE WORD
0123    7D27            BST     DEFL            START DEFLECTION
0124    7909            CCB     GE1             BRANCH TO GE1
                *
                                                ** CLUTTER MAPPER MESSAGE
0125    3014    CMAP    CFA     VTAB+5          COPY VIDEO WORD
0126    7866            CCB     MAPO            BRANCH TO MAP ROUTINE
                *
                                                ** START DEFLECTION
0127    2001    DEFL    STH     X                       STORE HI-SPEED
0128    2C02            STH     Y                       STORE HI-SPEED
0129    3C01    D1      CFH     X                       X TO HI-SPEED
012A    5811            TXH     S4              HANG IF BUSY PAINTING
012B    2809            CCL     BXNAB           X-ENABLE (BOOST)
012C    3C02            CFH     Y                       Y TO HI-SPEED
012D    2808            CCL     BYNAB           Y-ENABLE (BOOST)
012E    5880            TXS     S7              RADAR READY?
012F    7962            CCB     RADAR           BRANCH IF SO
0130    6000            CFB     RET             RETURN
                *
                                                ** INPUT BUFFER EMPTY
0131    5811    INPUT   TXH     S4              HANG TIL FINISHED PAINTING
0132    3CEA            CFH     XFC00                   CENTER
```

Table 5-37. DC Program Listing-Continued

```
0133  2801          CCL   XNAB          THE
0134  0000          NOP                 CRT
0135  2800          CCL   YNAB          BEAM
0136  5840  IN1     TXS   S6      INPUT READY?
0137  7939          CCB   *+2     BRANCH IF NOT
0138  6000          CFB   RET     RETURN IF SO
0139  5880          TXS   S7      RADAR READY?
013A  7960          CCB   IN2     BRANCH IF SO
013B  680D          DFS   TIME    DECREMENT FILE
013C  7936          CCB   IN1     BRANCH IF NOT -1
013D  0040          SSW   S6      NO INPUT SWITCH
013E  3CEA  CENTER  CFH   XFCOO         RETURN
013F  2801          CCL   XNAB          RADAR
0140  0000  NOP                         TO
0141  2800          CCL   YNAB          CENTER
0142  7804          CCB   MAIN    RETURN
                *
                              ** DELTA X - DELTA Y
0143  040E  DXDY    RSW   S1,S2,S3 RESET SWITCHES
0144  3401          CFO   X               FIND
0145  5506          SUB   TX,O            DX
0146  4CC3          ESB   X7FFF,A EXAMINE SIGN BIT
0147  794B          CCB   DX1     BRANCH IF PLUS
0148  0002          SSW   S1      SET TO REMEMBER DX<O
0149  1020          CBA   ACC,N   DX- -DX
014A  50A7          ADD   X1,A
014B  1400  DX1     CBO   ACC     PUT DX IN OPERAND
014C  3002          CFA   Y                 FIND
014D  5407          SUB   TY,A            DY
014E  4CC3          ESB   X7FFF,A EXAMINE SIGN BIT
014F  7953          CCB   DX2     BRANCH IF PLUS
0150  0004          SSW   S2      SET TO REMEMBER DY<O
0151  1020          CBA   ACC,N   DY--DY
0152  50A7          ADD   X1,A
0153  6CB4  DX2     CFI   XD      SET INDEX
0154  5DEC          NRM           NORMALIZE
0155  5821          TXH   S5      HANG TIL DEFL FINISHED
0156  0804          TSS   S2      IS DY<O
0157  48C4          ORI   XCOOO,A ADD SIGN BITS IF SO
0158  2004          STA   DY      STORE DY
0159  1080          CBA   OPR     PUT DX INTO ACCUM
015A  0802          TSS   S1      IS DX<O
015B  48C4          ORI   XCOOO,A ADD SIGN BITS IF SO
015C  2003          STA   DX      STORE DX
015D  36E1          CFO   LTAB,I  COPY LENGTH
015E  2405          STO   LEN     STORE IT
015F  6000          CFB   RET     RETURN
                *
                * MORE OF INPUT ROUTINE
0160  6800  IN2     DFS   RET     DECREMENT RETURN ADDR
0161  6800          DFS   RET     DECREMENT RETURN ADDR
                *
                              ** RADAR - SWEEP PAINTING
0162  3418  RADAR   CFO   RADAR:SWITCH PAINT RADAR?
0163  4DEC          ESB   X0,O            RETURN IF
0164  6000          CFB   RET             SWITCH = 0
0165  3CO09         CFH   RX      RADAR X TO HI-SPEED
0166  5811          TXH   S4      HANG IF BUSY PAINTING
```

Table 5-37. DC Program Listing-Continued

```
0167  2809          CCL  BXNAB          X ENABLE (BOOST)
0168  3C08          CFH  RY             RADAR Y TO HI-SPEED
0169  2808          CCL  BYNAB          Y ENABLE (BOOST)
016A  1780          CBO  SIN            COPY SIN
016B  1100          CBA  COS            COPY COS
016C  4DC3          ESB  X7FFF,O        DATA VALID?
016D  7971          CCB  RA1            BRANCH IF SO
016E  5002          SHF  3                    TIME
016F  1780          CBO  SIN            COPY SIN
0170  1100          CBA  COS            COPY COS
0171  1C80  RA1     CBH  OPR            SIN TO HI-SPEED
0172  2805          CCL  DXNAB          DELTA-X ENABLE
0173  5821          TXH  S5             HANG TIL DEFL FINISHED
0174  1C00          CBH  ACC            COS TO HI-SPEED
0175  2804          CCL  DYNAB          DELTA-Y ENABLE
0176  3C17          CFH  VTAB+8         VIDEO WORD TO HI-SPEED
0177  2A40          CCL  VNAB           VIDEO ENABLE
0178  5007          SHF  8              TIME
0179  4CEF          ESB  XDFFF,A              START
017A  797C          CCB  *+2                  SWEEP
017B  797E          CCB  RGO                  IF SIN
017C  4DEF          ESB  XDFFF,O              & COS
017D  797F          CCB  RGO+1                ARE OK
017E  2A10  RGO     CCL  SNAB           SWEEP ENABLE
017F  0420          RSW  S5             RESET SWITCH
0180  3C01          CFH  X                    X TO HI-SPEED
0181  34E9          CFO  XE00                 LOAD
0182  2419          STO  COUNT                COUNTER
0183  5810          TXS  S4             C.S. BUSY PAINTING?
0184  7988          CCB  *+4            YES - ADVANCE FOUR SPACES
0185  6819          DFS  COUNT          COUNT
0186  7983          CCB  *-3            GO CHECK AGAIN
0187  798D          CCB  SWLOST         BRANCH IF TERM COUNT
0188  2419          STO  COUNT          RESET COUNTER
0189  5808  RCNT    TXS  S3             ANYBODY BUSY?
018A  7990          CCB  ROK            BRANCH IF NOT
018B  6819          DFS  COUNT          COUNT IF SO
018C  7989          CCB  RCNT           GO TEST AGAIN
018D  1020  SWLOST  CBA  ACC,N                TURN OFF
018E  2018          STA  RADAR:SWITCH         RADAR AND
018F  0080          SSW  S7                   TELL A.P.
0190  2809  ROK     CCL  BXNAB          X-ENABLE (BOOST)
0191  3C02          CFH  Y              Y TO HI-SPEED
0192  2808          CCL  BYNAB          Y-ENABLE (BOOST)
0193  3COB          CFH  VIDEO          OLD VIDEO WORD TO HI-SPEED
0194  2A40          CCL  VNAB           VIDEO ENABLE
0195  6000          CFB  RET            RETURN
                    *
                                 * TEST MESSAGE
0196  34B0  1MSG    CFO  X3             SET UP
0197  240A          STO  TEMP           INDEX
0198  6COA  TEST:MAP CFI  TEMP          LOAD INDEX
0199  36D8          CFO  TMSG:X+1,I           SET UP
019A  2401          STO  X              BEGIN
019B  26DD          CFO  TMSG:Y+1,I     X AND Y
019C  2402          STO  Y              POSITIONS
019D  36D7          CFO  TMSG:X,I             SET UP
019E  2406          STO  TX                   END
```

Table 5-37. DC Program Listing-Continued

```
019F  36DC          CFO   TMSG:Y,I    X AND Y
01A0  2407          STO   TY          POSITIONS
01A1  7D29          BST   D1          START DEFLECTION
01A2  7D43          BST   DXDY        FIND DX,DY, AND LENGTH
01A3  3C03          CFH   DX                SEND
01A4  2805          CCL   DXNAB             ALL
01A5  3C04          CFH   DY                THE
01A6  2804          CCL   DYNAB             GOOD
01A7  3C05          CFH   LEN               STUFF
01A8  2803          CCL   LNAB              OVER
01A9  3C12          CFH   VTAB+3            TO
01AA  2A40          CCL   VNAB              C.S.
01AB  0000          NOP                 TIME
01AC  2806          CCL   SOL           START LINE
01AD  680A          DFS   TEMP          FINISHED?
01AE  7998          CCB   TEST:MAP     KEEP GOING IF NOT
0l1AF 3431          CFO   X7                SET UP
01B0  240A          STO   TEMP              INDEX
01B1  6COA  TEST:ARO CFI  TEMP          LOAD INDEX
01B2  3697          CFO   LINY,I            SEND
01B3  2402          STO   Y                 X & Y
01B4  3496          CFO   LINX              TO
01B5  2401          STO   X                 CENTER
01B6  7D29          BST   D1                SECTION
0187  6CB9          CFI   X3F           SET INDEX
01B8  5880  TLOOP   TXS   S7          RADAR READY?
01B9  7D62          BST   RADAR         BRANCH IF SO
O1BA  5821          TXH   S5          HANG TIL DEFL FINISHED
01BB  7DD6          BST   PATCH1
01BC  2A40          CCL   VNAB          VIDEO ENABLE
01BD  3401          CFO   X                 INCREMENT
01BE  51B6          ADD   X12,0             X FOR
01BF  2001          STA   X                 RADAR
01CO  3CC2          CFH   X2B00         CHAR TO HIGH SPEED
01C1  5C05          SHF   6             TIME
01C2  5811          TXH   S4            HANG TIL END OF CHAR
01C3  2B00          CCL   SOC           START CHAR
01C4  3CD5          CFH   XTAB              TAB TO
01C5  2802          CCL   TABNAB            NEXT POSITION
01C6  7400          DIS                 DECREMENT INDEX
01C7  79B8          CCB   TLOOP         BRANCH IF NOT -1
01C8  680A          DFS   TEMP          DECREMENT INDEX
01C9  79B1          CCB   TEST:ARO      BRANCH IF NOT -1
01CA  3CEA          CFH   XFCOO             CENTER
01CB  5811          TXH   S4                THE
01CC  2809          CCL   BXNAB             BEAM
01CD  0000          NOP                     ON THE
01CE  2808          CCL   BYNAB             CRT
01CF  79E1          CCB   PATCH2
01DO  5COE          SHF   15            TIME
01Di  3CE8          CFH   XFO00             SEND A
01D2  2B00          CCL   SOC               LITTLE CROSS
01D3  7804          CCB   MAIN          RETURN
            *
01D6                SPA   #1D6
01D6  3C15  PATCH1  CFH   VTAB+6        SEND ARO VIDEO
01D7  79BC          CCB   #1BC
01D8  5811  PATCH3  TXH   S4            HANG IF CS BUSY
```

Table 5-37. DC Program Listing-Continued

```
     01D9  1C00            CBH   ACC          PUT ON HSO
     01DA  6000            CFB   RET
     01E1                  SPA   #1E1
     01E1  0000  PATCH2    NOP
     01E2  5821            TXH   S5           HANG TILL DEFL FINISHED
     01E3  79DO            CCB   #1D0
                 *
                                 ****         RAM   FILE   0-127
F    0000                 SFA   *
F    0000        RET      DS    1            RETURN ADDR
F    0001        X        DS    1            X-POSITION
F    0002        Y        DS    1            Y-POSITION
F    0003        DX       DS    1            DELTA X
F    0004        DY       DS    1            DELTA Y
F    0005        LEN      DS    1            LENGTH
F    0006        TX       DS    1            TEMPORARY X
F    0007        TY       DS    1            TEMPORARY Y
F    0008        RY       DS    1            RADAR Y
F    0009        RX       DS    1            RADAR X
F    000OOOA     TEMP     DS    1            TEMPORARY STORAGE
F    000B        VIDEO    DS    1            CURRENT VIDEO WORD
F    000C        RETSA    DS    1            RETURN ADDR SAVE AREA
F    OOOD        TIME     DS    1            COUNTER
F    000E        MSG      DS    1            1ST WORD OF MESSAGE
F    000F        VTAB     DS    9            TABLE OF VIDEO WORDS
F    0018        RADAR:SWITCH DS 1
F    0019        COUNT    DS    1
                 *
                 *
                                 ***          PRO   FILE   12255
F    0080                 SFA   #80
F    0080  0004  MTAB     DC    MAIN,ARO,FIRE,MAP,SAFE,TRAK
F    0081  0012
F    0082  0036
F    0083  0060
F    0084  0081
F    0085  008F
F    0086  00C8           DC    CCON,HOOK,TMSG,POINT,FIX,GEO
F    0087  OOEE
F    0088  0196
F    0089  00F8
F    008A  00F9
F    008B  0100
F    008C  0004           DC    MAIN,TMKR,CMAP,MAIN
F    008D  00F7
F    008E  0125
F    008F  0004
F    0090  003D  FTAB1    DC    FI1,FI7
F    0091  005H
F    0092  0046  FTAB2    DC    F13,F13,F19,F16
F    0093  0046
F    0094  0040
F    0095  004E
F    0096  F9C0  LINX     DC    #F9C0
F    0097  B8D9  LINY     DC    #B8D9,#B8BA,B89B,#B87C,#B83D,#B83E,#B81F,
                                #B800
F    0098  B8BA
F    0099  B898
F    009A  B87C
```

Table 5-37. DC Program Listing-Continued

```
F  009B  B85D
F  009C  B83E
F  009D  B81F
F  009E  B800
F  009F  1000  RANGE   DC    #1000,#4000,#4000,#8000
F  00A0  4000
F  00A1  4000
F  00A2  8000
F  00A3  1C00  VMSB    DC    #1C00,#2C00,#4C00,#8C00
F  00A4  2C00
F  00A5  4C00
F  00A6  8C00
F  00A7        VLSB    EQU   *
F  00A7  0001  X1      DC    1
F  00A8  0002  X2      DC    2
F  00A9  0004  X4      DC    4
F  00AA  0008  X8      DC    8
F  00AB  0010          DC    16,32,64,128,256
F  00AC  0020
F  00AD  0040
F  00AE  0080
F  00AF  0100
F  00B0  0003  X3      DC    3
F  00B1  0007  X7      DC    7
F  00B3  000A  XA      DC    10
F  00B4  000D  XD      DC    #D
F  00B5  000F  XF      DC    15
F  00B6  0012  X12     DC    #12
F  00B7  001F  X1F     DC    #1F
F  00B8  0024  X24     DC    #24
F  00B9  003F  X3F     DC    #3F
F  00BA  0066  X66     DC    #66
F  00BB  007F  X7F     DC    #7F
F  00BC  OOFF  XFF     DC    #FF
F  00BD  01FF  X1FF    DC    #1FF
F  00BE  0200  X200    DC    #200
F  00BF  07FF  X7FF    DC    #7FF
F  00CO  PFFF  XFFF    DC    #FFF
F  00C1  1FFF  X1FFF   DC    #1FFF
F  00C2  2B00  X2B00   DC    #2B00
F  00C3  7FFF  X7FFF   DC    #7FFF
F  00C4  C000  XC000   DC    #C000
F  00C5  C7FF  XF7FF   DC    #F7FF
F  00C6  FFBF  XFFBF   DC    #FFBF
F  00C7  FFDF  XFFDF   DC    #FFDF
F  00C8  FFEF  XFFEF   DC    #FFEF
F  00C9  FFF7  XFFF7   DC    #FFF7
F  00CA  FFFD  XFFFD   DC    #FFFD
F  00CB  1009  CTAB    DC    #1009
F  00CC  061F  CTAB1   DC    #061F
F  00CD  061F          DC    #061F
F  00CE  1F12          DC    #1F12
F  00CF  161F          DC    #161F
F  00D0  161F          DC    #161F
F  00D1  0008  CTAB2   DC    #0008
F  00D2  061F          DC    #061F
F  00D3  061F          DC    #061F
```

Table 5-37. DC Program Listing-Continued

```
F   00D4   161F             DC     #161F
F   00DS   161F   XTAB      DC     #161F
F   00D6   1619   GEOTAB    DC     #1619
F   00D7   F800   TMSG:X    DC     #F800
F   00D8   FFFF             DC     #FFFF
F   001D9  FFFF             DC     #FFFF
F   00DA   F800             DC     #F800
F   00DB   F800             DC     #F800
F   00DC   F800   TMSG:Y    DC     #F800
F   00DD   F800             DC     #F800
F   00DE   FFFF             DC     #FFFF
F   00DF   FFFF   XFFFF     DC     #FFFF
F   00EO   F800             DC     #F800
F   OOE1   LTAB   EQU       *
F   OOE1   FFFE   XFFFE     DC     *FFFE
F   00E2   0FFC             DC     #FFC
F   00E3   0FF8             DC     #FF8
F   00E4   0FFO             DC     #FFO
F   00E5   0FEO             DC     #FEO
F   00E6   0FCO             DC     #FCO
F   00E7   0F80             DC     #F80
F   00E8   0FOO   XFOO      DC     #FOO
F   00E9   0EOO   XEOO      DC     #EOO
F   00EA   FCOO   XFCOO     DC     #FCOO
F   00EB   0800             DC     #800
F   00EC   0000   XO        DC     0
F   00ED   0000             DC     0
F   00EE   0000             DC     0
F   00EF   DFFF   XDFFF     DC     #DFFF
                  *
                  * COPY COMMAND TO LOW SPEED VALUES
F   0000         YNAB      EQU    0          Y ENABLE
F   0001         XANB      EQU    1          X ENABLE
F   0002         TABNAB    EQU    2          TAB ENABLE
F   0003         LNAB      EQU    3          LENGTH ENABLE
F   0004         DYNAB     EQU    4          DELTA Y ENABLE
F   0005         DXNAB     EQU    5          DELTA X ENABLE
F   0006         SOL       EQU    6          START OF LINE
F   0007         RANB      EQU    7          RATE RANGE ENABLE
F   0008         BYNAB     EQU    8          Y ENABLE WITH BOOST
F   0009         BXNAB     EQU    9          X ENABLE WITH BOOST
F   0210         SNAB      EQU    #210       SWEEP ENABLE
F   0240         VNAB      EQU    #240       VIDEO ENABLE
F   0300         SOC       EQU    #300       START OF CHARACTER
F   00FO                   END

    001C   AR1
    001E   AR2
    0032   AR3
    0033   AR4
    0012   ARO
=   0009   BXNAB
=   0008   BYNAB
    00CB   CC1
    00DE   CC2
    00C8   CCON
    013E   CENTER
    00AC   CH1
```

Table 5-37. DC Program Listing-Continued

```
    00A5  CHAR
    0125  CMAP
F   0019  COUNT
F   00CB  CTAB
F   00CC  CTAB1
F   00D1  CTAB2
    0129  D1
    0127  DEFL
F   0003  DX
    014B  DX1
    0153  DX2
    0143  DXDY
=   0005  DXNAB
F   0004  DY
=   0004  DYNAB
    003D  FI1
    0041  FI2
    0046  FI3
    0049  FI4
    004A  FI5
    0043  FI6
    005A  FI7
    0040  FI9
    0036  FIRE
    00OF9 FIX
F   0090  FTAB1
F   0092  FTAB2
    0109  GE1
    011C  GE2
    0100  GE0
F   00D6  GE0TAB
    OOEE  HOOK
    0136  IN1
    0131  INPUT
F   0005  LEN
F   0096  LINX
F   0097  LINY
=   0003  LNAB
F   00E1  LTAB
    0005  MA1
    000D  MA4
    0004  MAIN
    0060  MAP
    0066  MAPO
    006A  MAP1
    0072  MAP2
F   000E  MSG
F   0080  MTAB
    01D6  PATCH1
    01E1  PATCH2
    01D8  PATCH3
    00FA  PO1
    PPFB  P02
    00F0  P03
    00F8  POINT
    0171  RA1
    0162  RADAR
```

Table 5-37. DC Program Listing-Continued

```
F   0018   RADAR:SWITCH
F   009F   RANGE
    0189   RCNT
F   0000   RET
F   000C   RETSA
    017E   RGO
=   0007   RNAB
    0190   ROK
F   0009   RX
F   0008   RY
    0085   SA1
    0081   SAFE
=   0210   SNAB
=   0300   SOC
=   0006   SOL
    018D   SWLOST
=   0002   TABNAB
F   000A   TEMP
    01B1   TEST:ARO
    0198   TEST:MAP
F   000D   TIME
0   1B8    TLOOP
    00F7   TMKR
    0196   TMSG
F   00D7   TMSG:X
F   00DC   TMSG:Y
    00A1   TR1
    00BA   TR2
    0086   TRAK
F   0006   TX
F   0007   TY
F   000B   VIDEO
F   00A7   VLSB
F   00A3   VMSB
=   0240   VNAB
F   000F   VTAB
F   0001   X
F   00EC   X0
F   00A7   X1
F   00B6   X12
F   00OB7  X1F
F   00BD   X1FF
F   00C1   X1FFF
F   00A8   X2
F   00BE   X200
F   00B8   X24
F   00BD   X3
F   00B9   X3F
F   00A9   X4
F   00BA   X66
F   00B1   X7
F   00BB   X7F
F   00BF   X7FF
F   00C3   X7FFF
F   O0AA   X8
F   00B2   X9
F   00B3   XA
```

Table 5-37. DC Program Listing-Continued

```
F   00C4   XCOOO
F   00B4   XD
F   00EF   XDFFF
F   00E9   XEOO
F   00B5   XF
F   00E8   XFOO
F   00C5   XF7FF
F   00EA   XFCOO
F   OOBC   XFF
F   00C6   XFFBF
F   00C7   XFFDF
F   00C8   XFFEF
F   00C0   XFFF
F   00C9   XFFF7
F   00CA   XFFFD
F   00E1   XFFFE
F   00DF   XFFFF
=   0001   XNAB
F   00D5   XTAB
F   0002   Y
=   0000   YNAB
NO ERRORS DETECTED
```

Table 5-38. AP Initialization Program

Label (memory location)	Operation (command hex	Command (binary) 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	Command comment	Storage or constant comment	Functional description
0000	07BF	0 0 0 0 0 0 1 1 1 1 0 1 1 1 1 1 (RSW / ALL BUT SS6)	S0,S1,S2, S3,S4,S5 S7,S8,S9		Reset all set switches except SS6
0001	0040	0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 (SSW / SS6 ONLY)	SS6		Set SS6 for initialize mode.
0002	6CBE	0 1 1 0 1 1 0 0 1 0 1 1 1 1 1 0 (CFI / B / E)	LOAD INDEX	127 IS SWITCH LIMIT	Copy ROM file address 00BE (which contains 007F into index register.
0003	30A5	0 0 1 1 0 0 0 0 1 0 1 0 0 1 0 1 (CFA / A / 5)	LOAD ZEROES		Copy ROM file address 00A5 (which contains 0000) into accumulator.
0004	2200	0 0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 (STA / 0 / 0; INDEX)	STORE EM		Modify file address 0000 by index register 007F. Store accumulator in RAM file address 007F
0005	7400	0 1 1 1 0 1 0 0 0 0 0 0 0 0 0 0 (DIS)	AGAIN?		Decrement index register to 007E
0006	7804	0 1 1 1 1 0 0 0 0 0 0 0 0 1 0 0 (CCB / 0 / 4)	YES - GO BACK TWO SPACES		Command register bits 0-9 are loaded in program address counter. Unconditional branch to memory location 0004.
0004	2200	0 0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 (STA / 0 / 0; INDEX)	STORE EM		Modify file address 0000 by index register 007E. Store accumulator in RAM file address 007E.
0005	7400	0 1 1 1 0 0 1 0 0 0 0 0 0 0 0 0	AGAIN?		Decrement index register to 007D
•	•	•	•		•
•	•	•	•		•
•	•	•	•		•
•	•	•	•		•

Table 5-38. AP Initialization Program - Continued

Label (memory location)	Operation (command hex	Command (binary) 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	Command comment	Storage or constant comment	Functional description
0005	7400	0 1 1 1 0 0 1 0 0 0 0 0 0 0 0 0 DIS	AGAIN?		Decrement index register to 0000
0006	7804	0 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 CCB	YES - GO BACK TWO SPACES		Command register bits 0-9 are loaded into command register. Unconditional branch to memory location 0004.
0004	2200	0 0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 SRA INDEX 0 0	STORE EM		Modify file address 0000 by index register 0000. Store accumulator in RAM file address 0000.
0005	7400	0 1 1 1 0 1 0 0 0 0 0 0 0 0 0 0 DIS	AGAIN?		Since index register is all ZEROES, skip next instruction.
0007	30FI	0 0 1 1 0 0 0 0 1 1 1 1 0 0 0 1 CFA F 1	ASSUME RADAR ONLY MODE	ROOF	Load ROM file address (which contains 013A) into accumulator.
0008	2047	0 0 1 0 0 0 0 0 0 1 0 0 0 1 1 1 STA 4 7		RADAR ONYL OFFSET CONNECTOR	Stores accumulator (which now contains 013A) in RAM file location 0047.
0009	34DB	0 0 1 1 0 1 0 0 1 1 0 1 1 0 1 1 CFO D B	TO INITIATE COMPRESSOR RANGE	CHECK FOR RELOAD OF VIDEO COMPRESSOR	Copies ROM file address 000B (which contains F7FF) into operand.
000A	242E	0 0 1 0 0 1 0 0 0 0 1 0 1 1 1 0 STO 2 E	FOR RADAR ONLY	RANGEOVER,THREAT, COMPRESSOR RANGE	Stores operand (which contains F7FF) in RAM file location 002E.
000B	34FC	0 0 1 1 0 1 0 0 1 1 1 1 1 1 0 0 CFO F C	GET ADDRESS OF TIME	TIME	Copies ROM file address 00FC (which contains 001B) into operand.
000c	2449	0 0 1 0 0 1 0 0 0 1 0 0 1 0 0 1 STO 4 9	STORE IT	RADAR ONLY EOF MAIN CONNECTOR	Stores operand (which contains 001B in RAM file location 0049.

Table 5-38. AP Initialization Program - Continued

Label (memory location)	Operation (command hex	Command (binary) 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	Command comment	Storage or constant comment	Functional description
000D	308D	0 0 1 1 0 0 0 0 1 0 1 1 1 1 0 1 (CFA / B / D)	INITIALIZE		Copies ROM file address 00BD (which contains 0074 into accumulator.
000E	2012	0 0 1 0 0 0 0 0 0 0 0 1 0 0 1 0 (STA / 1 / 2)	UPPER SWIWTCH LIMIT	HOLDS CURRENT SWITCH FEEDBACK CODE	Stores accumulator (which contains 0074) in RAM file location 0012.
000F	7811	0 1 1 1 1 0 0 0 0 0 0 1 0 0 0 1 (CCB / 1 / 1)	ADVANCE TWO SPACES		Command bits 0-9 are loaded into program address counter. This is an unconditional branch to memory location 0011.
0011	30CE	0 0 1 1 0 0 0 0 1 1 0 0 1 1 1 0 (CFA / C / E)	LOAD STATUS REPORT CODE	ACTION CODE = NO SWITCH	Copy ROM file address (which contains 8000) into accumulator.
0012	2006	0 0 1 0 0 0 0 0 0 0 0 0 0 1 1 0 (STA / 0 / 6)	SAVE IT FOR CPU	HOLDS STATUS WORD	Store accumulator (which contains 8000 in RAM file location 0006.
0013	6812	0 1 1 0 1 0 0 0 0 0 0 1 0 0 1 0 (DFS / 1 / 2)	BLANK	HOLDS CURRENT SWITCH FEEDBACK CODE	Decrements RAM file address (which contains 0074) by 1 to 0073 which is stored in accumulator, then writes accumulator contents in file address 0012.
0014	7818	0 1 1 1 1 0 0 0 0 0 0 1 1 0 0 0 (CCB / 1 / 8)	CONSW2		Command bits 0-9 are loaded into program address counter. This is an unconditional branch to memory location 0018.
0018	50A6	0 1 0 1 0 0 0 0 1 0 1 0 0 1 1 0 (ASS / ACC / A / 6)			Contents of ROM file A6 (which contains 00010 is added to accumulator (which is 0073). Result (which is 0074) is stored in accumulator.
0019	2010	0 0 1 0 0 0 0 0 0 0 0 1 0 0 0 0 (SRA / 1 / 0)		HOLDS OLD SWITCH CODE	Content of accumulator (which is 0074) is stored in RAM file location 0010.

Table 5-38. AP Initialization Program - Continued

Label (memory location)	Operation (command hex	Command (binary) 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	Command comment	Storage or constant comment	Functional description
001A	7870	0 1 1 1 1 0 0 0 0 1 1 1 0 0 0 0 (CCB / 7 / 0)	CONSW1		Command bits 0-9 are loaded into program address counter. This is an unconditional branch to memory location 0070.
0079	6007	0 1 1 0 1 1 0 0 0 0 0 0 0 1 1 1 (CFI / 0 / 7)	SUBLUP	RETURN 2	Copy file address 0007 (which contains 00C2) into index register.
007A	32FF	0 0 1 1 0 0 1 0 1 1 1 1 1 1 1 1 (CFA / INDEX / F / F)			The index bit adds ROM file address 00FF to index register 00C2 which results in addressing memory location 00C1. ROM file location 00C1 (which contains 07FF is copied into accumulator.
007B	5023	0 1 0 1 0 0 0 0 0 0 1 0 0 0 1 1 (SHF / ACC LEFT / SHIFT 4)			Accumulator (which contains 07FF) is shifted left four bits and now contains 7FFF.
007C	40B0	0 1 0 0 0 0 0 0 1 0 1 1 0 0 0 0 (AND / ACCUM / B / 0)			Accumulator (which contains 7FFF) is ANDed with ROM file address 00B0 (which contains 000F). Resultant which is 000F is stored in accumulator.
007D	5011	0 1 0 1 0 0 0 0 0 0 0 1 0 0 0 1 (ADD / ACCUM / 1 / 1)	ADD TO SWITCH CODE		Add accumulator (which contains 000F) to RAM file address 0011 (which contains 0074). Resultant (which is 008E) is stored in accumulator.
007E	2011	0 0 2 1 0 0 0 0 0 0 0 1 0 0 0 1 (STA / 1 / 1)	SAVE SWITCH CODE + MANADD		Store accumulator (which contains 008E) in RAM file address 0011.
007f	4cbe	0 1 0 0 1 1 0 0 1 0 1 1 1 1 1 0 (ESB / ACCUM / B / E)	GREATER THAN 127?	127 IS SWITCH LIMIT	Accumulator contents (which contains 008E) are compared with ROM file address 00BE (which is 007F). Since accumulator is greater than 127, program address counter is skipped.

Table 5-38. AP Initialization Program - Continued

Label (memory location)	Operation (command hex	Command (binary) 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	Command comment	Storage or constant comment	Functional description
0081	2026	0 0 1 0 0 0 0 0 0 0 1 0 0 1 1 0 STA 2 6	SWFUIN - STORE FOR LATER	SWITCH FUNCTION INDEX - SWITCH PROC.	Accumulator content (which is 008E) is stored in RAM file location 0026.
0070	3410	0 0 1 1 0 1 0 0 0 0 0 1 0 0 0 0 CFO 1 0	PICK UP SWITCH CODE	HOLD OLD SWITCH CODE	Content of RAM file address 0010 (which is 0074) is copied into operand.
0071	30F4	0 0 1 1 0 0 0 0 1 1 1 1 0 1 0 0 CFA F 4	ASSUME NOT OVER 64	16 + MANADD - EBL	Copies ROM file address 00F4 (which contains-00B2) into accumulator.
0072	64EC	0 1 1 0 0 1 0 0 1 1 1 0 1 1 0 0 MCS E C	IS IT OVER 64?		Absolute magnitude comparison between operand (which is 0074) with contents of ROM file address 00EC (which is 0040). Value of operand is greater than file, therefore there is no skip.
0073	30F6	0 0 1 1 0 0 0 0 1 1 1 1 0 1 1 0 CFA F 6	YES - FIX IT	32 + MANADD - ELBL	Copies ROM file address F6 (which contains 00C2) into accumulator.
0074	2007	0 0 1 0 0 0 0 0 0 0 0 0 0 1 1 1 STA 0 7	PUT IN FOR SUBLUP	RETURN 2	Stores accumulator (which is 00C2) in RAM file address 0007.
0075	51BB	0 1 0 1 0 0 0 1 1 0 1 1 1 0 1 1 ADD B B OPERAND	ASSUME NOT OVER 64		Add contents of operand (which is 0074) to contents of file address BB (which is 003F). Store result (which is 00) in accumulator.
076	64EC	0 1 1 0 0 1 0 0 1 1 1 0 1 1 0 0 MCS E C	IS IT OVER 64?		Absolute magnitude comparison between operand (which is 0074) with contents of ROM file address 00EC (which is 0040). Value of operand is greater than file, therefore there is no skip.

Table 5-38. AP Initialization Program - Continued

Label (memory location)	Operation (command hex	Command (binary) 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	Command comment	Storage or constant comment	Functional description
0077	54BB	0 1 0 1 0 1 0 0 1 0 1 1 1 0 1 1 (SUB; ACCUM; B; B)	YES - FIX IT		Subtract file ROM file address 00BB (which contains 003F) from accumulator (which contains 00B3). Resultant (which is 0074) is loaded into accumulator.
0078	2011	0 0 1 0 0 0 0 0 0 0 0 1 0 0 0 1 (STA; 1; 1)	SAVE IT		Contents of accumulator (which is 0074) is stored in RAM file location 0011.

Section XV. WORD FORMATS

5-65. General. The following paragraphs describe the various external and internal word and message formats. All formats, with the exception of the AP and DC program command words, are covered. These command words are described in detail in the associated timing and control logic analyses.

a. *IOX/Console Message Formats.* The IOX determines the operational mode for the display console by means of a repertoire of operation commands. The primary programmed operation command is the device command. This permits the ADP software to instruct the console to assume normal, reset, or maintenance modes of operation. The OFR and ITR operation commands implement the console BIT functions. The EOB opera- tion command terminates the console DOU inhibit. Finally, the device STOP command aborts all current data processing.

(1) For each of the above operations, the IOX activates the command line accompanied by an address byte, followed by a control byte and, if required, one or more data bytes. The address byte is an 8-bit unary code that addresses one of eight consoles. The control byte is coded to indicate the type of operation as follows:

Control byte active bits	Function
0 and 3	Device (DEV)
0 and 4	OFR
0 and 5	ITR
0 and 6	EOB
0 and 7	Device stop (STOP)

The EOB and device STOP operations are self-descriptive and require no additional data information. The device operation is appended by a data byte which indicates the type of console mode required, as follows:

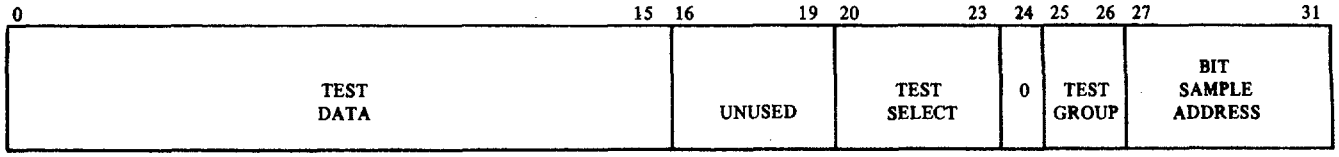
Device operation active data byte bit	Device operation mode type
0	Normal
1	Reset
2	Maintenance

(2) Each OFR operation is appended by four bytes of data information constituting the 32-bit OFR word. There are two types of OFR words (the input buffer test and the noninput buffer test), the type being determined by bit 24 of the word (see fig. 5-91). Bits 24 thru 26 determine the general type of test to be performed (refer to table 5-39). For a noninput buffer test, bits 20 thru 23 select the specific test. Bits 27 thru 31 select the internal console data path for the test data and resultant BIT sample. The BIT sample, when collected, will be requested by the IOX sending an ITR operation. This IOX operation consists of an address byte and a control byte containing the ITR code. The console then replies with four bytes of BIT sample data followed by an indicator signal. (The two last bytes of BIT sample data are the two most significant bytes of the ITR data.) The contents of the two BIT sample bytes constructed by the console and the associated BIT sample addresses are detailed in table 5-40.

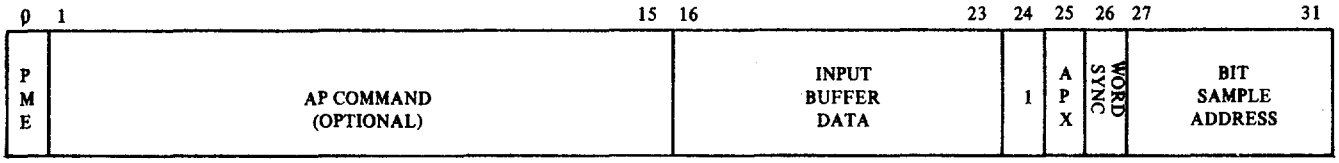
(3) The IOX is also used to transfer the console status word. When the console is prepared to transmit a status word, an active request signal is supplied to the IOX. When the IOX is prepared to accept the status word, an enable signal, accompanied by an address byte, is supplied to the console. The console then replies with the 4 status bytes. The contents of the console status words are detailed in table 5-41.

b. *DOU/Console Message Formats.* During each display refresh cycle, the DOU supplies the console with the complete contents of the CPU main memory store of synthetic data referred to as the display refresh file. There are 16 types of messages, including the test message. The number of words in each message is dependent upon the message type content. The word contents of the various message types is illustrated in figures 5-92 thru 5-106. The display refresh file comprises the complete repertoire of messages for up to eight consoles. Each console is assigned an individual console control, hook marker, and pointer message. The file provides for three safe corridor (each 48 words maxi- mum), six jam strobe (each 24 words maximum), and nine clutter map (each eight words maximum) messages which are available for all consoles. The CPU program alternates track message with map and ARO messages. This provides protection against overloading the input buffer, since map and ARO data require less display time per data word and any one console will have additional time represented by the unused ARO messages.

c. *AP Front Panel Message Formats.* After processing the display refresh file, the AP enters the console status mode. The AP will forward a series of command words to the front panel requesting switch, manual control, and lamp status. The front panel responds with requests and the AP generates enable signals to permit transfer of the appropriate status information. The AP front panel command word formats are listed in table 5-42. The 1 in bit 15 identifies the command as an AP input command; a 1 in bit 14 indicates an AP output command. For an AP output command (lamp data), a data word is appended to the command word. A 1 in any of bits 0 thru 12 of the data word lights the associated lamp in the addressed lamp group (refer to table 5-43). Table 5-44 details the front panel output word formats.



NON-INPUT BUFFER TEST



INPUT BUFFER TEST

NOTE
PME = PROGRAM MEMORY ENABLE
APX = AP EXECUTE

MS200097

Figure 5-91. OFR Data Word Formats

Table 5-39. OFR Test Command Encoding

	Code							
	Group select			Test select				
	24	25	26	20	21	22	23	Test type
	0	0	0	X	0	0	0	Bit sample inhibit
				X	0	0	0	New bit sample
Single				X	0	1	0	Video compressor test
action				X	0	1	1	Reset AP and DC
test				X	1	0	0	Execute AP command
commands				X	1	0	1	Execute DC command
				X	1	1	0	Display buffer test load
				X	1	1	1	AP-DC free run
	0	0	1	X	0	0	0	Input buffer loop enable
				X	0	0	1	Input buffer loop disable
Mode				X	0	1	0	Display buffer loop enable
change				X	0	1	1	Display buffer loop disable
test				X	1	0	0	Run AP to breakpoint
commands				X	1	0	1	Run DC to breakpoint
				X	1	1	0	Force stick test enable
				X	1	1	1	Unused

Table 5-39. OFR Test Command Encoding -Continued

	Code							
	Group select			Test select				
	24	25	26	20	21	22	23	Test type
Radar video mixer test commands	0	1	0	0	0	0	0	Unused
				0	0	0	1	RVM test channel 1
				0	0	1	0	RVM test channel 2
				0	0	1	1	RVM test channel 3
				0	1	0	0	RVM test channel 4
				0	1	0	1	RVM test channel 5
				0	1	1	0	RVM test channel 6
				0	1	1	1	RVM test channel 7
				1	0	0	0	RVM test channel 8
				1	0	0	1	RVM test channel 9
	0	1	1	X	X	X	X	Unused
	1	0	0	Data				Load third byte
Input buffer test commands	1	0	1	Data				Load 3rd byte, word sync
	1	1	0	Data				Load 3rd byte, execute one AP command
	1	1	1	Data				Load 3rd byte, word, sync, execute one AP command

Table 5-40. BIT Sample Data

BIT sample addresses OFR and ITR							BIT sample (ITR)														
(HEX)		27	28	29	30	31	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	0	M ← CENTER SECTION TEST BITS → L															
							+15V	-15V	VIDEO MIXER		Y DEF AMP		X DEF AMP		Y SUM AMP		X SUM AMP		Y DIG.		X DIG.	
0	1	0	0	0	0	1	M ← CENTER SECTION LINE GEN. Y → L															
0	2	0	0	0	1	0	M ← CENTER SECTION CHAR. GEN. → L															
0	3	0	0	0	1	1	M ← CENTER SECTION LINE GEN. X → L															
0	4	0	0	1	0	0	M ← AP LOW SPEED I/O BUS → L															
																AP	ALU CONTROL					
0	5	0	0	1	0	1	M ← AP FILE ADDRESS → L									X	X	$\overline{CO}$	M	$\overline{S3}$	$\overline{S2}$	$\overline{S1}$	S0
0	6	0	0	1	1	0	P15	G15	AP ALU P11	G11	P7	G7	P3	G3	0-3	4-7	8-11	12-15	C12	C8	C4	C16
0	7	0	0	1	1	1	M ← AP DATA BUS → L															
0	8	0	1	0	0	0	M ← AP INPUT BUFFER MEMORY → L															
0	9	0	1	0	0	1	M ← AP FILE DATA → L															
0	A	0	1	0	1	0	M ← AP PROGRAM MEMORY → L															
0	B	0	1	0	1	1	M ← AP COMMAND REGISTER → L															
								AP BUS SELECT														
0	C	0	1	1	0	0	X	$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	X	X	M ← AP PROGRAM ADDRESS → L									

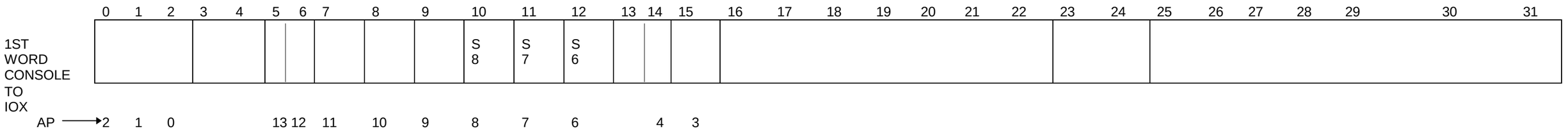
Table 5-40. BIT Sample Data - Continued

BIT sample addresses OFR and ITR							BIT sample (ITR)														
(HEX)		27	28	29	30	31	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	D	0	1	1	0	1	M ← AP INPUT BUFFER RECEIVING REG. → L															
0	E	0	1	1	1	0	M ← AP HIGH SPEED OUTPUT REG. → L															
0	F	0	1	1	1	1	UNASSIGNED															
1	0	1	0	0	0	0	UNASSIGNED															
1	1	1	0	0	0	1	UNASSIGNED															
1	2	1	0	0	1	0	UNASSIGNED															
1	3	1	0	0	1	1	UNASSIGNED															
1	4	1	0	1	0	0	M ← DC LOW SPEED OUTPUT → L															
																DC ALU CONTROL						
1	5	1	0	1	0	1	M ← DC FILE ADDRESS → L									X	XO	M	$\overline{S3}$	$\overline{S2}$	$\overline{S1}$	$\overline{S0}$
1	6	1	0	1	1	0	P15	DC ALU G15	P11	G11	P7	G7	P3	G3	0-3	4-7	8-11	12-15	C12	C8	C4	C16
1	7	1	0	1	1	1	M ← DC DATA BUS → L															
1	8	1	1	0	0	0	M ← DC DISPLAY BUFFER MEMORY → L															
1	9	1	1	0	0	1	M ← DC FILE → L															
1	A	1	1	0	1	0	M ← DC PROGRAM MEMORY → L															
1	B	1	1	0	1	1	M ← DC COMMAND REGISTER → L															

Table 5-40. BIT Sample Data - Continued

BIT sample addresses OFR and ITR							BIT sample (ITR)															
(HEX)		27	28	29	30	31	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
								DC BUS SELECT														
1	C	1	1	1	0	0	X	$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	X	X	X	M	← DC PROGRAM ADDRESS →							L
1	D	1	1	1	0	1	UNASSIGNED															
1	E	1	1	1	1	0	M	← DC HIGH SPEED OUTPUT REG. →														L
1	f	1	1	1	1	1	X	X	X	X	X	X	X	X	RVM TEST				VID COMPRESSOR			

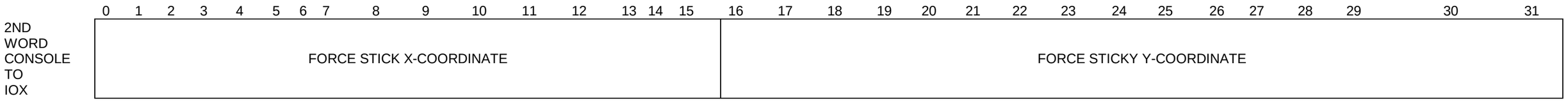
Table 5-41. Console Status Words

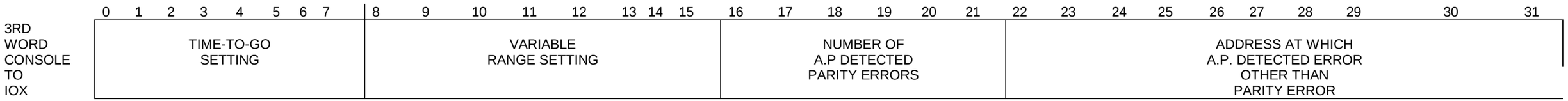


STATUS BITS IN

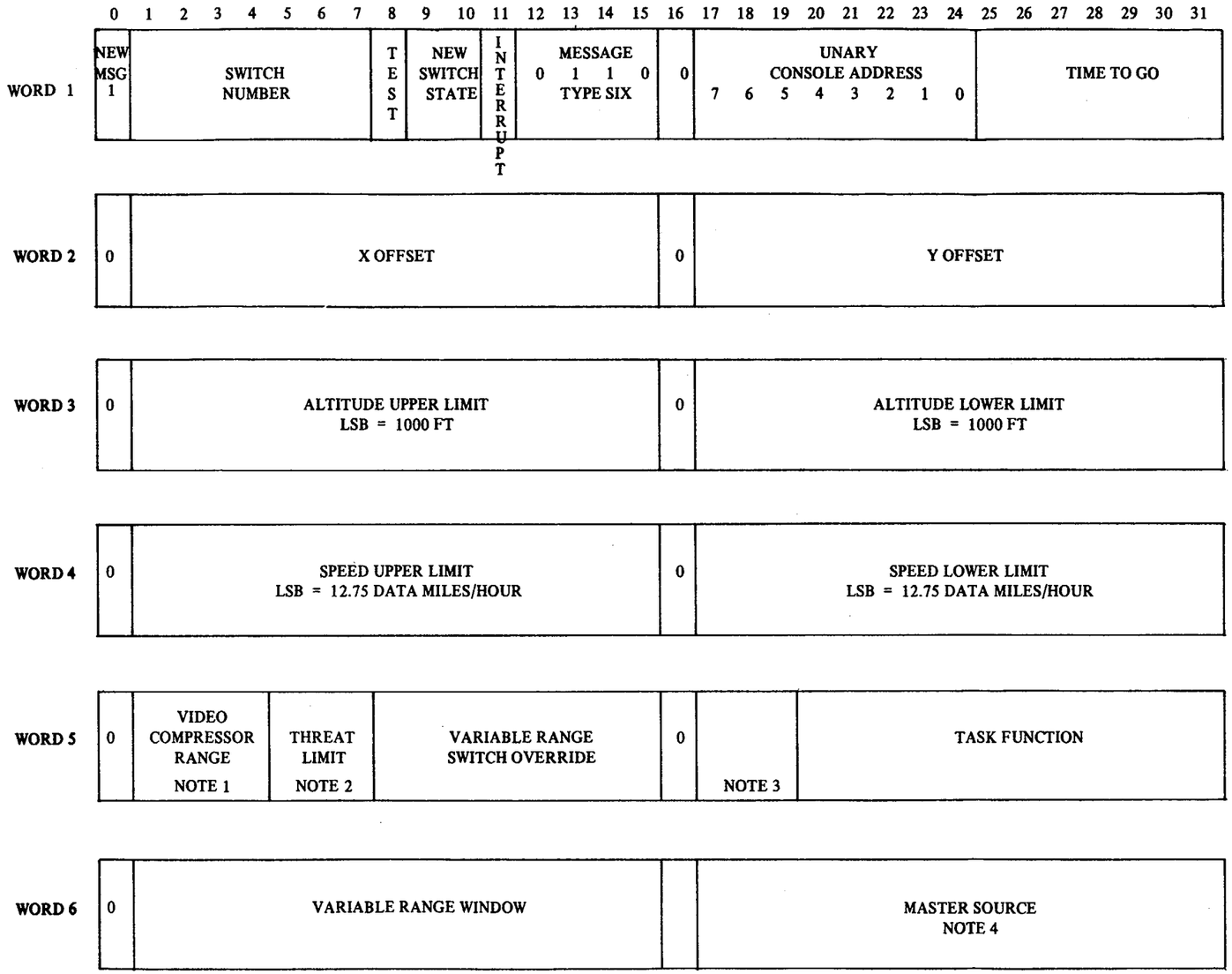
Bit positions	Bit description
0 - 2	CONSOLE NUMBER
3 - 4	ACTION CODE (SWITCH ACTION INPUT CODE) ACTION CODE = 00 NO REPORT MESSAGE = 01 ALPHANUMERIC ENTRY IN BITS 25 - 31 (KEYBOARD Sw. ACTION) = 10 SWITCH STATUS REPORT IN BITS 23 - 31 (NO NEW Sw. ACTION STATUS) = 11 SWITCH ACTION REPORT IN BITS 23 - 31 (Sw. ACTION STATUS)
5	CONSOLE PROCESSING RADAR ONLY
6	DOU MEMORY TIME OUT ERROR
7	DOU MEMORY PARITY ERROR
8	DOU CONTROL WORD PARITY ERROR
9	FILE OVERRUN
10	D.C. SENSE SWITCH 8 (NOT USED)
11	D.C. SENSE SWITCH 7 (SWEEP LOST)
12	D.C. SENSE SWITCH 6 (NO INPUT TO D.C.)
13	A.P. SENSED ERROR
14	CONSOLE TO DOU REQUEST LINE STATUS
15	CONSOLE OFF-LINE OVERRIDE SWITCH
16 - 22	NOT USED
23 - 24	LAMP STATUS OF INDICATED SWITCH/INDICATOR
25 - 31	SWITCH NUMBER OR ALPHANUMERIC CODE

Table 5-41. Console Status Words - Continued





NOTE: WORD 3 IS REPLACED BY TEST DATA FOR A DOU LOOP TEST.



NOTE 1:

BITS 1	2	3	4		
1	1	1	0	=	304 mi
1	1	0	1	=	256 mi
1	0	1	1	=	128 mi

NOTE 2:

BITS 5	6	7		
0	0	0	=	NO THREAT
0	0	1	=	THREAT 1
0	1	1	=	THREAT 2
1	1	1	=	THREAT 3

NOTE 3:

BITS 17	18	19		
1	0	0	=	Variable range + time to go
0	1	0	=	Switch number + new switch state
0	0	1	=	Task Function

NOTE 4:

BIT	SOURCE
17	BATTALION 6
18	BATTALION 5
19	BATTALION 4
20	BATTALION 3
21	BATTALION 2
22	BATTALION 1
23	REMOTE RADAR 2*
24	REMOTE RADAR 1*
25	ADJACENT 2
26	ADJACENT 1
27	GROUP
28	LOCAL MANUAL*
29	LOCAL AUTO*
30	OTHER SERVICE*
31	AMTS – TOS*

*CAN ALSO BE SELECTED FROM THE FRONT PANEL.

MS200098

Figure 5-92. Console Control Message

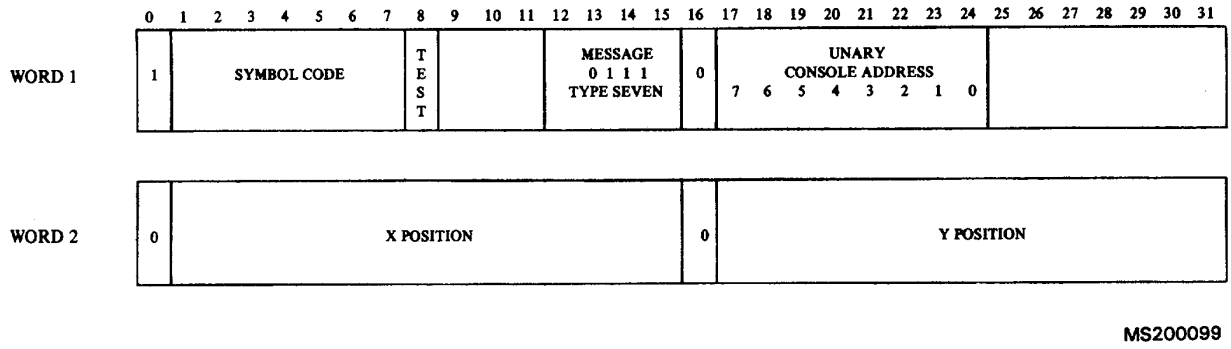


Figure 5-93. Hook Marker Message

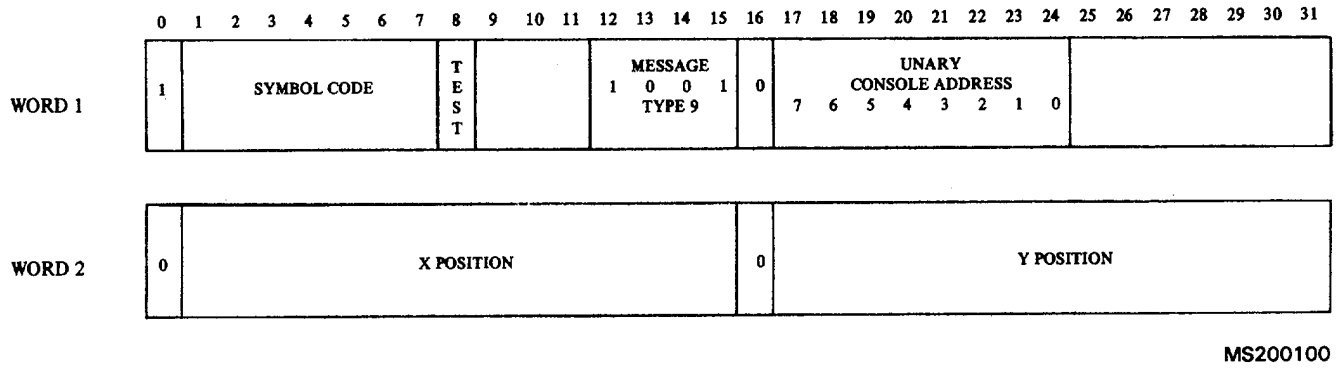


Figure 5-94. Pointer Message

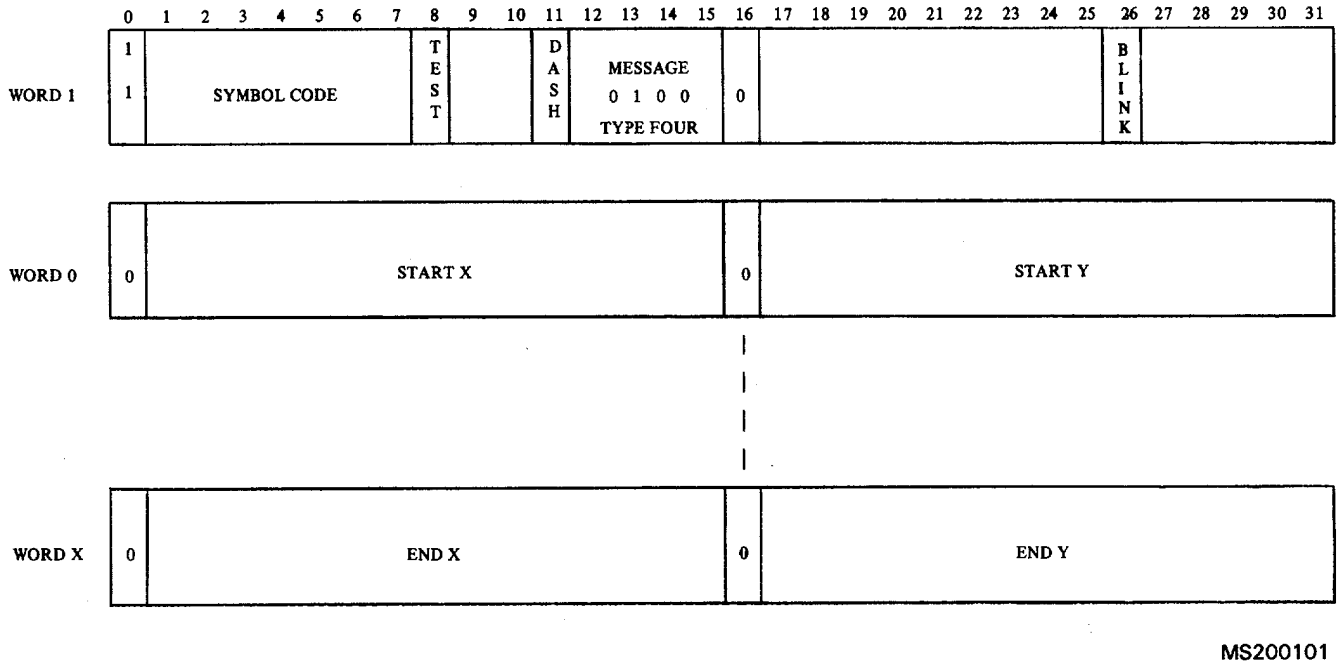


Figure 5-95. Safe Corridor Message

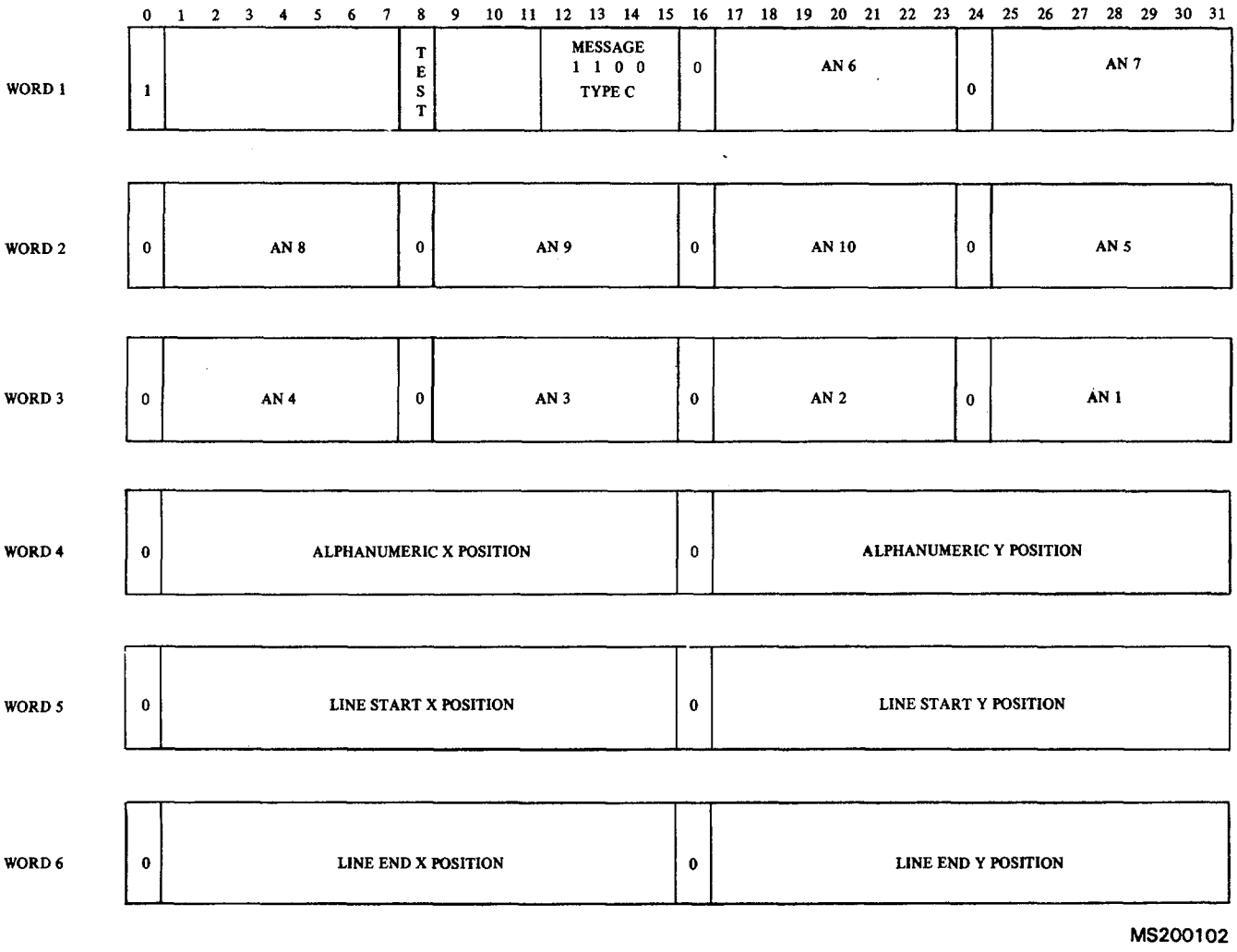


Figure 5-96. Jam Strobe Message

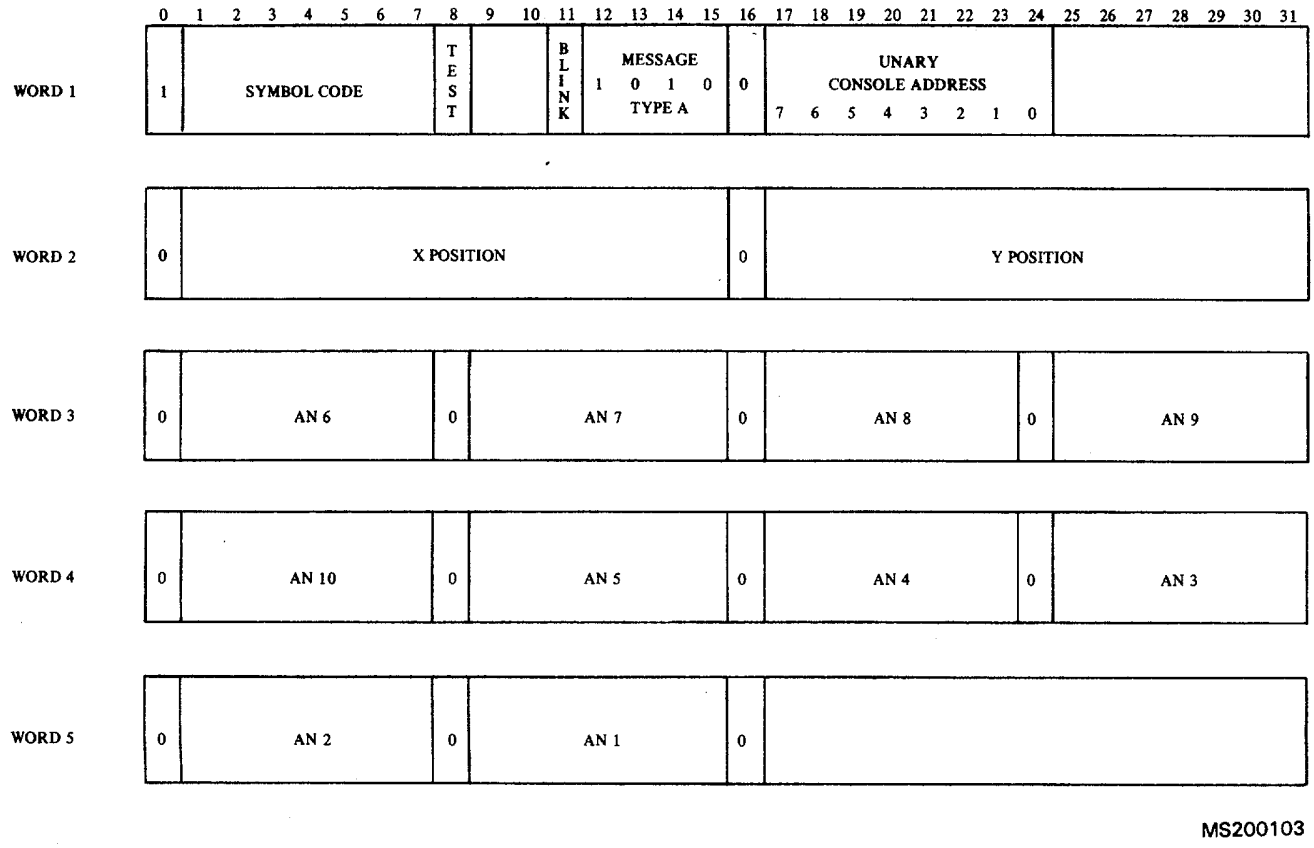


Figure 5-97. Fixed Point Message

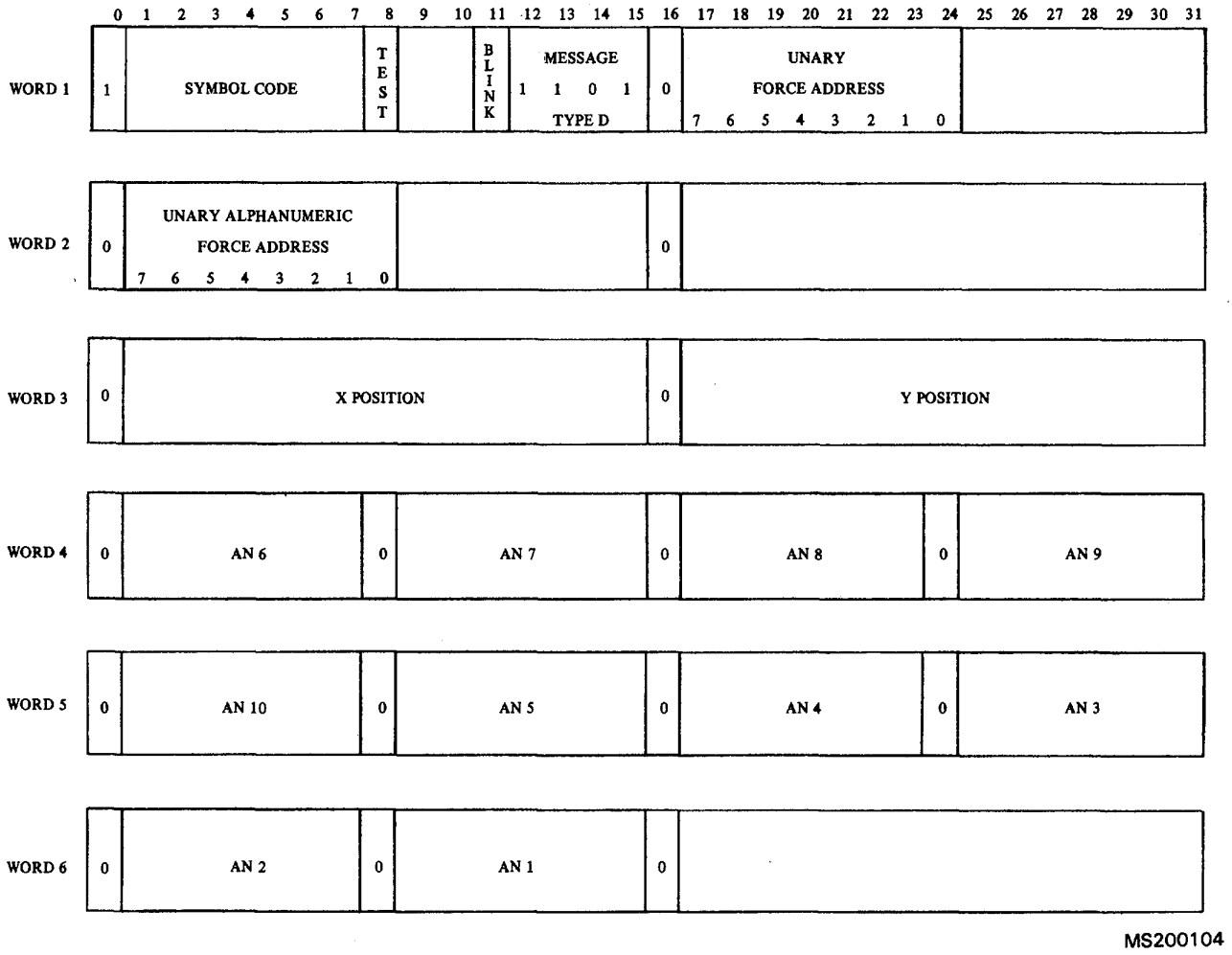
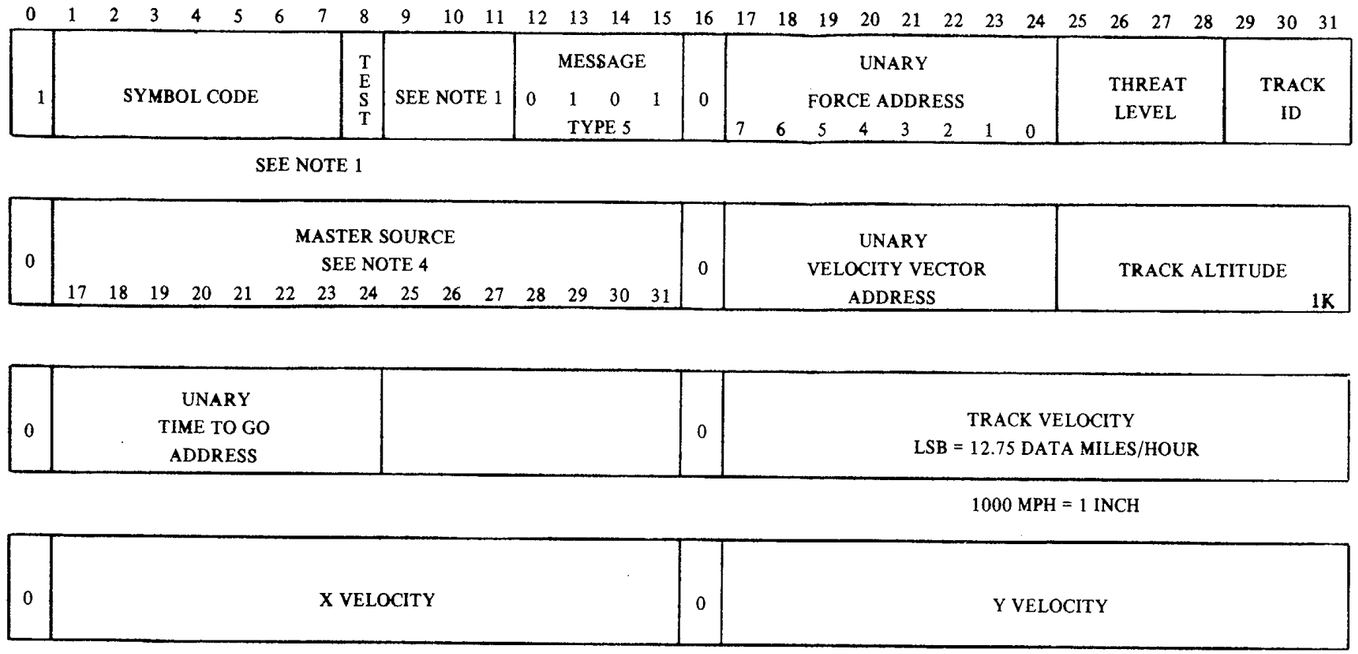


Figure 5-98. Track Marker Message

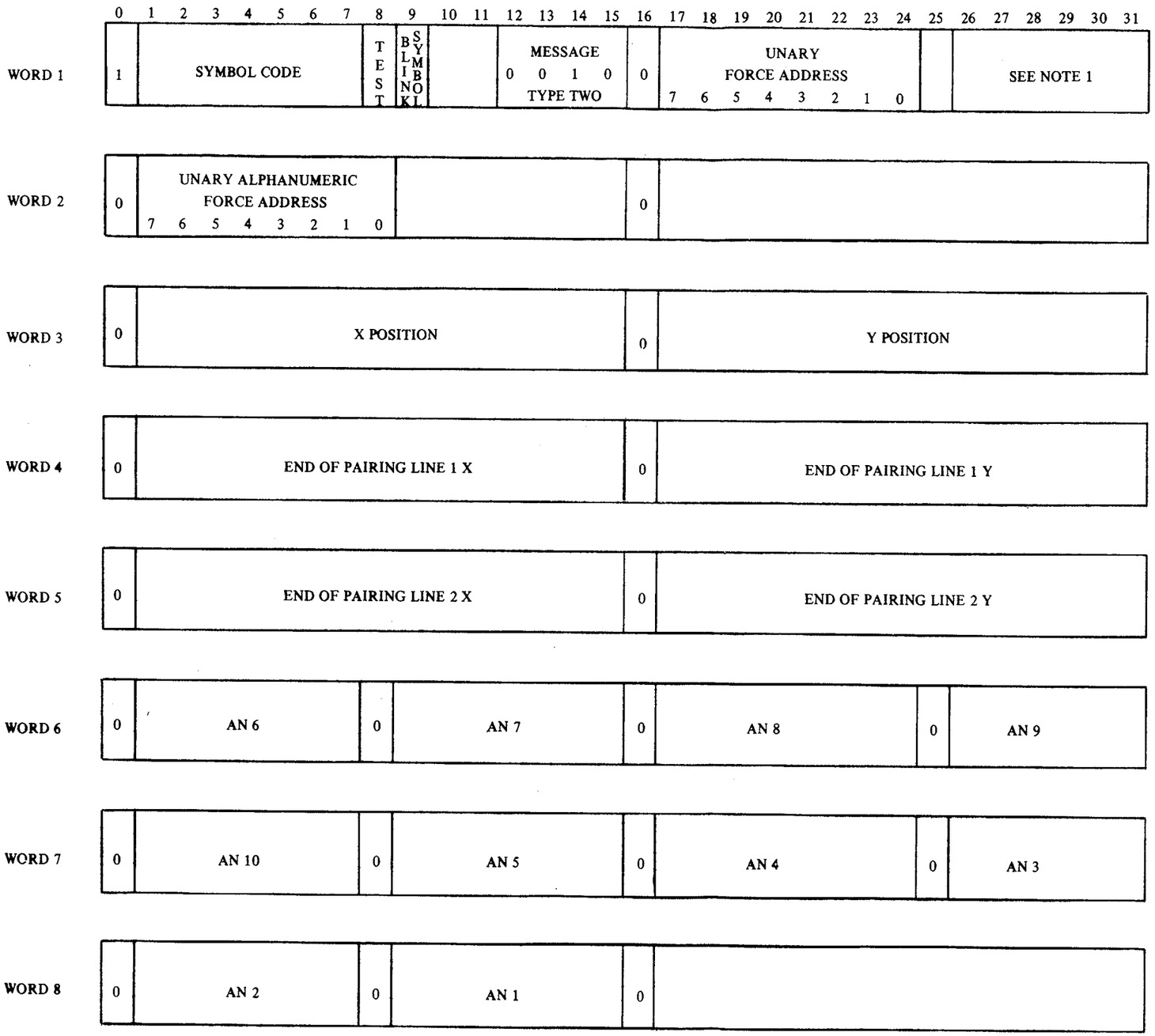


NOTE 1:

BIT	DESCRIPTION
9	SIMULATED TRACK
10	BLINK SYMBOL
11	BLINK LINE

MS200105

Figure 5-99. Track Message



NOTE 1:

BIT	DESCRIPTION
26	DISPLAY PAIRING LINE 1
27	DISPLAY PAIRING LINE 2
28	BLINK PAIRING LINE 1
29	BLINK PAIRING LINE 2
30	DASH PAIRING LINE 1
31	DASH PAIRING LINE 2

MS200106

Figure 5-100. Fire Unit and Site Message

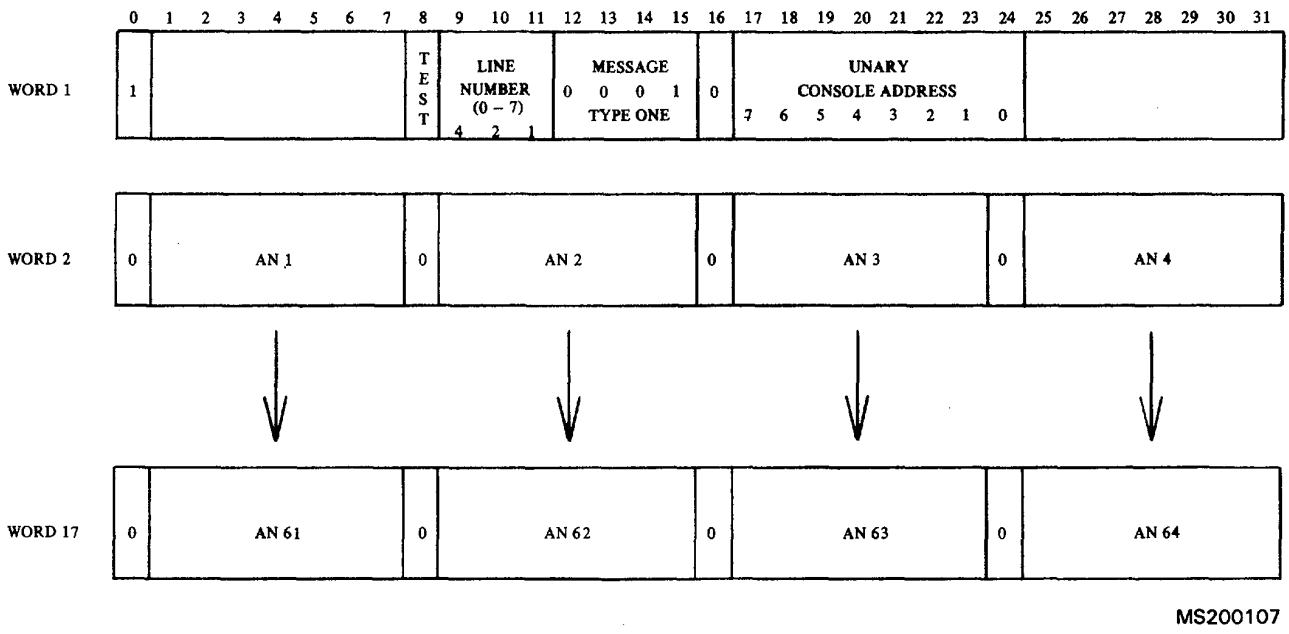


Figure 5-101. Alphanumeric Read Out (ARO) Message

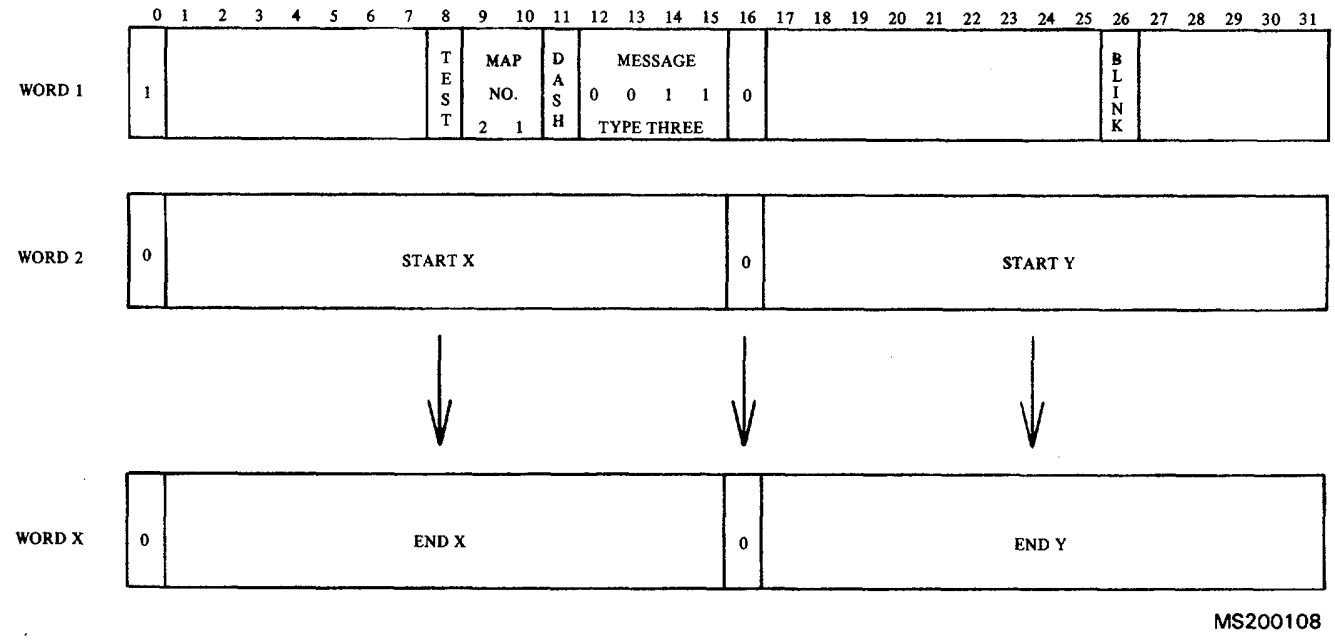


Figure 5-102. Geographic Map Message

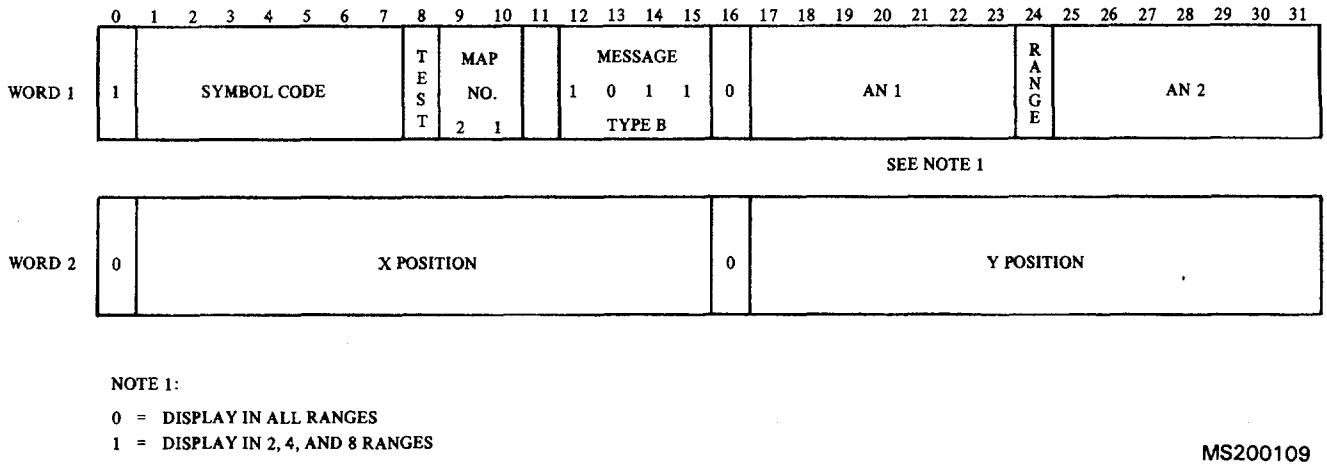


Figure 5-103. Geo Ref Message

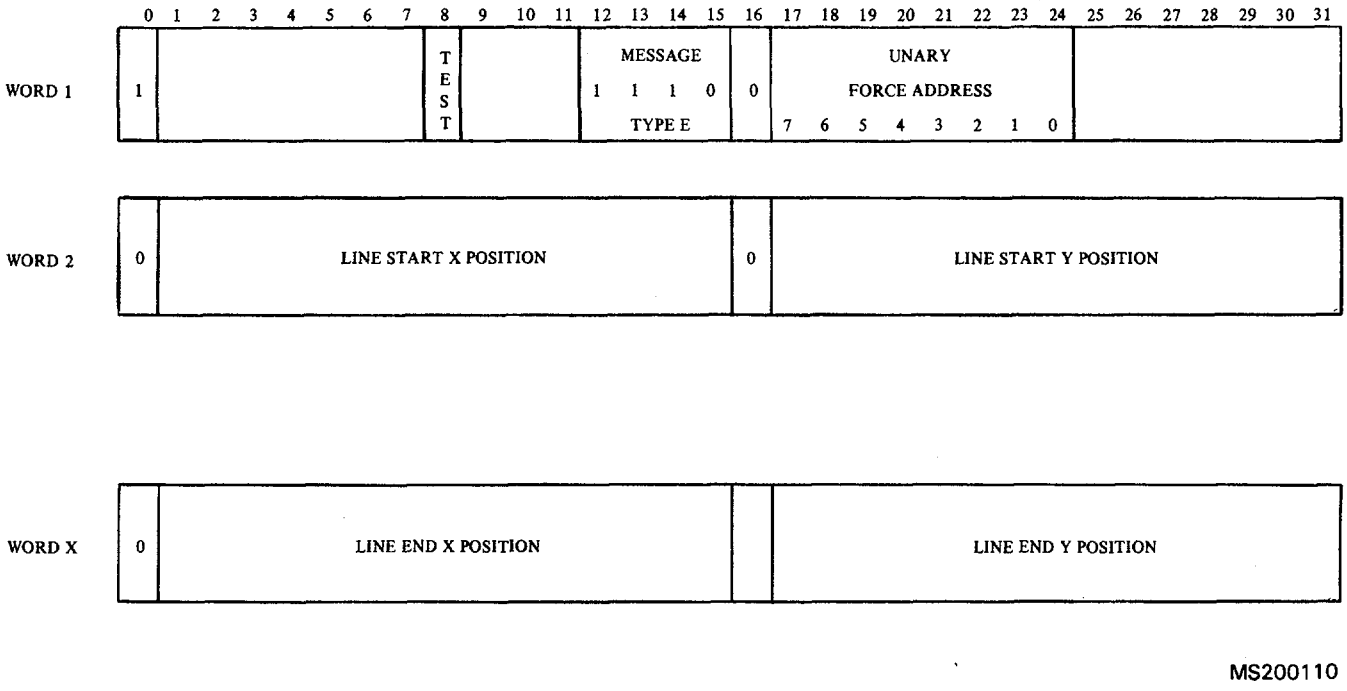


Figure 5-104. Clutter Map Message

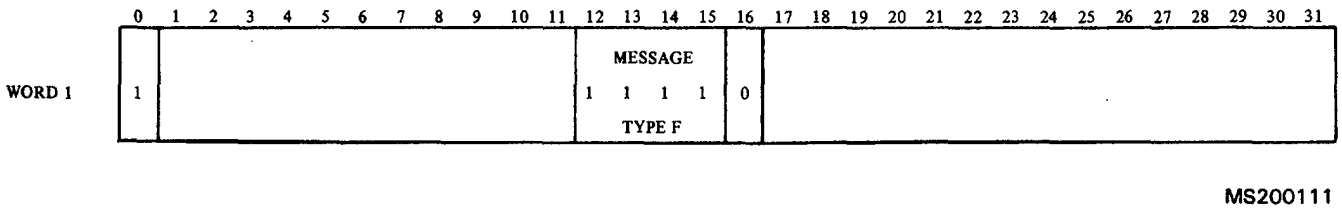


Figure 5-105. End of File (EOF) Message

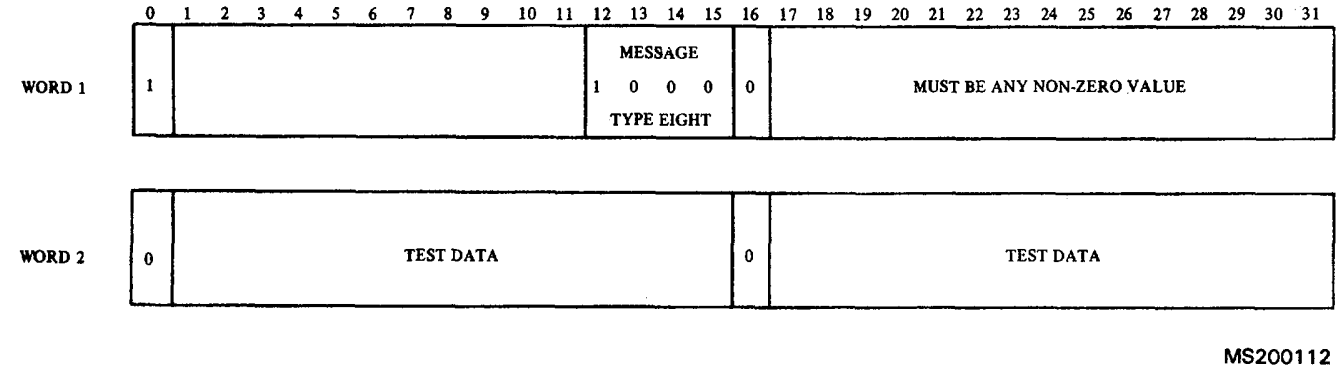


Figure 5-106. Test Message

Table 5-42. AP Front Panel Command Word Formats

Data transfer command	Data bits 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Variable range	1	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0
Force stick	1	0	0	0	0	1	1	0	0	0	0	0	0	0	1	0
Time-to-go	1	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0
Panel switches	1	0	0	0	1	1	1	0	0	0	0	0	0	0	1	0
Lamp status	1	0	Lamp group					1	0	0	0	0	0	0	1	0
Lamp data	0	1	Lamp group					0	0	0	0	0	0	0	1	0

Table 5-43. Lamp Data Formats

Command word lamp group code 13	12	11	10	9	Data word lamp register data 12	11	10	9	8	7	6	5	4	3	2	1
1	0	0	0	0	6	6	5	5	4	4	3	3	2	2	1	1
1	0	0	0	1	12	12	11	11	10	10	9	9	8	8	7	7
1	0	0	1	1	18	18	17	17	16	16	15	15	14	14	13	13
1	0	1	0	0	24	24	23	23	22	22	21	21	20	20	19	19
1	0	1	1	0	30	30	29	29	28	28	27	27	26	26	25	25
1	0	1	1	1	36	36	35	35	34	34	33	33	32	32	31	31
0	0	1	1	0	97	97	96	96	95	95	39	39	38	38	37	37
0	0	0	0	0	45	45	44	44	43	43	42	42	41	41	40	40
0	0	0	0	1	51	51	50	50	49	49	48	48	47	47	46	46
1	0	0	1	0	57	57	56	56	55	55	54	54	53	53	52	52
1	0	1	0	1	63	63	62	62	61	61	60	60	59	59	58	58
0	0	1	1	1	SPARE											
0	1	0	0	0	70	70	69	69	68	68	67	67	66	66	65	65

Table 5-43. Lamp Data Formats- Continued

Command word lamp group code					Data word lamp register data											
13	12	11	10	9	12	11	10	9	8	7	6	5	4	3	2	1
0	0	1	0	1	74	74	73	73	72	72						
1	1	0	0	0	116	116	115	115	114	114	82	82	81	81	80	80
0	0	0	1	1	88	88	87	87	86	86	85	85	84	84	83	83
0	0	1	0	0	94	94	93	93	92	92	91	91	90	90	89	89
0	0	0	1	0	113	113	112	112	111	111						

Table 5-44. Front Panel Output Word Formats

Data bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Variable range (range is comp.)	1	1	1	1	1	1	1	1	MSB	Range →						LSB
Force stick	YSIGN	MSB	Magnitude →					LSB	XSIGN	MSB	→					LSB
Time-to-go (TTG is comp.)	1	1	1	1	1	1	1	1	1	1	TTG					
Panel switches and keyboard SB = 1 for panel switches	SB	MSB	→					LSB	SB	MSB	→					LSB
Lamp data					MSB	→										LSB

Section XVI. GLOSSARY OF TERMS

5-66. General. This glossary provides a convenient reference to various terminology utilized in the console theory. No attempt is made to define standard electronic terminology that is used unambiguously in this manual. Terminology that may vary in context (word, message, etc) and terminology esoteric to the console (force stick, address byte, etc) is included. Terminology that is sufficiently described in the text (alterable processor, FIFO memory, etc) is also omitted.

Accumulator	A 16-bit bi-polar register which provides scratchpad storage for all arithmetic logic unit results and also provides temporary storage of data being transferred between various registers and buffers through the data bus. The accumulator is capable of left or right shifting.
Address byte	The initial byte which accompanies each command or enable from the IOX and contains a unary code addressing one of eight consoles.
Arithmetic logic unit (ALU)	Four 4-stage monolithic integrated circuits which provide all Boolean and arithmetic manipulations of the 16-bit console words.
ASCII code	American Standard Code of Information Interchange which reflects standard character coding for communications and digital data transmission.
Asynchronous operation	Refers to processing of data or commands which are unrelated to the clock system of the receiving device.
Built-in-test (BIT)	Off-line logic incorporated into a device to simulate normal data processing and provide indications of device status as aides for fault isolation.
BIT sample	The 16-bit BIT resultant which is returned to the IOX in response to a test operation.
Branch	The interruption of the program sequence by an instruction which causes the program address counter to utilize the current command utility field for addressing the next instruction.
Buffer	A bipolar register which provides temporary storage of data in order to compensate for asynchronism between the transmitting and receiving device.
Byte	The 8-bit group of data, sometimes accompanied by a parity bit, which constitutes half of the console 16-bit word.
Command line	The line used by the controlling device (the IOX or the AP) to inform the receiving device that a programmed instruction and accompanying data is being supplied over the data lines.
Command	A 16-bit bipolar register used to register temporarily store the current command from the program memory.
Command word	The 16-bit word containing the operation code and utility field which directs data manipulation for each instruction cycle.
Console status word	One of the three 32-bit words which are constructed by the AP and transmitted to the IOX at the end of each display refresh cycle. The words contain console status, error, and front panel switch setting indications.
Control bus	A control line (eg, indicator lines) bussed such that all connected receiving devices are simultaneously supplied with the control signal. Accompanying address information selects the proper device.
Control byte	The 2nd byte supplied with each IOX command or enable signal. This byte indicates the type of operation (device, OFR, ITR, etc).
Data bus	The 16-bit parallel data paths used in the console to transfer information from any of a number of sources to any of a number of destinations.
Data file RAM/ROM	The 256-word constant ROM file and 127-word scratchpad RAM file which provide the primary memory elements for the AP and DC.
Dead time	That portion of the radar pulse repetition period when the transmitter is turned off and no coherent data is received.

Device operation	A programmed IOX operation instruction that determines the general mode (normal, reset, or test) of console operation.
Digilog	A digital-to-analog converter.
Enable line	The control line used by the controlling device (the IOX or the AP), in response to a request, to indicate that the controlling device is prepared to transfer data.
End of block (EOB)	The end of block operation is used by the IOX to clear the console DOU inhibit condition.
Feedback cycle	After the display refresh file is received and processed by the console, the AP enters the feedback cycle when the console status words are constructed and transmitted to the IOX.
Force stick	This data reflects the current contents of the force stick register which indicates any operator action on the POSN TAB control.
High speed buffer	Used to temporarily store and synchronize high speed asynchronous data from the DOU and between the console primary functional assemblies.
Index register/counter	When the index bit (command word bit 9) is a one, the index register/ counter is used to modify the file address reflected by the current utility field. The index register/ counter is a down counter, permitting the file address to be sequentially decremented.
Indicator line	Used by the receiving device as an acknowledgement to a command signal.
Initialization	A series of programmed routines performed when power is applied to the console, which clears all RAM memory locations, conditions front panel lamps for the particular console mode, and reports console status to the IOX.
Input-to-register (ITR)	The ITR operation from the IOX instructs the console to transmit the BIT sample word which was collected as a result of a previous OFR.
Instruction	The operation code of the current command word which determines the type of data transmission, arithmetic, Boolean, branch, or miscellaneous operation to be performed.
Live time	That portion of the radar pulse repetition period when the transmitter is turned on and coherent video data is being received.
Low speed data	Data other than the high speed data required for display refresh (console status and front panel data).
Master reset	Function occurring due to power-on, or console or IOX initiated action that resets all pertinent console logic.
Message	Contiguous group of words that provide various information on a related function (hook marker, safe corridor, console status, etc).
Mnemonic	A 5 to 7 bit alphanumeric designation, unique to each logic signal line, that describes the signal source, logic function, and logic state.
Multiplexer (mux)	A logic element that provides a designed selection matrix (one of ten, one of two, etc).
Operand register	A 16-bit temporary storage register that provides coefficients for Boolean and arithmetic manipulation by the ALU.
Operation code	Bits 10 thru 14 of the command word which. area a hexadecimal code for the particular instruction.
Output from register (OFR)	The OFR operation from the IOX, when preceded by a DEV-3 (test) operation, instructs the console to exercise an addressed portion of the console with an IOX-supplied data word and construct a BIT sample word for subsequent transmission to the IOX.
Parity	An additional bit to an 8-bit byte that causes the 9 bits to reflect an odd number of ones.
Pincushion distortion	Distortion which results in a monotonic increase in radial magnification in a reproduced image away from the axis of symmetry of the electron optical system.
Program	The sequence of instructions that determine how a data processor receives, stores, processes, and transmits information.

Program address counter	A 9-bit register/counter used to access addressed program memory locations.
Radar only display mode	The mode assumed by the console during initialization when radar video is displayed but no synthetic data is processed.
Radar range	Operator selectable data which permits display sweeps to be painted with representative ranges of 128, 256, or 384 miles.
Range max	The point in a radar pulse repetition cycle when the transmitter turns off, terminating live time and initiating dead time.
Range zero	The point which defines the beginning of a radar pulse repetition cycle.
Request	The control line used by a receiving device to indicate that data is available for transmission.
Routine	A sequence of program instructions which is used to perform a general program function (initialization, message processing, console status, etc).
Sense switch	A bistable device, which may be software and/or hardware controlled to provide a referable indication of equipment or data status.
Skip	An instruction to bypass the next sequential instruction dependent upon the current data meeting certain predetermined criteria.
Source code	A 3-bit code contained in bits 7 thru 9 of each copy command word which determines the source of the data to be copied.
STOP operation	The STOP operation is used by the IOX to halt all current console processing.
Sub-routine	A group of related instructions that can be constantly branched in order to perform iterative functions.
Sweep rate	The rate at which sweeps are displayed on the crt.
Sync bit	A separate DOU input line which is activated to indicate that the current byte is the initial byte of a new word.
Synchronous operation	Refers to processing of data or commands that are time-related to the clock system of the receiving device.
Synthetic data	The contents of the DOU display refresh file which contains stored information reflecting hook markers, safe corridors, jam strobes, etc.
Time-to-go	An operator-selected value which is used to extend the tracking of an obscured target.
Unary code	A multiplicity of lines, one of which is activated to indicate data or control content.
Utility field	Bits O thru 9 of the command word which provides supplementary information for processing the associated instruction.
Video data	The seven channels of raw or processed video data from the RIE.

By Order of the Secretary of the Army:

JOHN A. WICKHAM, JR.
General, United States Army
Chief of Staff

Official:

DONALD J. DELANDRO
Brigadier General, United States Army
The Adjutant General

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TEAR ALONG PERFORATED LINE

THE METRIC SYSTEM AND EQUIVALENTS

'NEAR MEASURE

. Centimeter = 10 Millimeters = 0.01 Meters = 0.3937 Inches
1 Meter = 100 Centimeters = 1000 Millimeters = 39.37 Inches
1 Kilometer = 1000 Meters = 0.621 Miles

'VEIGHTS

Gram = 0.001 Kilograms = 1000 Milligrams = 0.035 Ounces
1 Kilogram = 1000 Grams = 2.2 lb.
1 Metric Ton = 1000 Kilograms = 1 Megagram = 1.1 Short Tons

LIQUID MEASURE

1 Milliliter = 0.001 Liters = 0.0338 Fluid Ounces
1 Liter = 1000 Milliliters = 33.82 Fluid Ounces

SQUARE MEASURE

1 Sq. Centimeter = 100 Sq. Millimeters = 0.155 Sq. Inches
1 Sq. Meter = 10,000 Sq. Centimeters = 10.76 Sq. Feet
1 Sq. Kilometer = 1,000,000 Sq. Meters = 0.386 Sq. Miles

CUBIC MEASURE

1 Cu. Centimeter = 1000 Cu. Millimeters = 0.06 Cu. Inches
1 Cu. Meter = 1,000,000 Cu. Centimeters = 35.31 Cu. Feet

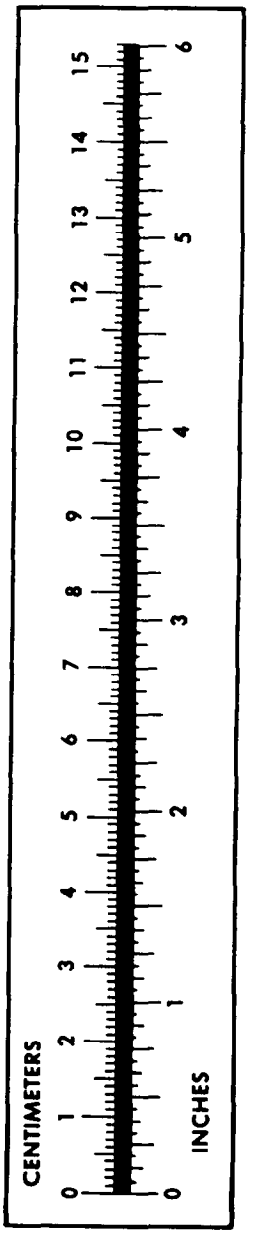
TEMPERATURE

5/9(°F - 32) = °C
212° Fahrenheit is evuivalent to 100° Celsius
90° Fahrenheit is equivalent to 32.2° Celsius
32° Fahrenheit is equivalent to 0° Celsius
9/5C° + 32 =°F

APPROXIMATE CONVERSION FACTORS

TO CHANGE	TO	MULTIPLY BY
Inches	Centimeters	2.540
Feet	Meters	0.305
Yards	Meters	0.914
Miles	Kilometers	1.609
Square Inches	Square Centimeters	6.451
Square Feet	Square Meters	0.093
Square Yards	Square Meters	0.836
Square Miles	Square Kilometers	2.590
Acres	Square Hectometers	0.405
Cubic Feet	Cubic Meters	0.028
Cubic Yards	Cubic Meters	0.765
Fluid Ounces	Milliliters	29.573
ıts	Liters	0.473
arts	Liters	0.946
allons	Liters	3.785
Ounces	Grams	28.349
Pounds	Kilograms	0.454
Short Tons	Metric Tons	0.907
Pound-Feet	Newton-Meters	1.356
Pounds per Square Inch	Kilopascals	6.895
Miles per Gallon	Kilometers per Liter	0.425
Miles per Hour	Kilometers per Hour	1.609

TO CHANGE	TO	MULTIPLY BY
Centimeters	Inches	0.394
Meters	Feet	3.280
Meters	Yards	1.094
Kilometers	Miles	0.621
Square Centimeters	Square Inches	0.155
Square Meters	Square Feet	10.764
Square Meters	Square Yards	1.196
Square Kilometers	Square Miles	0.386
Square Hectometers	Acres	2.471
Cubic Meters	Cubic Feet	35.315
Cubic Meters	Cubic Yards	1.308
Milliliters	Fluid Ounces	0.034
Liters	Pints	2.113
Liters	Quarts	1.057
ers	Gallons	0.264
ms	Ounces	0.035
ograms	Pounds	2.205
Metric Tons	Short Tons	1.102
Newton-Meters	Pounds-Feet	0.738
Kilopascals	Pounds per Square Inch	0.145
lometers per Liter	Miles per Gallon	2.354
meters per Hour	Miles per Hour	0.621



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